ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ
ΣΧΟΛΗ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ
ΚΑΙ ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

ΤΟΜΕΑΣ ΗΛΕΚΤΡΙΚΗΣ ΙΣΧΥΟΣ

Μελέτη, Ανάλυση, Προσομοίωση, Συγκριτική μελέτη Ημιαγωγικών Διακοπτών τύπου Αραίωσης και Πύκνωσης JFETs Καρβιδίου του Πυριτίου και εφαρμογή σε Αντριστροφέα Ισχύος

Διπλωματική Εργασία

του

Νικόλαου Χρυσόγελου

Επιβλέπων : Στέφανος Ν. Μανιάς

Καθηγητής Ε.Μ.Π.

Εργαστήριο Ηλεκτρικών Μηχανών και Ηλεκτρονικών Ισχύος

Αθήνα, Ιούνιος 2014

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Νικόλαος Χρυσόγελος

Διπλωματούχος Ηλεκτρολόγος Μηχανικός και Μηχανικός Υπολογιστών
Ε.Μ.Π.

Περίληψη

Σκοπός της παρούσας διπλωματικής εργασίας είναι η μελέτη, η ανάλυση και η συγκριτική μελέτη μεταξύ ημιαγωγικών διακοπτών τύπου Αραίωσης και Πύκνωσης JFETs Καρβιδίου του Πυριτίου. Οι νέοι ημιαγωγοί μελετώνται και συγκρίνονται με σύγχρονους ημιαγωγούς Πυριτίου που χρησιμοποιούνται μέχρι σήμερα σε εφαρμογές. Ιδιαίτερη έμφαση δίνεται στη συμπεριφορά τους τόσο κατά την ορθή όσο και κατά την ανάστροφη λειτουργία αγωγής. Σκοπός είναι να εξηγηθεί και να διαπιστωθεί κατά πόσον είναι απαραίτητη η προσθήκη αντιπαράλληλων διόδων αγωγής σε διάφορες εφαρμογές ηλεκτρονικών ισχύος. Επιπλέον σχεδιάζονται νέα μοντέλα των ημιαγωγών στο λογισμικό Orcad Pspice έτσι ώστε να γίνει αποτελεσματικά η προσομοίωση τους.

Ύστερα καινοτόμα κυκλώματα οδήγησης σχεδιάστηκαν με σκοπό την αξιοποίηση όσο το δυνατόν περισσότερο των ιδιαιτέρων χαρακτηριστικών των καινούριων ημιαγωγών. Πειραματική μελέτη και σύγκριση μεταξύ τους διεξάγεται έτσι ώστε να καταλήξουμε στην καλύτερη δυνατή λύση. Αφού εξηγηθεί η λειτουργία των κυκλωμάτων και τα σημεία στα οποία πρέπει να δοθεί ιδιαίτερη έμφαση κατά την κατασκευή τους, προχωράμε στην ανάπτυξη μεθόδων με τις οποίες μπορούμε να περιορίσουμε το ανεπιθήμητο φαινόμενο των ταλαντώσεων στις κυματομορφές των τάσεων και ρεύματος εξόδου.

Στο τελευταίο κεφάλαιο, γίνεται η προσομοίωση αντιστροφέων με ημιαγωγικούς διακόπτες Καρβιδίου του Πυριτίου με και χωρίς αντιπαράλληλες διόδους και συγκρίνονται με σύγχρονους αντιστροφείς Πυριτίου. Τέλος, κατασκευάζεται αντιστροφέας μόνο με ημιαγωγούς τύπου Αραίωσης JFET και οι κυματομορφές εξόδου καθώς και η απόδοση του παρουσιάζονται.

Λέξεις Κλειδιά

JFETs Καρβιδίου του Πυριτίου, JFET τύπου Αραίωσης και Πύκνωσης, Κυκλώματα οδήγησης, Κυκλώματα Σβέσης, Αντιστροφέας Ισχύος

Abstract

The purpose of this diploma thesis is the study, analysis and comparison study between Silicon Carbide Depletion Mode and Enhancement Mode JFETs. The new semiconductors are presented and compared with equivalent modern Silicon devices which are used to today applications. Special attention is given to the forward and reverse characteristics of the Silicon Carbide JFETs in order to evaluate and explain if the addition of freewheeling diodes in Silicon Carbide power electronics applications is necessary.

Furthermore, novel gate drive circuits were designed so that it can be possible to exploit the unique features of the new devices. Experimental evaluation and comparison between them is exhibited to conclude to the best solution. After we have explained the operation of the circuits and the points on which special care should be given, we proceed to the development of methods in order to reduce the undesirable problem of oscillations in the output voltage and current waveforms.

In the last chapter, an analytical simulation between power inverters based on Silicon JFETs with and without antiparallel diodes is done and they are compared with up to date Silicon converters. Finally, an inverter consisted only by Depletion Mode JFETs is constructed and the output voltage and current waveforms as well as its efficiency are presented.

Keywords

Silicon Carbide JFETs, Depletion mode and Enhancement mode JFETs, Gate drive circuits, Snubber circuits, Power Inverter.

Ευχαριστίες

Αρχικά θα ήθελα να ευχαριστήσω θερμά τον επιβλέποντα καθηγητής της διπλωματικής μου εργασίας, Στέφανο Μανιά, για την ευκαιρία που μου έδωσε να δουλέψω πάνω σε ένα θέμα το οποίο αρχίζει να απασχολεί ιδιαίτερα την επιστημονική κοινότητα. Επίσης θα ήθελα να ευχαριστήσω τον υποψήφιο διδάκτορα Γεώργιο Καμπίτση για την καθοδήγηση και τη σημαντική του συμβολή τόσο στη θεωτηρική όσο και στην πειραματική ολοκλήρωση της εργασίας μου. Τέλος, οφείλω να δώσω ιδιαίτερες ευχαριστίες στην Γενική Γραμματεία Έρευνας και Τεχνολογίας (ΓΓΕΤ) για το πρόγραμμα ΕΣΠΑ 2007-2013 «Συνεργασία» με κωδικό 09ΣΥΝ-32-1181 για την οικονομική υποστήριξη του έργου «Ανάπτυξη νέων τρανζίστορ και αντιστροφέων ισχύος φωτοβολταικών συστημάτων με χρήση καρβιδίου του πυριτίου» υπο την αιγίδα της οποίας ολοκληρώθηκε η παρούσα εργασία.

Τέλος οφείλω να ευχαριστήσω την οικογένεια μου για τη ψυχολογική και υλική υποστήριξη κατά τη διάρκεια των σπουδών μου και το μικρό μου αδερφό που αποτελεί τη μόνιμη πηγή έμπνευσής μου.

Contents

Chapter 1

WIDE BAND GAP SEMICONDUCTORS

It is worldwide accepted today that a real breakthrough in the Power Electronics field may mainly come from the development and use of Wide Band Gap (WBG) semiconductor devices. In power electronic systems there has been a continuous trend towards a higher system power density in the last decades and due to environmental concerns and rising energy costs, also the efficiency of the systems became an important system performance criteria over the past years besides costs. For meeting these demands, the development of power semiconductors is a crucial factor. WBG semiconductors show superior material properties, which allow operation at high-switching speed, high-voltage and high-temperature. These unique performances provide a qualitative change in their application to energy processing.

From energy generation (carbon, oil, gas or any renewable) to the end-user (domestic, transport, industry, etc), the electric energy undergoes a number of conversions. These conversions are currently highly inefficient to the point that it is estimated that only 20% of the whole energy involved in energy generation reaches the end-user [1]. WBG semiconductors can increase the conversion efficiency thanks to their outstanding material properties.

In the area of power electronic converter systems there is a general trend to higher power densities and higher efficiency which is driven by cost reduction, an increased functionality, saving resources and in some applications by the limited weight/space requirements. In order to continue this trend new devices, which enable high switching frequencies at higher power levels or show reduced losses at moderate switching frequencies are required.

On this chapter a review in the materials of WBG semiconductors is done while their characteristics are presented and compared. After having stated the benefits and drawbacks of the technology of Silicon Carbide (SiC), the different types of SiC semiconductors are displayed. Finally the different variants of SiC JFET are demonstrated in order to choose the right one to build the inverter system which is the scope of this master thesis.

1.1 Characteristics of Wide Band Gap Semiconductors

Power semiconductor devices made from materials with bandgap energies larger than in Si have been touted for many decades. The potential advantages of these wide bandgap devices include higher achievable junction temperatures and thinner drift regions (because of the associated higher critical electric field values) that can result in much lower on-resistance than is possible in Si [2],[3],[4],[5]. Wide bandgap (WBG) semiconductor materials allow power electronic components to be smaller, faster, more reliable, and more efficient than their silicon (Si)-based counterparts. These capabilities make it possible to reduce weight, volume, efficiency and life-cycle costs in a wide range of power applications. Harnessing these capabilities can lead to dramatic energy savings in industrial processing and consumer appliances, accelerate widespread use of electric vehicles and fuel cells, and help integrate renewable energy onto the electric grid.

The continuous development of improved power semiconductors is a key enabling factor for propelling the constantly increasing demand for high power density and higher efficiency in many power-electronic applications. The technological progress in manufacturing power devices based on wide bandgap materials has resulted in a significant improvement of the operating voltage range, of the switching speed and on resistance compared with silicon power devices. On the table 1 various semiconductor materials are presented with their characteristics. [5]

From the table, it can be noted that the materials with a value of thermal conductivity close to or exceeding Si are GaN, GaP, SiC, and C (diamond). This implies higher melting temperatures. Of these four semiconductors, GaP has much lower carrier mobility values than Si. So, one good semiconductor material for the future is C (diamond). It has the largest thermal conductivity and bandgap of any of the materials from Table 1. Diamond also has the largest electron mobility of any material from Table 1 with a bandgap larger than Si.

However, there are some aspects of C (diamond) that make it less than ideal. First, the material and device fabrication technology is much less mature and developed than for SiC and GaN. Second, the thermal expansion coefficient (CTE) for C (diamond) is very low. So there is a clear thermo-mechanical mismatch which would make the package unreliable [5]. Also, the diamond is one of the most expensive materials which make it inappropriate for integration in large scale systems.

On the other hand, GaN and SiC are by comparison to C (diamond) very well suited to typical package materials, and in fact provide a better thermo-mechanical match than Si. In addition, the material and device fabrication technology is much more advanced for SiC and GaN such that the near-term power device development will be directed into these material systems.

Semiconductor Material	Bandgap (eV) Direct, D Indirect, I	Electron Mobility μ_e (cm^2/Vs)	Hole Mobility μ_h (cm^2/Vs)	Density (g/cm^3)	Critical or Breakdown Field E_c (V/cm)	Thermal Conductivity σ_T ($W/(m * K)$)	Coefficient of Thermal Expansion (ppm/K)
Indium antimonide (InSb)	0.17 , D	77,000	850	5.77	1,000	18	5.37
Indium arsenide (InAs)	0.354 , D	44,000	500	5.68	40,000	27	4.52
Gallium antimonide (GaSb)	0.726 , D	3,000	1,000	5.61	50,000	32	7.75
Indium phosphide (InP)	1.344 , D	5,400	200	4.81	500,000	68	4.6
Gallium arsenide (GaAs)	1.424 , D	8,500	400	5.32	400,000	55	5.73
Gallium nitride (GaN)	3.44 , D	900	10	6.1	3,000,000 (3500000 @ vsat = 2.5x107 cm/s)	110	5.4-7.2
Germanium (Ge)	0.661 , I	3,900	1,900	5.32	100,000	58	5.9
Silicon (Si)	1.12 , I	1,400	450	2.33	300,000	130	2.6
Gallium phosphide (GaP)	2.26 , I	250	150	4.14	1,000,000	110	4.65
Silicon carbide (SiC) (3C,β)	2.36 , I	300-900	10 - 30	3.17	1,300,000 @ vsat = 2.5x107 cm/s	700	2.77
Silicon carbide (SiC) (6H,α)	2.86 , I	330-400	75	3.21	2,400,000	700	5.12
Silicon carbide (SiC) (4H,α)	3.25 , I	700			3,180,000 @ vsat = 2.5x107 cm/s	700	5.12
C (diamond)	5.46-5.6 , I	2,200	1,800	3.52	5,700,000 (7000000 @ vsat = 3x107 cm/s)	600-2,000	0.8

Table 1. Characteristics of Wide Band Gap Semiconductor Materials at 300K., [6],[7],[8],[9],[10],[11].

Most discussions of packaging related to wide band gap semiconductors have been with respect to operation at elevated temperatures. A good overview of general problems in using wide bandgap semiconductors and associated packaging at high temperatures is covered by [12]. Silicon Carbide is beginning to be used in commercial power devices though the use of SiC in bipolar devices is questionable. However GaN are also being used in RF and electro-optic applications. Various poly-types of SiC shown in Table 1 have electron mobilities similar, but generally less than in GaN. The hole mobilities are very similar to GaN as well as the CTE values [5].

Consequently, novel and innovative power devices based on WBG semiconductors can play a main role in energy efficient systems. Among the possible candidates to be the base materials for these new power devices, SiC and GaN present the better trade-off between theoretical characteristics (high-voltage blocking capability, high-temperature operation and high switching frequencies), and real commercial availability of the starting material (wafers) and maturity of their technological processes. Table 1 summarizes the main material parameters of WBG semiconductors candidates to replace Si in the next generation of power devices. GaN and especially SiC process technologies are by far more mature and, therefore, more attractive from the device manufacturer's perspective, especially for high power and high temperature electronics. GaN can offer better high-frequency and high-voltage performances, but the lack of good quality bulk substrates is a disadvantage for vertical devices [1].Nevertheless, GaN presents a lower thermal conductivity than SiC.

At present, SiC is considered to have the best trade-off between properties and commercial maturity with considerable potential for both high temperature applications and high power devices. However, the industrial interest for GaN power devices is increasing recently. For this reason, SiC and GaN are the more attractive candidates to replace Si in these applications. In fact, some SiC devices, such as Schottky diodes, are already competing in the semiconductor market with Si power diodes. Currently, it is a sort of competition between SiC and GaN in a battle of performance versus cost. Nevertheless, scientific and industrial actors agree in considering that both will find their respective application fields with a tremendous potential market. However, many of the material advantages still remain not fully exploited due to specific material quality, technology limitations, non-optimized device designs and reliability issues. It is worth mentioning that diamond exhibits the best properties of all the WBG semiconductors. Theoretically diamond would be ideal for bipolar device designs, particularly in operating environments of elevated temperatures. The high values of carrier mobilities, as well as the large bandgap and high thermal conductivity, make diamond the ideal future material for electronic devices of all power levels and types. However, there are critical problems related with the crystal growth (small areas single crystal wafers), both p-type and n-type dopings and processing. Therefore, there is not a diamond power device in the market and it is not expected in the next decade. SiC power devices recently reported in literature include high-voltage and high-temperature diodes, junction controlled devices (like JFETs), MOSFETs and MESFETs. Those based on GaN

include diodes, HEMTs and MOSFETs; and advanced research on novel devices concerning low-losses digital switches based on SiC and GaN is also of main concern. These novel devices represent a real breakthrough in power devices. Furthermore, the development of modelling and electro-thermal characterization tools for these power devices, and the design of their packaging, drivers and controllers which are tried to be done in the following chapters need a great research effort and they represent a world-class innovation.

1.2 Silicon carbide Overview

Silicon carbide (SiC) was accidentally discovered in 1890 by Edward G. Acheson, an assistant to Thomas Edison, when he was running an experiment on the synthesis of diamonds. Acheson thought the new material was a compound of carbon and alumina present in the clay, leading him to name it carborundum, a name that is still being used on some occasions. Silicon carbide occurs naturally in meteorites, though very rarely and in very small amounts. Being the discoverer of SiC, Acheson was the first to synthesize SiC by passing an electric current through a mixture of clay and carbon. Today, SiC is still produced via a solid state reaction between sand (silicon dioxide) and petroleum coke (carbon) at very high temperatures in an electric arc furnace. [13]

Silicon carbide (SiC) is a semiconductor material with highly suitable properties for high-power, high-frequency, and high-temperature applications. This almost worn-out opening statement may be found in many papers dealing with SiC. Yet, it cannot be left out because it really brings forward the essence of the material's potential. Silicon carbide is a wide bandgap semiconductor material with high breakdown electric field strength, high saturated drift velocity of electrons, and a high thermal conductivity. Therefore, these properties make SiC ideally suited for a vast number of applications. Today there are high-frequency metal-semiconductor-field effect transistors (MESFETs) offered commercially, as well as an emerging market for Schottky diodes made from SiC. We are still at the beginning of the SiC revolution, however, and the material's full potential has yet to be realized. During this chapter, we will discuss more details of these exciting properties and provide commercial models currently available in the industry.

Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. The SiC crystals consist of 50% carbon atoms covalently bonded with 50% silicon atoms. There are over 100 different crystal structures (polytypes), each SiC polytype has its own distinct set of electrical semiconductor properties. However, only few polytypes are used for semiconductor production, the cubic 3C-SiC, hexagonal 4H-SiC and 6H-SiC. The [*Figure 1*] indicates the geometrical form of the crystal structure and the number shows the stacking

sequence [14]. A common system of nomenclature used to describe the different crystalline polytypes assigns a number corresponding to the number of layers in the unit cell followed by a letter suffix designating the crystal symmetry; “C” for cubic, “H” for hexagonal and “R” for rhombohedral. The most common SiC polytypes are the 3C, 4H, 6H, 15R and 9T [13], [14]. The cubic 3C is commonly referred to as beta silicon carbide, β-SiC, which has the zinc blend structure, while all other polytypes are referred to as alpha silicon carbide, α-SiC. In general, α-SiC phase is mainly 6H, which is a wurtzite structure.

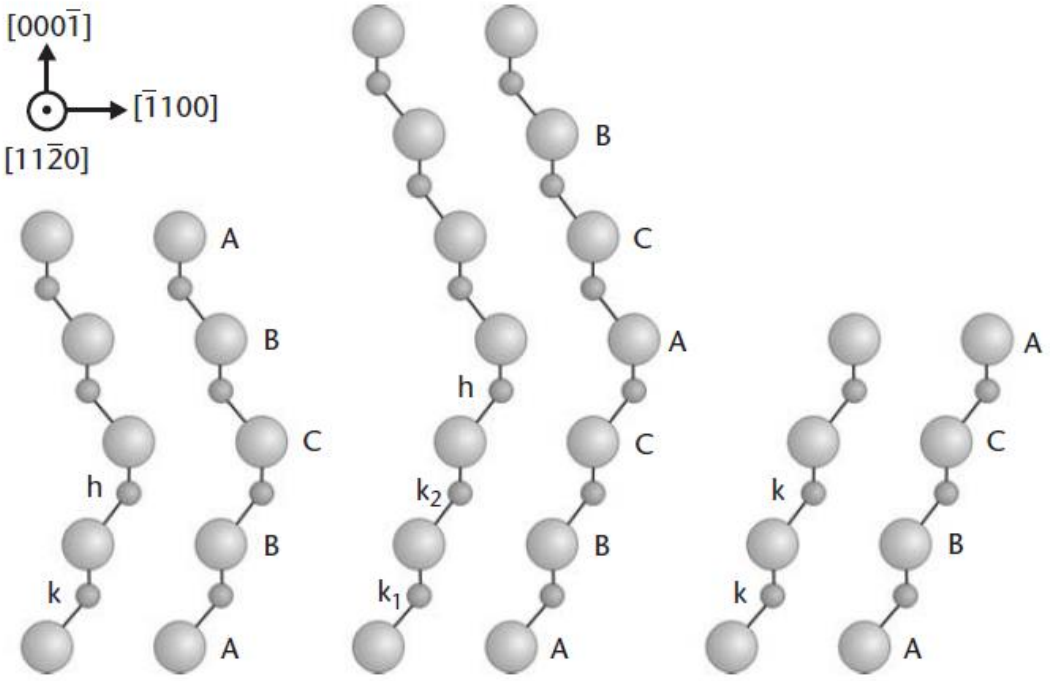

Figure 1. The three most common polytypes in SiC viewed in the [1120] plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; k and h denote crystal symmetry points that are cubic and hexagonal, respectively.

By referencing the possible positions as A, B, and C, we can begin constructing polytypes by arranging the sheets in a specific repetitive order. Thus, the only cubic polytype in SiC is 3C-SiC, which has the stacking sequence ABCABC… The simplest hexagonal structure we can build is 2H, which has a stacking sequence ABAB… The two important polytypes, 6H-SiC and 4H-SiC, have stacking sequences ABCACBABCACB… and ABCBABCB…, respectively.

- **Mechanical and Chemical Properties**

Silicon carbide is a very hard substance. It is chemically inert and reacts poorly (if at all) with any known material at room temperature. It is practically impossible to diffuse anything into SiC. Dopants need to be implanted or grown into the material. Furthermore, it lacks a liquid phase and instead sublimes at temperatures above 1,800°C. The vapor constituents

during sublimation are mainly Si, Si_2C, and SiC_2 in specific ratios, depending on the temperature [14].

- **Bandgap**

The bandgap varies depending on the polytype between 2.36 eV for 3C-SiC to 3.33 eV for 2H-SiC[15]. The most commonly used polytype is 4H-SiC, which has a bandgap of 3.265 eV [15]. The wide bandgap makes it possible to use SiC for very high temperature operation. Thermal ionization of electrons from the valence band to the conduction band, which is the primary limitation of Si-based devices during high temperature operation, is not a problem for SiC-based devices because of this wide bandgap.

- **Critical Field**

For power-device applications, perhaps the most notable and most frequently quoted property is the breakdown electric field strength, $E_{c,max}$. This property determines how high the largest field in the material may be before material breakdown occurs. This type of breakdown is obviously referred to as catastrophic breakdown. Curiously, the absolute value of $E_{c,max}$ for SiC is frequently quoted as the relative strength of the $E_{c,max}$ against that of Si. Most discussions on this subject note that $E_{c,max}$ of SiC is 10 times that of Si. As with Si, there exists a dependence of $E_{c,max}$ with doping concentration. Thus, for a doping of approximately 10^{16} cm^{-3}, $E_{c,max}$ is 2.49 MV/cm, according to a study by Kostantinov et al. [16]. For Si, the value of $E_{c,max}$ is about 0.401 MV/cm for the same doping [17]. As can be seen, the value for SiC is only about a factor of six higher than that of Si and not the often-claimed 10 times higher critical field strength. Why the discrepancy? It is more correct to compare the critical strengths between devices made for the same blocking voltage [14]. Thus, a Si device constructed for a blocking voltage of 1 kV would have critical field strength of about 0.2 MV/cm, which should be compared with the 2.49 MV/cm of SiC. This is where the order of magnitude larger breakdown field spec comes from.

- **Saturated Drift Velocity**

For high-frequency devices, the breakdown electric field strength is not as important as the saturated drift velocity. In SiC, this is 2×10^7 cm/sec [17], [23], which is twice that of Si. A high-saturated drift velocity is advantageous in order to obtain as high channel currents as possible for microwave devices, and clearly SiC is an ideal material for high-gain solid-state devices.

- **Thermal Conductivity**

The second most important parameter for power and high-frequency device applications is the material's thermal conductivity. An increase in temperature generally leads to a change in the physical properties of the device, which normally affects the device in a negative way. Most important is the carrier mobility, which decreases with increasing temperature. Heat generated through various resistive losses during operation must thus be conducted away from the device and into the package. More detailed studies have been made where the thermal conductivity in the different crystal directions have been determined for SiC [17]. As can be seen, there is dependence on the purity of the crystal as well as on the crystal direction. High-purity semi-insulating (SI) SiC material has the highest reported thermal conductivity with a value of 4.9 W/(cm-K). Lower values are measured for the doped crystals but they are all above 4 W/(cm-K) at room temperature [19].

- **Figures of Merit**

There have been several attempts to summarize the importance of various material properties to enable comparisons between materials for high-frequency and high power applications. Johnson suggested a figure of merit, the so-called Johnson Figure of Merit (JFOM)[23], which considers the potential power handling and high frequency capability of a device. The JFOM takes into account the critical field and saturated drift velocity, as shown in the following equation.

$$JFOM = \frac{E_B^2 v_{sat}^2}{4\pi^2}$$

where E_B and v_{sat} are the breakdown field and saturated drift velocity, respectively.

Taking into account the material's thermal properties, which, as mentioned, are specifically apparent during high-frequency operation, Keyes proposed another figure of merit, the Keyes Figure of Merit (KFOM) [21]:

$$KFOM = \kappa\sqrt{\frac{cu_{sat}}{4\pi\varepsilon}}$$

where κ, c, and ε are the thermal conductivity, the speed of light in vacuum, and the dielectric constant, respectively.

Baliga proposed a figure of merit more accurate for power devices for low-frequency applications, called the Baliga Figure of Merit (BFOM) [22]:

$$BFOM = \varepsilon\mu E_B^2$$

where μ is the carrier low-field mobility. In the following Table the figures of merit for the two most common SiC polytypes are compared with Si and GaAs. All values are normalized to Si.

Material	JFOM	KFOM	BFOM
Si	**1**	**1**	**1**
GaAs	**9**	**0.41**	**22**
6H-SiC	**900**	**5.0**	**920**
4H-SiC	**1,640**	**5.9**	**1,840**

Table 2. Comparison of figures of merit between different materials.

With all of these benefits, why hasn't SiC had more of an impact in new products? One reason is the continuous improvements of silicon devices, which benefits from having an infrastructure – process, circuit design, production equipment – that has been fine tuned for over fifty years. By contrast, SiC technology is still in its infancy. The higher cost of SiC devices has been a barrier to most commercial applications. This is due in large part to the fact that SiC is a much more difficult material to process than silicon.

1.3 Silicon Carbide devices

On this paragraph, an overview of the available SiC devices is given. The dramatic quality improvement of the SiC material [25] in combination with excellent research and development efforts on the design and fabrication of SiC devices by several research groups has recently resulted in a strong commercialization of SiC switch-mode devices [25], [26]. Nevertheless, the SiC device market is still in an early stage, and today, some available SiC switches are the JFET [26], [27], BJT [28], MOSFET [29], [30], and Barrier Shottky diode. Commercially available SiC devices are still not in mass production. Thus, the market price of these components is significantly higher than their Si counterparts. On the other hand, because of the low voltage and current ratings of these SiC devices, they are currently not suitable for power ratings above several hundred kilowatts. In particular, voltage ratings in the range of 1,200V and current ratings of few tens of amperes are available. Finally, it is also worth mentioning the progress of the research on the SiC IGBT [26].

- *SiC Barrier Schottky*

The SiC version of this p-n junction may offer many improvements in contrast to Silicon's version. Silicon carbide (SiC) Schottky barrier diodes (SBDs) have been available for more than a decade but were not commercially viable until recently.

The highest performance silicon power diodes are Schottky barrier diodes. Not only do SBDs have the lowest reverse recovery time (t_{rr}) compared to the various types of fast

recovery (fast recovery epitaxial), ultrafast recovery and super-fast recovery diodes, they also have the lowest forward voltage drop (V_F). Both of these parameters are essential to high efficiency. Table 3 shows a comparison of breakdown voltage, V_R, and t_{rr} for commonly available diodes. While Schottky barrier diodes have the advantage of low forward losses and negligible switching losses compared to other diode technologies, the narrow bandgap of Silicon limits their use to a maximum voltage of around 200 V. Si diodes that operate above 200 V have higher V_F and t_{rr}. Silicon carbide devices have higher breakdown voltage, operating temperature and thermal conductivity, as well as shorter recovery time and lower reverse current than silicon diodes with comparable breakdown voltage. These device characteristics equate to low-loss, high-efficiency power conversion, smaller heat sinks, reduced cooling costs and lower EMI signatures. Continuing progress in raising high (250°C) operating temperature and high blocking voltage promise exciting new applications such as motor drive in HEV/EV and solid-state transformers. With silicon fast recovery diodes, the t_{rr} increases significantly with temperature. In contrast, SiC SBDs maintain a constant t_{rr} regardless of temperature. This enables SiC SBD operation at higher temperature without increased switching losses. The numerous SiC SBD performance advantages can result in more compact, lighter power devices with higher efficiency. SiC has demonstrated temperature stability over a wide operating range. This simplifies the parallel connection of multiple devices and prevents thermal runaway.

	Type	V_{br}	V_F	t_{rr}
Si	Schottky Barrier Diode	15V-200V	0.3V-0.8V	<10ns
	Super-Fast Diode	50V-600V	0.8V-1.2V	25ns-35ns
	Ultra-Fast Diode	50V-1,000V	1.35V-1.75V	50ns-75ns
	Fast Recovery (Epitaxial) Diode	50V-1,000V	1.2V	100ns-500ns
	Standard Recovery Diode	50V-1,000V	1.0V	1µs-2µs
SiC	Schottky Barrier Diode	600V-1,200V	1.5V	<15ns

Table 3. Comparison of different types of p-n junction for SiC and Si.

Furthermore, the most remarkable advantage of SiC SBDs is the continuing increase in the blocking voltage and conduction current ratings. They range from the initial 300V, 10 A and 600V, 6 A to the actual 600 V, 20 A and 1.2/1.7 kV. With the latest ratings, it is foreseen that these diodes may replace Si bipolar diodes in medium power motor drive modules. Power Factor Correction and High-Voltage Secondary Side Rectification are applications of 600 V SiC SBDs [40]. Besides, it is expected that SBDs can be advantageously applied for blocking voltages up to 3.5 kV. Large area 3.3 kV SBDs have been fabricated with high-temperature operation [41] that are able to supply forward currents in the range of 20 A. In comparison with Si counterpart, a 10 times increase in voltage blocking is possible with the same SiC drift layer thickness. The main difference to ultra-fast Si PiN diodes lies on the absence of reverse recovery charge in SBDs. Therefore, SiC SBDs are well suited for high switching speed applications. 1.2 kV SiC SBDs match perfectly as freewheeling diodes with Si IGBTs.

- *SiC MOSFET*

Several years have been spent on the research and development of the SiC MOSFET. SiC is the most attractive compound semiconductor, because of its native oxide SiO_2 – comparable to oxides used in Si MOSFETs [42]. This means that the main power devices made-up in silicon, i.e. the power MOSFET, insulated gate bipolar transistor (IGBT), and MOS-controlled thyristor (MCT) can be fabricated in SiC too. However, the fabrication and stability of this oxide layer has been challenging. SiC oxides are not showing the same reliability as in Si MOSFETs. They have higher threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFET's, [43]. One of the obvious differences between thermal oxidations of Si and SiC to form SiO_2 is the presence of carbon in SiC. While most of the C in SiC converts to gaseous CO and CO_2 and evaporates from the oxide layer during thermal oxidation, remaining C resides near the SiC-SiO_2 interface. This has detrimental impact on SiO_2 electrical quality [44]. Consequently much longer and higher temperature maintenance (annealing) is required to improve the SiC oxide quality.

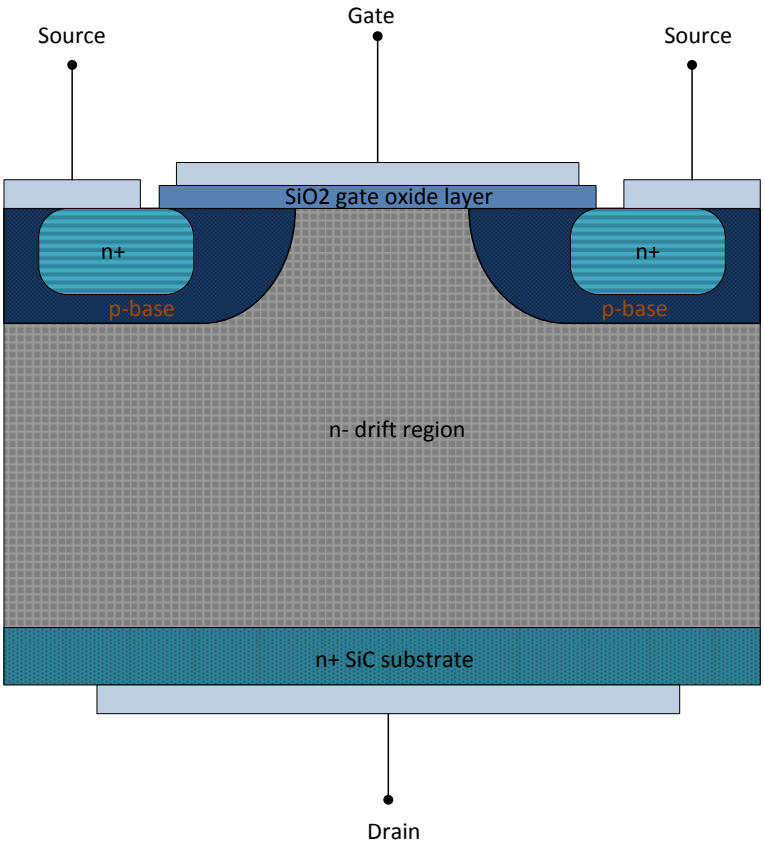

Figure 2. **Cross section of 4H-SiC Vertical Double Implanted MOSFET (DIMOS).**

In [46] differences between the basic electrical properties of n-type versus p-type SiC MOS devices are discussed. A cross section of a popular commercialized Vertical Double Implanted SiC MOSFET (DIMOS) structure is shown in [**Figure 2**] while in [45] a SPICE model for the DIMOS transistor has been developed and implemented in the circuit simulator Orcad PSpice 10.5. The normally off behavior of the SiC MOSFET makes it attractive to the designers of power electronic converters. Unfortunately, the low channel mobilities cause additional on-state resistance of the device and thus increased on-state power losses. Additionally, the reliability and the stability of the gate oxide layer, especially over long time periods and at elevated temperatures, have not been confirmed yet. Fabrication issues also contribute to the deceleration of SiC MOSFET development. However, the currently presented results regarding the SiC MOSFETs are quite promising, and it is believed that such devices will be available for mass production within a few years. The SiC MOSFET is the most recent SiC switch, which was released during the end of 2010 from Cree, while other manufacturers (e.g., ST Microelectronics) have released their own MOSFET in SiC during the last years [25], [30]. At present, 1.2-kV SiC MOSFETs with current ratings of 10–20 A and on-state resistances of 80 and 160 mΩ are available on the market. Furthermore, SiC MOSFET chips rated at 10 A and 10 kV have also been investigated by Cree as a part of a 120-A half-bridge

module [47]. When compared with the state of-the-art 6.5-kV Si IGBT, the 10-kV SiC MOSFETs have a better performance.

It is worth mentioning that except from DIMOSFET (**Figure 2**) other designs of this type of semiconductor have also been proposed like the classical U-groove n channel power Mosfet (UMOSFET), which is a vertical device which comprises epitaxially grown thick n-drift region and p-type base region, and SiC power lateral DMOSFET (LDMOS). However it is not in the goals of this thesis to go in deep with the SiC MOSFET structures and more details can be found in [13].

- *SiC IGBT*

The Si-based IGBT has shown an excellent performance for a wide range of voltage and current ratings during the last two decades [49]. The fabrication of a Si n-type IGBT started on a p-type substrate. Such substrates are also available in SiC, but their resistivity is unacceptably high and prevents these components from being used in power electronics applications. Furthermore, the performance of the gate oxide layer is also poor, resulting in high channel resistivities. These issues have already been investigated by many highly qualified scientists, and it is believed that such SiC devices will not be commercialized within the next ten years [26], [39]. On the contrary, even if high-voltage SiC IGBTs will be commercially available in the future, it is not obvious that they will give low-power losses as a high-voltage SiC JFET (e.g., 3.3-kV SiC JFET) if modularized circuits such as modular multilevel converter (M2C) are used for high-voltage high-power applications [48].

- *SiC BJT*

The SiC BJT is a bipolar normally off device, which combines both a low on-state voltage drop (0.32 V at 100 A/cm^2) [45] and a quite fast switching performance. It has been deeply investigated, designed, and fabricated by TranSiC. A cross section of this device is shown in [*Figure 3*], where it is obvious that this is an NPN BJT. The low on-state voltage drop is obtained because of the cancellation of the base-emitter and base-collector junction voltages. The SiC BJT is a current-driven device, which means that a substantial continuous current is required as long as it conducts a collector current. The available SiC BJTs have a voltage rating of 1.2 kV and current ratings in the range of 6–40 A, while current gains of more than 70 have been reported at room temperature for a 6-A device [46]. The fabrication of the SiC BJTs with improved surface passivation leads to current ratings of 50 A at 100^{o}C. However, the current gain is strongly temperature dependent, and in particular, it drops by more than 50% at 250^{o}C compared with room temperature. The development of SiC BJTs has been successful, and in spite of the need for the base current, SiC BJTs having competitive performance in the kilovolt range are expected in the future [49], [13].

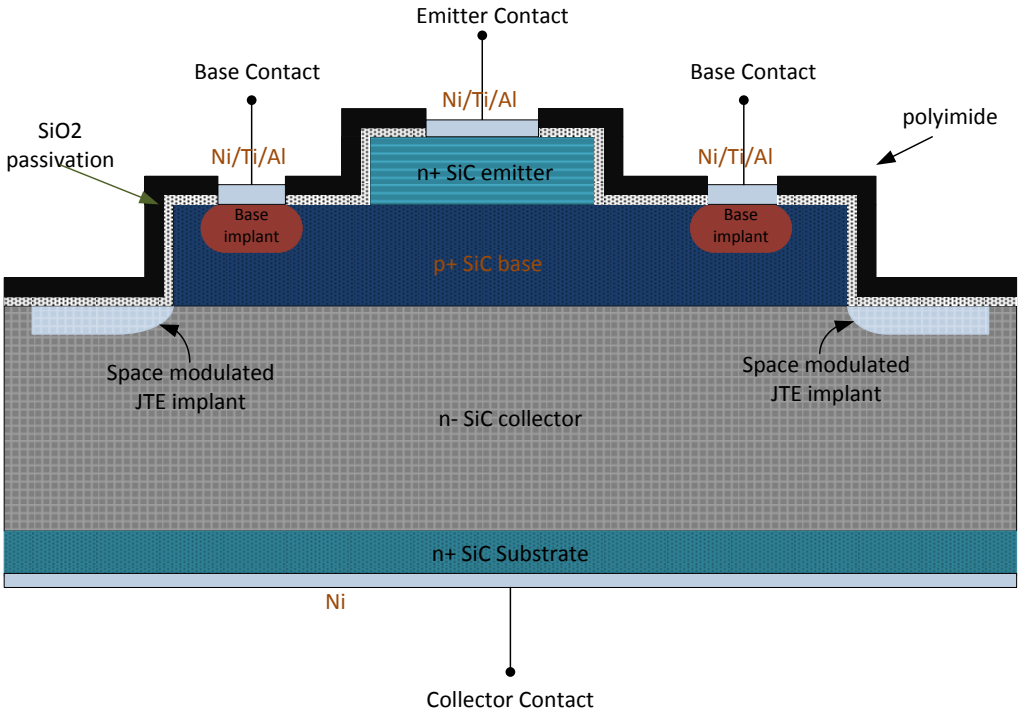

Figure 3. Cross section of SiC BJT.

- *SiC JFET*

A Junction Field Effect Transistor (JFET) has no SiO2-SiC interface and could therefore be available as a commercial power device within a few years. As soon as the prices for SiC substrates reduce and large area chips without defects appear on the market, a family of 0.5-6 kV JFETs can be produced. The high quality of the conduction channel and good control of the channel dimensions and doping are crucial for the JFET performance. The normally-on (N-on) JFET design is capable of extremely low on-state resistance. Normally-on JFETs are not easily accepted by the market due to system safety requirements, regardless of their excellent on-resistance. N-off JFETs on the other hand require a narrow and relatively low doped channel to ensure the N-off performance, and thus pay a penalty in terms of the on-state performance. N-off JFETs are also vulnerable to the electromagnetic interference (EMI) noise due to the small range of the gate control voltage. Hence, the gate control circuitry for JFETs requires special attention to ensure reliable operation. In the case of N-on JFETs the development of inherently safe gate drivers is particularly desired in order to guarantee the safety of the whole system [52].

Another significant difference between the JFET and the MOSFET is that the MOSFET is normally-off, whereas the JFET can be either normally-on or normally-off. Normally-on means that the JFET conducts if no voltage is applied to the gate. This may lead to large transient current flows at system power-up. Because of this feature the power JFET has been

dismissed as an undesirable device according to Baliga [53] for instance. The discussion whether normally-on devices should be used in power electronics or not is not a new discussion. During the last decades different possible devices in Si have been proposed, and up to now normally-off devices have been chosen for large-scale use. For the SiC JFET it is perhaps wiser to discuss whether we could manage without it or not [50]. Having such an opportunity to reduce the losses, the normally-on problem appears to be secondary at the first glance. According to Mihaila et al. [54], a 6.5 kV SiC JFET will have a lower voltage drop than a SiC trench MOSFET even though the JFET is much simpler to manufacture. In order to obtain information on the system aspects of a normally-on device, a number of interviews with industry representatives have been performed.

The first attempts to design and fabricate a SiC JFET were made in the early 1990s when the main research issues were dealing with the design optimization to realize high-power and high-frequency SiC devices [31]. It was during these years that a few research groups had started mentioning the advantageous characteristics of the SiC material compared with Si [32], [33]. However, from the structure design point of view, the early-year SiC JFET was suffering from relatively low transconductance values, low channel mobilities, and difficulties in the fabrication process [32], [33]. During the last decade, the improvement on the SiC material and the development of 3- and 4-in wavers have both contributed to the fabrication of the modern SiC JFETs [26], and it was around 2005 when the first prototype samples of SiC JFETs were released to the market. The commercially available SiC JFETs are mainly rated at 1,200 V, while 1,700 V devices are also available on the market. The current rating of normally on JFETs is up to 48 A, and devices having on-state resistances of 100, 85, and 45 mΩ at room temperature can be found. As for the normally on JFETs, the normally off counterparts are available at current ratings up to 30 A and have on-state resistances of 100 and 63mΩ. On the next paragraph we demonstrate analytically the different variants of this type of Silicon-Carbide semiconductor.

1.4 Silicon Carbide Junction gate Field-Effect Transistor Variants

There are several ways of designing a SiC JFET. Depending on which applications are aimed at or which specific features are desired, different JFET structures have been developed.

- ***Lateral Channel JFET (LCJFET)***

The most successful JFET type in terms of voltage and current ratings has been the lateral channel JFET developed by SiCED [55]. A schematic drawing of the LCJFET design is shown in *Figure 4*. The LCJFET allows optimal control of the channel parameters and offers the largest ease of fabrication compared to other concepts. It also offers the use of the inherent body diode as an anti-parallel diode in switching applications since the buried gate is preferably connected to source. This is necessary in order to reduce the Miller capacitance and thus maintain high speed operation. The original LCJFET structure uses ion-implantation for the gate and the base region, and planar epitaxial growth for the defect-free channel layer. This leads to advantages in terms of ease of fabrication, freedom of parameter choice due to a wide design window, and small fabrication tolerances. The disadvantage is a relative large specific on resistance, which is related to the large cell pitch due to the lateral configuration of the channel. In addition, the large cell pitch of 10 to 16 μm makes the use of both gates for the conduction control not feasible due to the prohibitively large gate charge required during switching. The concept is also characterized by relatively low saturation current levels and in order to achieve low on-state resistance, the demonstrated LCJFET designs are typically of N-on type. In [51] it is stated that the N-off design is not feasible with the LCJFET concept.

The load current through the device can flow in both directions depending on the circuit conditions, and it is controlled by a buried p^+ gate and an n^+ source p-n junction. This SiC JFET is a normally on device, and a negative gate-source voltage must be applied to turn the device off. By applying a negative gate source voltage, the channel width is decreased because of the creation of a certain space-charge region, and a reduction in current is obtained. There is a specific value of the negative gate-source voltage, which is called ‘‘pinch-off voltage,’’ and under this voltage, the device current equals zero. The typical range of the pinch-off voltages of this device is between -16 and -26 V. An important feature of this structure is the antiparallel body diode, which is formed by the p^+ source side, the n^- drift region, and the n^{++} drain. However, the forward voltage drop of the body diode is higher compared with the on-state voltage of the channel [26], [34] at rated (or lower) current densities. Thus, for providing the antiparallel diode function, the channel should be used to minimize the on-state losses. The body diode may be used for safety only for short-time transitions [35]. This type of SiC JFET has been released by SiCED (Infineon) a few years ago.

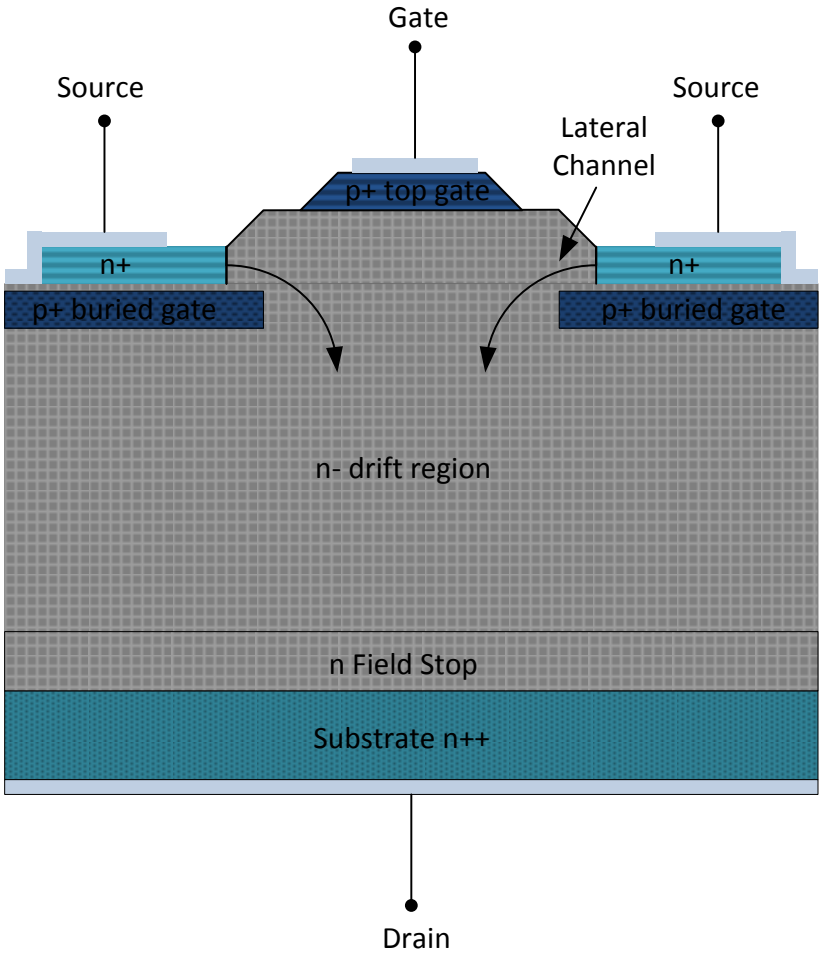

Figure 4. **Cross section of SiC Lateral Channel JFET (LCJFET).**

- ***Vertical Trench JFET (VTJFET)***

The second commercially available SiC JFET is the vertical trench (VTJFET), which was released in 2008 by Semisouth Laboratories [35], [36]. A cross-section schematic of its structure is shown in Figure 5. The VTJFET SiC JFET can be either a normally off (enhancement-mode VTJFET-EMVTJFET) or a normally on (depletion-mode VTJFET-DMVTJFET) device, depending on the thickness of the vertical channel and the doping levels of the structure. As other normally on JFET designs, a negative gate-source voltage is necessary to keep it in the off state. On the other hand, a significant gate current (approximately 200 mA for a 30-A device) is necessary for the normally off JFET to keep it in the conduction state. The pinch-off voltage for the DMVJFET equals approximately -6 V, whereas the positive pinch-off voltage for the normally off one is slightly higher than 1 V. Comparing this type of SiC JFETs to the LCJFET there is no physical antiparallel body diode

in this design [49]. However, the VTJFET can conduct current in the reverse direction. When the vertical-channel JFETs are used for freewheeling purpose, the reverse-recovery currents are only caused by the depletion charge of the device and no minority injection is involved. This is different and superior to devices with parasitic reverse P–N junction diodes like MOSFETs or lateral–vertical JFETs and is because of the symmetrical structure of the design [56]. More details for this type of JFET will be demonstrated on the following chapter.

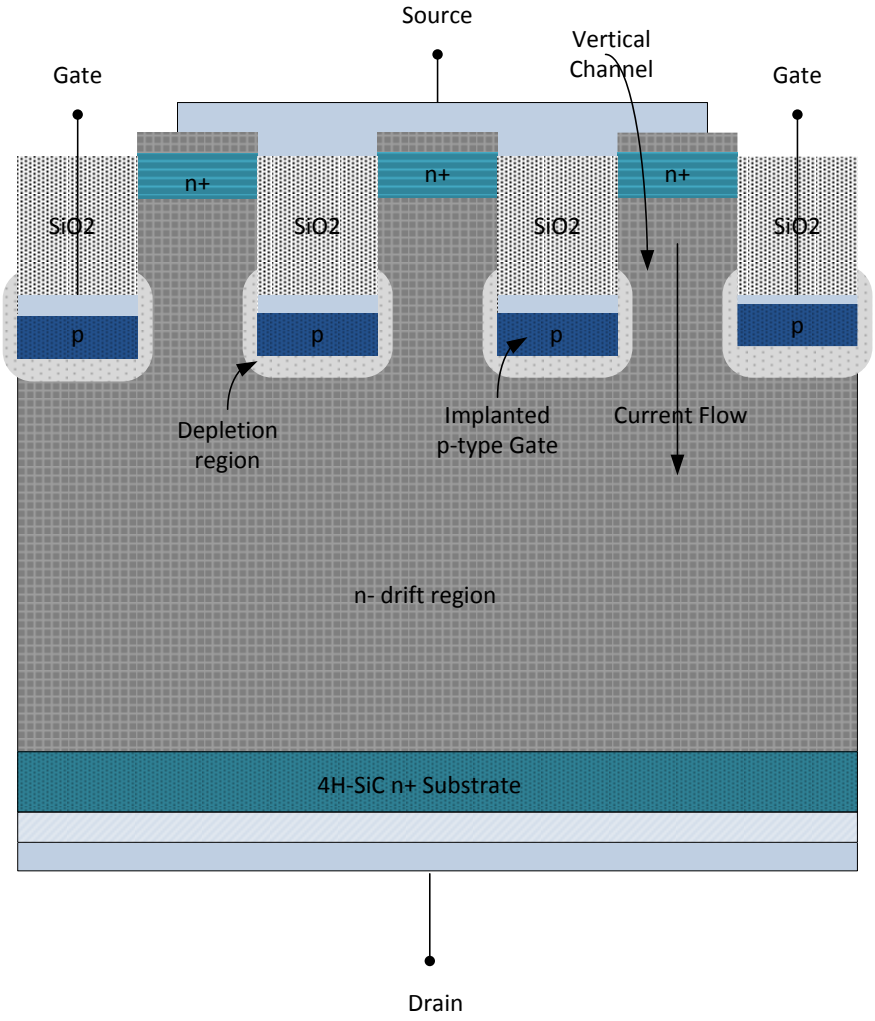

Figure 5. **Cross-section of Vertical Trench JFET produced by Semisouth (VTJFET).**

- ***Buried Grid JFET (BGJFET)***

The single gate drive with the buried gate connected to the source is necessary to mitigate the large Miller effect related to the large cell pitch that otherwise dominates the turn-off behavior. The large cell pitch and the single gate drive make the saturation current levels prohibitively low for any power switching application. A schematic drawing of the BGJFET

design is shown in *Figure 6*. The main advantage of the vertical BGJFET concept is the small cell pitch that makes low specific on-state resistance and high saturation current densities possible. Furthermore, the inherent symmetric gate drive and the wide design window for the channel length, width, and doping make the N-off design feasible. The disadvantage is that optimization of the channel doping is not as easy as in the case of the lateral channel growth. Trenches have to be etched in the p-doped grid layer. These etched trenches must be epitaxially refilled to full extent. In the case of an implanted grid the possible use of higher doping in the channel is limited by the necessity to compensate the higher doped n-layer on top of the drift layer by the p-type grid implant. The channel doping in this concept is ultimately limited by the tolerances of the photolithography and trench etching process. Another disadvantage is that the use of the integral gate to drain body diode is not readily available with this concept. Consequently, the absence of the antiparallel body diode and the difficulties in the fabrication process compared with the LCJFET count as two basic drawbacks of this design. Finally, The BG VJFET can be designed with different threshold voltages (V_{th}), thus displaying so-called normally-on (N-on) and normally-off (N-off) characteristics. It is important to evaluate the performance of the BG VJFET with different threshold voltage designs in order to select the best device for a given application.

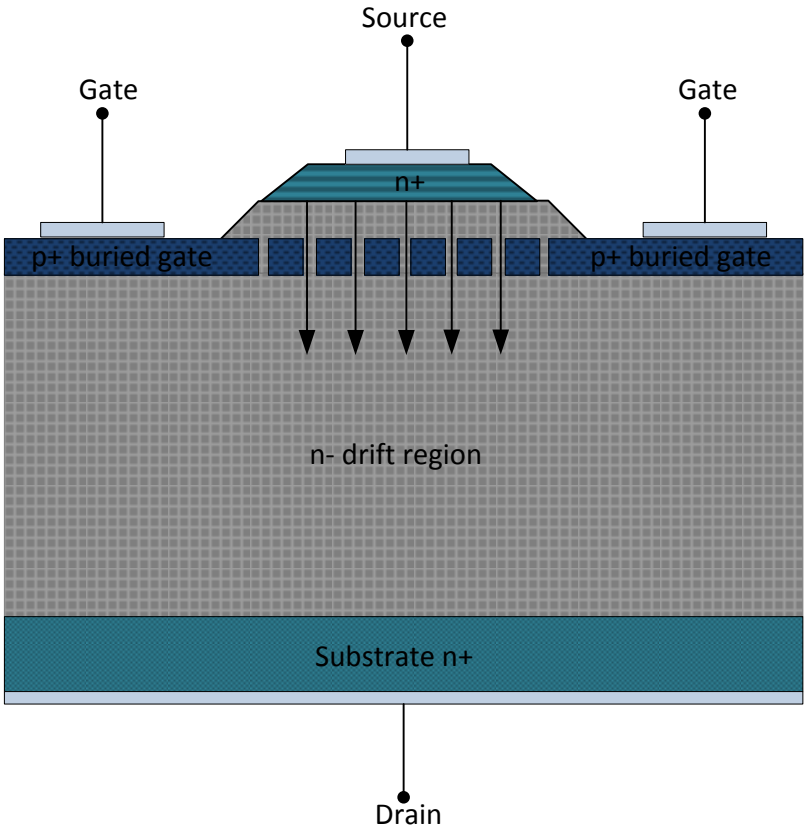

Figure 6. **Cross-section of Buried-grid JFET (BGJFET).**

- ***Double Gate Vertical Trench JFET (DGTJFET)***

A schematic drawing of the DGTJFET structure suggested by DENSO [57] is shown in Figure 7. The DGTJFET offers high current rating capabilities for N-off mode operation. This design combines the advantages of the LCJFET and the BGJFET concepts by using epitaxial regrowth in trenches to define the pitch and the direction of the channel, transforming it from lateral to vertical. The epitaxial channel is grown on the vertical trench walls with the tolerances and the wide design window comparable to the LCJFET. The DGTJFET is basically the same concept as the LCJFET, but allows a dramatic reduction of the cell pitch and of the Miller capacitances due to the vertical channel. The low gate to drain capacitance makes fast switching possible even under dual gate driving conditions, while the small cell pitch and the dual gate control results in very low specific on-resistance. The dual gate drive and the wide design window for the channel optimization give also exceptionally high saturation current levels for N-off designs. In addition, the negative temperature dependence of the saturation current is greatly reduced due to the possibility of using highly doped channels. It has thus the advantages of the BGJFET, but it also can surpass its performance due to the larger design window for the channel doping and width. The use of the integral gate to drain body p-n diode is possible in this concept. It is, however, a matter of trade-off with the possible saturation current density. The disadvantage of this concept is the complex process involving epitaxial regrowth in trenches and planarization techniques.

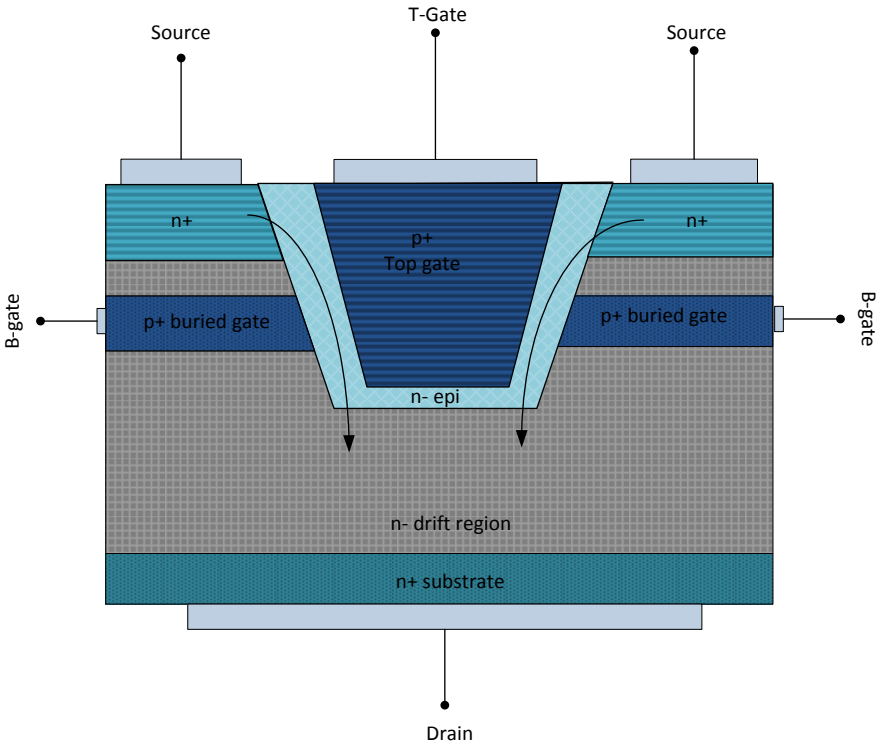

Figure 7. **Cross-section of Double gate vertical channel JFET (DGVTJFET).**

- ***JFET Integral Cascodes***

The prospects of integral JFET/JFET cascodes are discussed. The integral cascode consisting of a high voltage (HV) N-*on* SiC power JFET and a control low voltage (LV) N-*off* JFET is a powerful concept for a N-*off* SiC switch [58]. The main advantage of the cascode solution is the greatly increased speed of switching due to the fact that the buried gate of the high voltage device, which is connected to the source (ground) of the cascode (source of the LV device), shields the low voltage device, which is driven by the control gate [59]. The gate to drain capacitance is thus reduced. In this way the Miller capacitance is being charged by the main circuit and not by the gate circuit. Another advantage is the possibility of utilizing the built-in body p-n diode formed between the buried gate of the high voltage N-*on* device and the drain of the cascode as an anti-parallel diode in the switching applications. Two integral cascode concepts considered for analysis are shown in [*Figure 8*, *Figure 9*]. Both are based on a HV BGJFET controlled in first case by a LV N-*off* recessed gate JFET (RGJFET) [58] and in the second case by a LV N-off BGJFET. It is of interest to analyse the prospects of these integral cascode solutions for power applications. The hybrid cascode is difficult to optimize, which results in degraded on-state and switching performance [60]. In addition, the cascode configuration with a Si MOSFET compromises the high temperature capability of the SiC JFET [61].

The integral cascode concept allows the optimization of the cascode performance and achieves an on-state voltage comparable to the stand alone N-on JFET with equal voltage rating. This is due to several factors. First of all the LV N-off JFET can be made less N-off by shortening the channel. This is facilitated by the electric field shielding effect due to the buried gate of the HV JFET. The limit is set by the highest tolerated value for the leakage current. It is very important to have as high doping in the channel of the LV JFET as possible since the LV N-off JFET determines the current throughput of the whole cascode [51]. Secondly, the HV N-on JFET can be made more conductive by increasing the spacing of the buried gate grid. The limit is set by the electric field crowding at the edges of the buried grid when spacing becomes too large. The grid of the N-on HV JFET section must support the full high voltage. This means the grid spacing has to be chosen so that the premature breakdown due to the enhanced electric field at the grid corners is avoided [51]. As a result the cascode with output pentode characteristics may be controlled by a short channel JFET with triode characteristics. In this case the negative bias appearing on the buried gate of the HV JFET is beneficial in obtaining output characteristics with saturation at high current densities and with high value of the saturation current due to the very low on-state voltage of the optimized LV JFET. This will be further exemplified below using the concept from Figure 8. This is due to the larger field shielding effect and wider grid spacing range available at lower doping concentrations of the drift region [51]. The on-resistance values lower than those of the N-on JFETs are feasible in the voltage range above 1000V [51].

- *Recessed gate JFET controlled cascade*

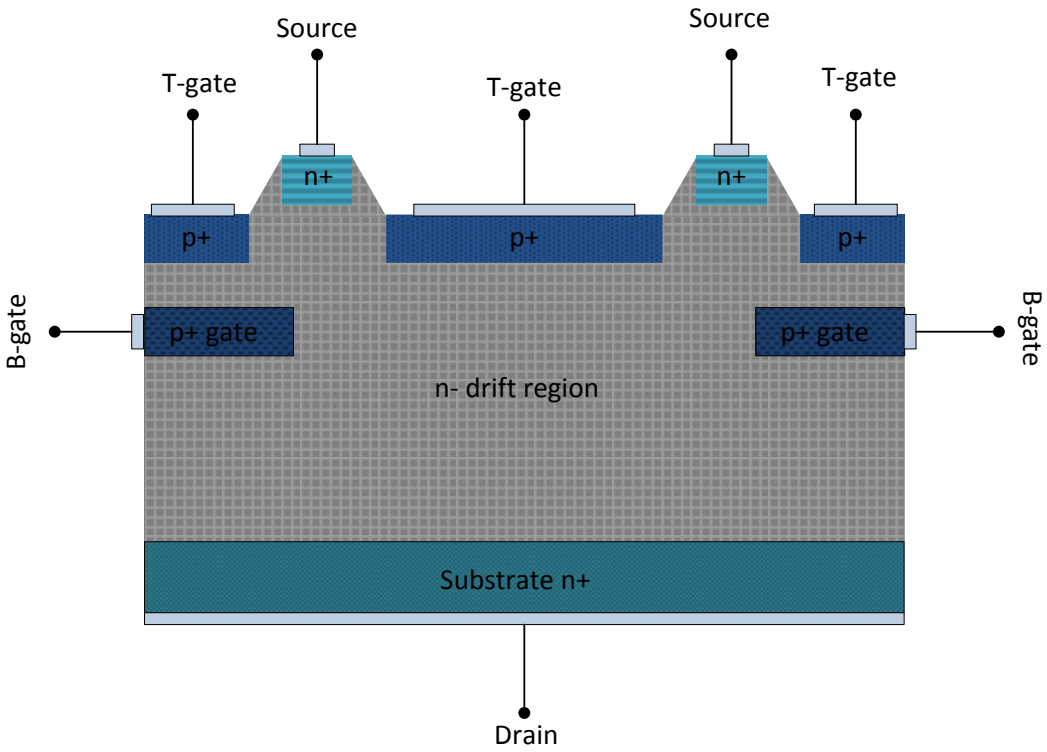

Figure 8. Cross-section of Recessed gate JFET controlled cascode (RGJFET).

- *Buried grid JFET controlled cascade*

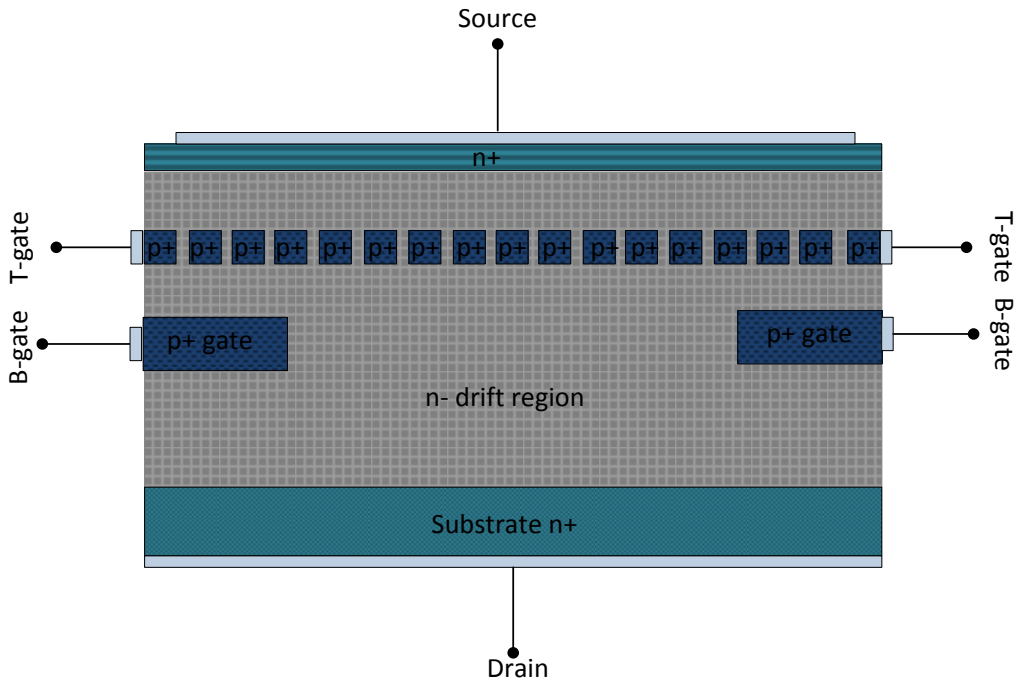

Figure 9. Cross-section of buried grid JFET controlled cascode.

- *SiC JFET – Si MOSFET cascode*

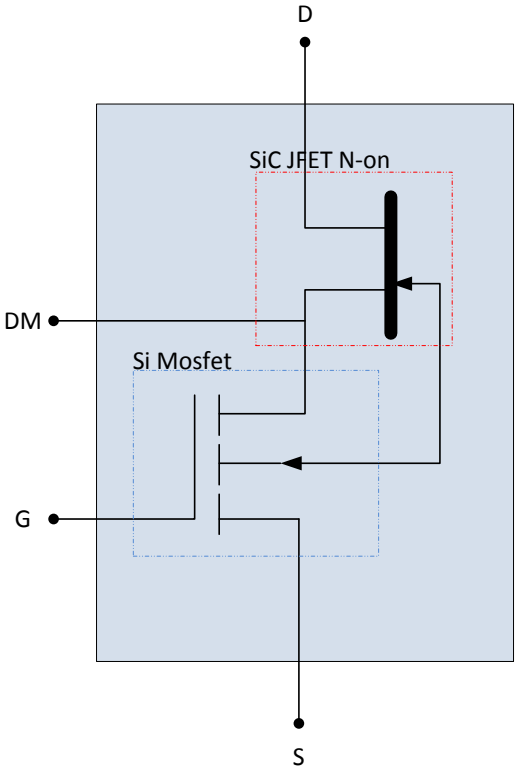

Figure 10. SiC JFET - Si MOSFET cascode design.

After we have presented the characteristics of the different structures that a SiC JFET may be fabricated, we can now do a simple comparison in order to choose the proper type of JFET for the inverter which will be built. Firstly, we exclude from the comparison the JFET integral cascodes as they limit a lot the capabilities of the SiC JFET by increasing the switching losses and the on-state resistance mainly because of the use of an auxiliary device like Si MOSFET or a second SiC JFET. Secondly BGJFET and DGTJFET were not commercially ready by the time of the construction of the inverter, so both of them can't compete with the other two. Furthermore, as was mentioned LCJFET has a larger on-state resistance in comparison with VTJFET and the threshold voltage for the first devices is not the same for all of them and thus it ranges from -16V to -25V which makes it extremely difficult to drive them. As a result an efficient design of a gate driver and a safety system for them would be much more difficult than the VTJFET's ones. Moreover, the presence of a parasitic body diode in LCJFET which may only be used for short time transients because of its big voltage drop and large recovery times is also an obstacle for the proper design of a power electronics application. Consequently, we conclude to the VTJFET which demonstrates lower channel resistances whereas the commercial voltage and current capabilities available in the industry for LCJFET and VTJFET variants are the same. VTJFET also has a very unique characteristic; reverse

current capabilities but not because of a body diode but because of structural reasons which means that the device is symmetrical. These characteristics are examined in the next chapter. Finally we also choose to use a normally-on device because it demonstrates more research interest due to its superior characteristics and because power electronics applications based on normally-on devices are not yet mature and there is a severe lack of knowledge about them. The author also agrees with the opinion of Allebrand and Nee [50] that the discussion about the use of normally-on power devices should be more on the direction of whether we will manage with them to improve the efficiency of our systems and that's the purpose of this thesis.

1.5 Commercial outlook and challenges

WBG materials and devices are rapidly gaining acceptance. By the time of doing this thesis Semisouth stopped providing SiC devices and had just announced its closure. Although the laboratory closed, it is not a sign of failure for SiC technology but it was due to bad economic management from the part of the company. On the contrary, there are more and more new companies opening or expanding their activities to SiC as well as GaN technologies like United SiC, Mitsubishi, STMicroelectronics, etc. [62]

However, a number of manufacturing challenges must be addressed to make WBG materials cost effective in more applications.[66]

- Substrate size and cost: While the quality of GaN and silicon carbide (SiC) wafers is improving, the cost of producing larger-diameter wafers needs to be reduced.
- Device design and cost: Novel device designs that effectively exploit the properties of WBG materials are needed to achieve the voltage and current ratings required in certain applications. Alternative packaging materials or designs are also needed to withstand the high temperatures in WBG devices. Architectures that improve manufacturability and affordability are needed to spur commercialization.
- Systems integration: WBG devices are not always suitable drop-in replacements for Si-based devices. The larger, more complex systems must be redesigned to integrate the WBG devices in ways that deliver unique capabilities.

WBG semiconductors are a foundational technology that promises to transform multiple industries and markets. Low- cost, high-performance power electronics are expected to become integral to everything from household appliances and consumer goods to military systems, vehicles, and a modernized grid that incorporates renewable energy. The WBG share of the global lighting market alone is projected to reach $84 billion by 2020. GaN and

SiC are expected to claim 22% of the $15 billion global market for discrete power electronic components by 2020 in just four industry segments (buildings and industrial, electronics and IT, renewables and grid storage, and transportation) [67]..

A rapidly emerging field that can dramatically accelerate the need for SiC are vehicles with some form of electric propulsion such as hybrid, plug-in hybrid, electric, and fuel cell vehicles. Efficiency, size, and cost are extremely important factors, making SiC devices particularly suitable. These vehicles require the efficiency that SiC can provide and, equally important, they have an operating environment that demands SiC's temperature stability and higher temperature operating capabilities. Cars with SiC SBDs and SiC transistors can potentially eliminate a liquid cooling system to help justify the increased costs of SiC technology. Acceptance in these vehicles will create a high volume demand and push the technology into the mainstream. While EV usage will occur in the future when SiC transistors are more affordable and widely available, having them as a driving force should encourage engineers with other applications to take a closer look at SiC technology [67].

Silicon carbide has a clear place in society today, yet it has only one major commercial application today, which basically is materials or, more specifically, substrates for LED applications [13]. This is perhaps not such a glamorous place to be in the commercial market but it does represent a significant starting point for SiC. The military has had SiC on its radar screen for many years for radar applications, electronic warfare, more electric airplanes, more electric ships, more electric combat vehicles, and rail guns (which, we suppose, are also of the "more electric" variety). These applications require high-quality materials and large wafer sizes. Thanks to the military and its requirements for large wafers of high quality, the commercial SiC sector has started to wake up and aggressively pursue product development to meet these needs.

As far as high-frequency applications are concerned Cree is currently offering MESFET devices geared toward the cellular base station market. It was estimated by Rutberg and Co. that the RF transistor market was $1.9 billion in 2006 [13]. Cell-phone base stations are clearly the biggest market for high-frequency devices. It will not be meaningful to replace all the transistors in a base station with SiC MESFETs or GaN high-electron mobility transistors (HEMTs), but a conservative estimate is that SiC will capture about 20% of this market, which would be approximately $400 million. Unlike SiC, GaN is still not mature for the market.

By far the biggest application for SiC technology is the high-power electronics market. It may not be as glamorous as the high-frequency or the optoelectronic markets but it is big. The current size of the power-device market is $16 billion [65] and it is growing at a rate of almost 10% per year [66]. The question on everyone's mind is how big will the SiC share be? [13]

If we begin substituting the old-fashioned Si devices with fresh new ultra-fast SiC unipolar devices, more than 75% of the power will go through a SiC device. This will be a major deal for the power industry on account of the superior performance of the SiC devices. If we

assume that we improve the efficiency of the Si circuits with another 5%, approximately $50 billion will be saved in power consumption annually as a result [13]. On top of this are additional savings due to the fact that the air-conditioning needed to remove the heat that is no longer generated is dramatically reduced. SMA and RefuSol inverters are today's only inverters with full SiC-JFETs. SMA is using JFET from Infineon [62]. The inverters from SMA have been lighter and have offered an increased efficiency of more than 1%.

Unfortunately, where the power is used is not where the bulk of power devices are sold. Most devices that are sold are for low-voltage (below 300V) and low current applications in markets where SiC is not competitive. In the range between 300–600V, the picture is a little different. Approximately one-third of this market will be accessible for SiC (i.e., $1.32 billion of the Si share). Above 600V, it is estimated that SiC will capture 70% of the market (i.e., $1.68 billion of the Si share Thus, the $3 billion Si share would convert into an approximately $10 billion SiC power-device share when the market is fully developed [62]. A customer will be willing to pay a higher price for the SiC devices because there will be significantly larger savings on the passive components and on the cooling devices due to the higher switching frequency and increased efficiency. Infineon, as well as Cree, has already launched its first power-device products— Schottky diodes. The SiC Schottky diode market alone is estimated to be around $250 million. An interesting observation with respect to SiC Schottky diodes is that the invention of the very fast Si CoolMOS transistor is helping the introduction of the SiC Schottky diode. The power transistors always have a freewheeling diode in antiparallel, however, there has been no diode fast enough to match these fine Si transistors until the introduction of the SiC Schottky diode. In the higher voltage range, SiC transistors as well as Schottky diodes will be important. Specifically, motor drives will be the main application where SiC will become a major player, especially where power conservation is of prime concern; for instance, in the drives to the electric motors for fuel-cell vehicles.

The future will be very interesting and very bright. There is no doubt that the technological issues will be overcome but it will take some time. And finally, since money rules in the ruthless commercial world, will the manufacturing cost of SiC devices be low enough to capture a lion's share or just a niche portion of the market?

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Chapter 2

FORWARD AND REVERSE CHARACTERISTICS OF THE SiC JFET

On this chapter we discuss about the forward and the unique reverse characteristics of the Vertical Trench SiC JFET produced by Semisouth Laboratories. In the beginning we present the structure of this type of semiconductor and compare the basic parameters of the new devices with traditional Silicon semiconductors (MOSFET and IGBT from Fairchild) used until today in the industry. Then we analyse the mechanisms of the forward and reverse conduction for both the Depletion-mode (SJDP120R085) and Enhancement-mode (SJEP120R100) high voltage SiC VT JFETs. Moreover, we introduce the features of the SiC Power Schottky Diode (SDP30S120) and compare them with the reverse characteristics of the VT SiC JFET in order to determine the necessity of an anti-parallel diode in an inverter circuit built in chapter 5. An analytical study is done in which a comparison of the reverse current capabilities between the new SiC transistors, the body diode of a modern MOSFET and the anti-parallel diode of an IGBT is presented. The results indicate that the SiC-JFETs can perform the function of antiparallel diodes with acceptable performance sacrifice for use in power converters. Reverse conduction through the body diode of the MOSFET has been studied in many publications. However for high frequency in bridge configurations, this parasitic effect is no longer useful since its large recovery time presents a risk of destructive latchup of MOSFETs. Finally the methodology of the modelling of these devices in Pspice Model Editor is described and their typical voltage and current waveforms are simulated in order to confirm the coherence of the models with the experimental results and the datasheet plots.

2.1 Basics about the structure of a VT SiC Jfet

Comparing to other types of semiconductors (IGBT, MOSFET, BJT) SiC JFETs are the first stable commercial transistor available in Silicon Carbide technology. Basic operation of the power SiC JFET is modulation of the channel depletion region through the applied gate-source voltage. Threshold voltages can range from negative to positive enabling the

characteristics of both enhancement mode (normally-off) and depletion mode (normally-on) devices.

One commercial type of SiC JFET available in the industry is the vertical trench (VTJFET) which was released in 2008 by Semisouth Laboratories. It can be either Depletion-mode or Enhancement-mode, depending on the thickness of the channel and the doping levels of the structure. VT JFET merges some of the recognizable characteristics of both MOSFETs and BJTs, without the most common negative characteristics of either. Power device semiconductors for higher voltages and power ratings are usually designed as vertical devices. One electrode – mostly the high side connections like the drain or collector – is located at the backside of the power chip. The other electrodes – source and gate – can be found at the front side. Thus, the current flows mostly through a chip from one surface to the opposite one. This offers the possibility of fully exploiting the channel of the semiconductor. Consequently it has great voltage blocking capability and can manage large amounts of current. It does not have a p-n junction between drain-source and therefore has no intrinsic body diode. The SiC-JFET used and compared are SJDP120R085 (DM JFET) and SJEP120R100 (EM JFET) from Semisouth Laboratories. The pinch-off voltage for the normally-on is -7V and for the normally-off +1V.

Conventionally, JFETs have a normally-on behavior due to wider channel structure aimed to increase device current carrying capability. However, controlling the width of vertical channel can result in a normally-off behavior with low threshold voltage.

The basic advantages of the vertical design for the SiC JFET can be summarized in the following points:

- *Low on-resistance*: Low on-resistance of all 1200V-class semiconductor devices due to the fact that SiC material enables reduced conduction losses and higher system efficiencies.

- *No saturation voltage*: Due to unipolar conduction in the JFET structure there is not a saturation voltage to overcome before output current is available, enabling lower conduction losses and higher systems efficiencies.

- *No tail-current*: No tail current is present at the turn-off transition enabling lower switching losses and higher practical switching frequencies.

- *Low Intrinsic Capacitance*: Lower device capacitances allow for reduced gate charge requirements and high-frequency switching applications.

- *No Body Diode*: There is no intrinsic body diode in the JFET structure.

- *Positive Temperature Coefficient*: Allows multiple die to be paralleled easily without concerns for unbalanced current sharing or thermal runaway.

- *Reverse Conduction*: Despite the absence of a traditional body diode, the SiC JFET are shown able to be used in a forward and reverse conduction.

A cross section drawing of the trench JFET structure and a simplified electrical equivalent circuit schematic is shown in Figure 11 and Figure 12 respectively. The 4H-SiC VJFETs reported here were fabricated on n+ substrates with epitaxially grown n-type drift and channel layers. Trenches were dry etched and implanted with Al to form the p-type gates. The trenches were filled with oxide followed by the formation of ohmic contacts and contact pads. After dicing, the devices were mounted TO257 packages for testing before they will be released in the market.

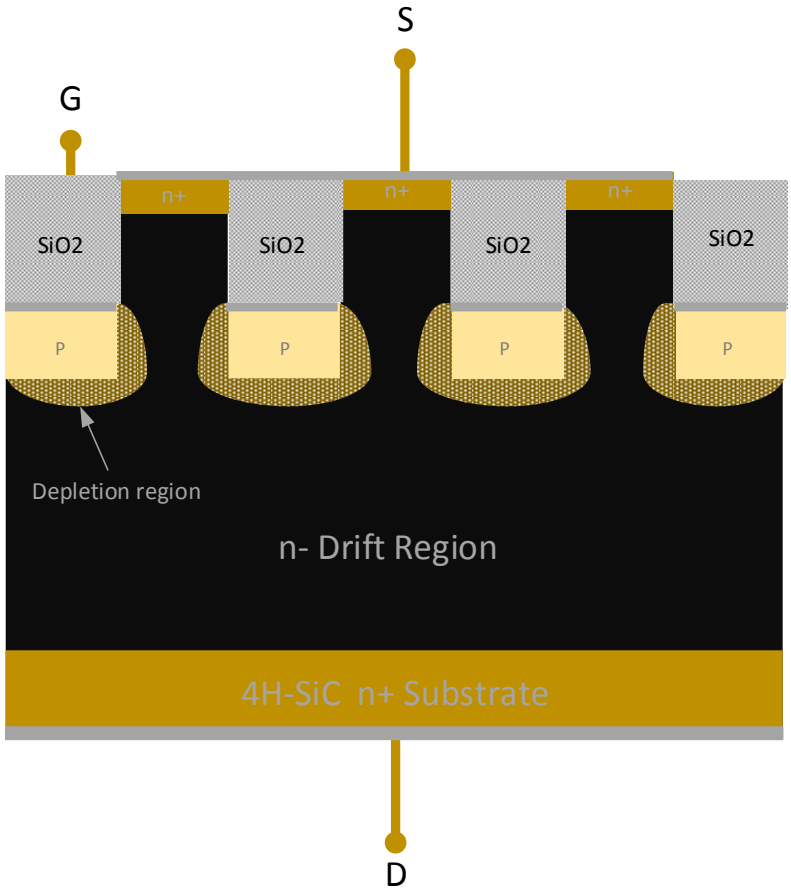


Figure 11. Cross Section of the Vertical Trench SiC JFET.

By investigating the device structure a number of parasitic elements could be pointed out. P-N diode are formed between the gate-source (D_{GS}) and gate-drain region (D_{GD}). These diodes play an important role in device performance as by controlling their voltages it is managed to shape the channel either by applying directly a voltage in the case of D_{GS} or by changing the voltage in D_{GD} indirectly through V_{GS} and V_{DS}. By forward biasing them, the depletion region that blocks the conductive channel shrinks allowing the current to start conducting. Avoiding excessive current flowing through D_{GS} is one of the basic driving requirements for VTJFETs. It remains in reverse biased (or slightly biased with very small forward current in the case of the forward bias as we will see in chapter 3) during normal operation as source potential is higher than gate potential. Parasitic capacitances C_{GS} C_{GD} and C_{DS} appear between gate source and gate-drain terminals, respectively. These three capacitances define the

switching behavior of the element while they act as non-linear, voltage-dependent capacitances in the circuit. Notice that C_{DS} is negligible compared with the other two capacitances. Gate-drain capacitance (C_{GD}) is referred as Miller capacitance in literature and plays vital role in device performance, specifically during switching. This role is more prominent at high frequency switching.

Moreover, the resistances in the contacts of the source, drain and gate of the JFET are modelled as three linear resistors R_G, R_D, R_S whereas L_S, L_D, L_G are the unavoidable parasitic inductances due to the packaging. The current source represents the current flow of the JFET during the conductance of the device.

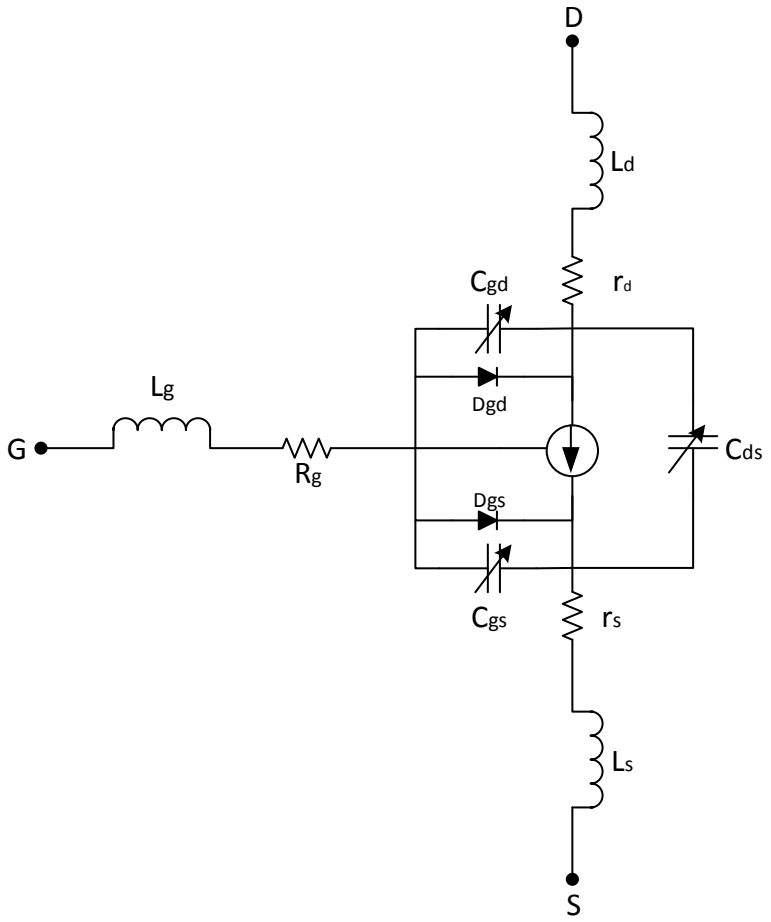


Figure 12.Electrical equivalent circuit for VT SiC Jfet.

There is neither structural nor electrical difference between normally-on and normally-off JFET. This JFET property is determined only by the width of the channel region and its doping concentration. Depending on the desired device characteristics, these two parameters can be designed in such a way, so channel is fully depleted (normally-off) or partially depleted (normally-on) under zero gate bias condition.

The function of the VT JFET can be distinguished in two stages as depicted in Figure 13. Quadrant I describes the forward characteristic of the VT SiC JFET whereas the third one defines the reverse behavior of the device.

The first part of the figure in both quadrants, which is called triode (or linear), determines the typical function of the device during the forward or the reverse conduction. On this region the power losses of the device are acceptable as long as the values of V_{DS} remain in low levels. The slope of the plots on the linear region defines the "on"-resistance. As this slope is increasing by the growing of V_{DS}, the plots reach to a knee where we have the saturation voltage, $V_{DS,sat}$.

The limit between the triode and saturation region is the current I_{DSS} which is defined by the manufacturers. In the saturation part the current is growing slowly as it has reached its limit while V_{ds} is getting large values. As the drain-source voltage is rising the drain-gate junction is depleted since $V_{GD} = V_{GS} + V_{SD} = V_{GS} - V_{DS} \overset{V_{DS}\uparrow}{\Longrightarrow} V_{GD} \leq V_p$.

On the other hand for the reverse conduction the controlling voltage becomes V_{GD} and this value determines in which region we operate the device. As it is evident from the Figure 13 the saturation current in the third quadrant is significantly smaller than the first one which denotes the limited capability of the channel to conduct reverse current. We will explain why this happens in the next sections of the chapter.

In any case it is shown that the larger the applied voltage in the gate-source junction (forward conduction) or gate-drain voltage (reverse conduction), the larger is the point in which the current is saturated.

Consequently we can extract the following equations.

$$I_D = \begin{cases} 0, \quad (1) & , V_{GS} \leq V_p \; and \; V_{GD} \leq V_p \\ I_{DSS} \cdot \left[2 \cdot \left(1 - \frac{V_{GS}}{V_p} \right) \left(\frac{V_{DS}}{-V_p} \right) - \left(\frac{V_{DS}}{V_p} \right)^2 \right] \; (2) & , V_{DS} \leq V_{GS} - V_p \\ I_{DSS} \cdot (1 + \lambda V_{DS}) \cdot \left(1 - \frac{V_{GS}}{V_p} \right)^2 \; (3) & , 0 \leq V_{GS} - V_p \leq V_{DS} \\ I_{DSS\_r} \cdot \left[2 \cdot \left(1 - \frac{V_{GD}}{V_p} \right) \left(\frac{V_{DS}}{V_p} \right) - \left(\frac{V_{DS}}{V_p} \right)^2 \right] \quad (4) & , V_{DS} \leq V_{GD} - V_p \\ I_{DSS\_r} \cdot (1 - \lambda_r V_{DS}) \cdot \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad (5), & 0 \leq V_{GD} - V_p \leq V_{DS} \end{cases}$$

Equation (2) and (4) refer to the linear region while (3) and (5) to the saturation region during the forward and the reverse conduction respectively. I_{SDD}, I_{SDD_r} are the saturation currents and λ ,λ_r are the channel-length modulation parameters and are equal to the slope of the current waveform at saturation in forward and reverse region. Equation (1) describes the behavior of the channel while it is fully depleted due to the threshold voltage applied to the gate-source junction which leads also to the closure of the gate-drain contact. On this point it is noted that the breakdown voltage of the device (D_{gs}) is below -15V at temperatures until 150^{o}C which means that we must not apply to the gate-source junction voltages below this level otherwise we will lead our device to destruction due to the excessive currents that will pass through the channel.

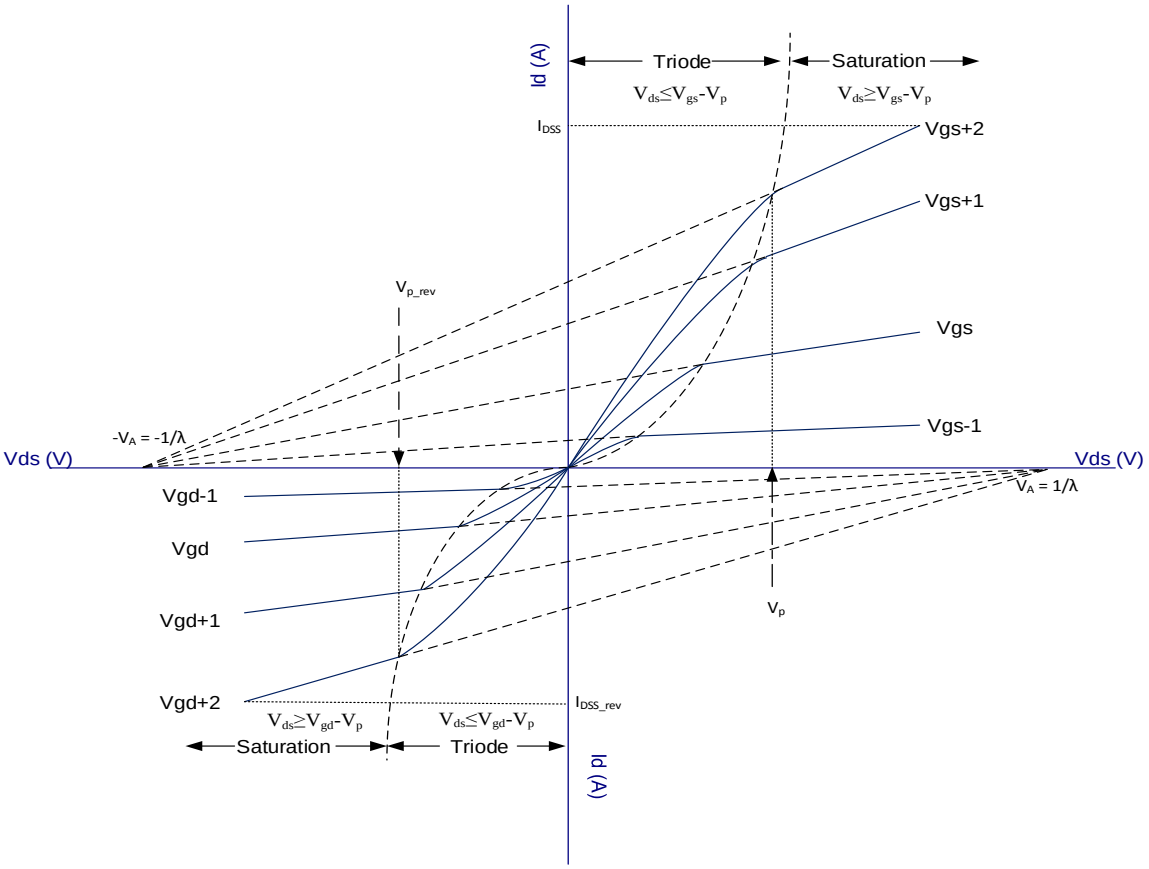


Figure 13. Typical voltage characteristics of a SiC VT JFET in I and III quadrant operation.

Another advantage of the vertical design is that one can shift the threshold voltage negative or positive by widening or narrowing the nominal source finger width. Some of these devices were designed to have a negative threshold voltage and therefore be normally-on at zero source-gate bias while others were designed to have a small negative or slightly positive. In general, the more "on" a JFET is, the lower the specific on resistance. However, the more negative threshold voltage, the more gate bias required to pinch the drain current off, especially at high drain voltages. Normally-off JFETs typically require very small negative gate biases to block the rated maximum voltage, but usually suffer from much lower saturation current than normally-on devices. These remarks are noted in the next table where it is evident that the on-resistance is larger for the normally-off device while the maximum drain current that it can give is significantly smaller (10 A).

In the table below, you can find a first comparison between the two types of VT SiC JFET produced by Semisouth and two other usually used Silicon semiconductors (600V N-Channel MOSFET → FQPF12N60C and 1200V NPT IGBT→ FGA25N120) with the most important parameters of the devices according to their datasheets. The packaging of the IGBT also include an antiparallel diode.

	SJDP120R085	SJEP120R100	600V MOSFET	1200V IGBT
Blocking Voltage, BV_{DS} (V)	1200	1200	600	1200
Drain Current I_D (A) (25°C)	27	17	12	50
Drain Current I_D (A) (100°C)	17	10	7.4	25
Gate-Source Voltage (V)	±15	±15	±30	±20
Threshold Voltage (V), V_p	-7	1	4	7.5
Die Size (mm^2)	315	315	100	320
$R_{DS(on),max}$ (mΩ)	85	100	650	-
Input Capacitance (V_{DD}=100V)(pF), Ciss	255	800	2290	3700
Output Capacitance (pF)(V_{DD}=100V), Coss	80	95	235	130
Reverse Transfer Capacitance (V_{DD}=100V), Crss	80	89	28	80
Drain Leakage Current, $I_{DSS,typical}$ (μA) (25°C)	10	100	-	-
Drain Leakage Current, $I_{DSS,typical}$ (μA) (100°C)	100	300	10	-
Gate Forward Current,I_{GFWD} (mA)	0.04 (V_{gs}=2V)	300 (V_{gs}=3V)	0 (very small)	0 (very small)
Total Gate Charge (nC), Q_g	32 (V_{DS}=600V)	71 (V_{DS}=800V)	63 (V_{DS}=400V)	200
$E_{TS,typical}$ (μJ)	290	121	-	5800
$E_{on,\ typical}$ (μJ)	160	90	-	4300
$E_{off,\ typical}$ (μJ)	130	47	-	1500

Operating Temperature	-55°C – 150°C	55°C – 150°C	55°C – 150°C	55°C – 150°C
Price ($)	27 (September 2012)	24 (September 2012)	2.5	4.5

Table 1. Comparison of the two SiC JFETs (EM and DM) produced by Semisouth and classic Silicon devices.

The EM JFETs have the advantage of safe, normally-off operation, low R_{DSON}, and switching energies which are five to ten times lower than that of comparable rated Si IGBT's. The DM JFETs, with the same die size, have to be protected for fail-safe operation, but have twice the saturation current, 15% lower R_{DSON} at room temperature, and switching energies which are comparable than the EM JFET's. The same gate drive concept can be employed with both, but no on-state current (I_{GFWD}) is required for the DM JFETs. It is also shown that the typical characteristics of the devices are affected by the temperature (there is a great difference in some values depending the temperature 25°C, 150 °C). Operating these devices at elevated temperatures result in an expected reduction of forward current which was investigated in [10] by Semisouth (but for a previous model of VT SiC JFET). According to it, with sufficient gate voltage to turn the device on, the drain current for a fixed DC drain voltage exhibited an exponential decrease for temperatures from 25° to 250°C. The devices were limited to 250°C during Semisouth's measurements to avoid melting the backside die-attach.

On the other hand, apart from the high current that the specific Si IGBT can conduct and its low price comparing to its capabilities, there is no other obvious advantage of the Si semiconductors comparing the SiC JFET. The parasitic capacitances are much larger in Si MOSFET and Si IGBT which result in high switching energy losses. Also the required voltages for the gate driving are smaller for the SiC JFETs which lead in lower power gate driving requirements. The high price of the SiC JFET can be explained by the immaturity of the technology while it is expected to be dropped in the upcoming years.

Consequently, both the SiC JFETs can lead in converter applications with significantly improved power efficiencies. In the following figures, the advantages of the proposed devices are also shown graphically.

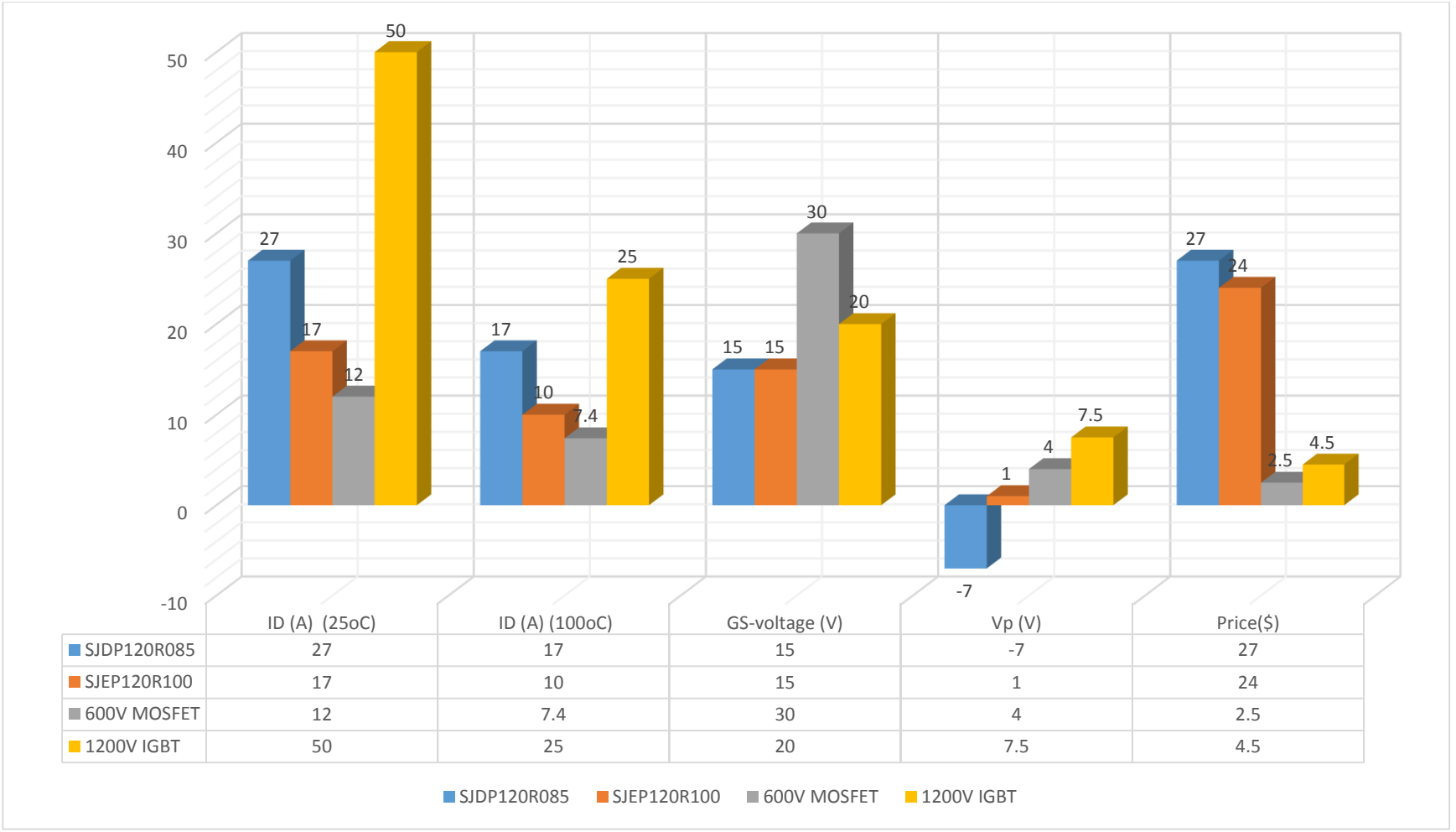
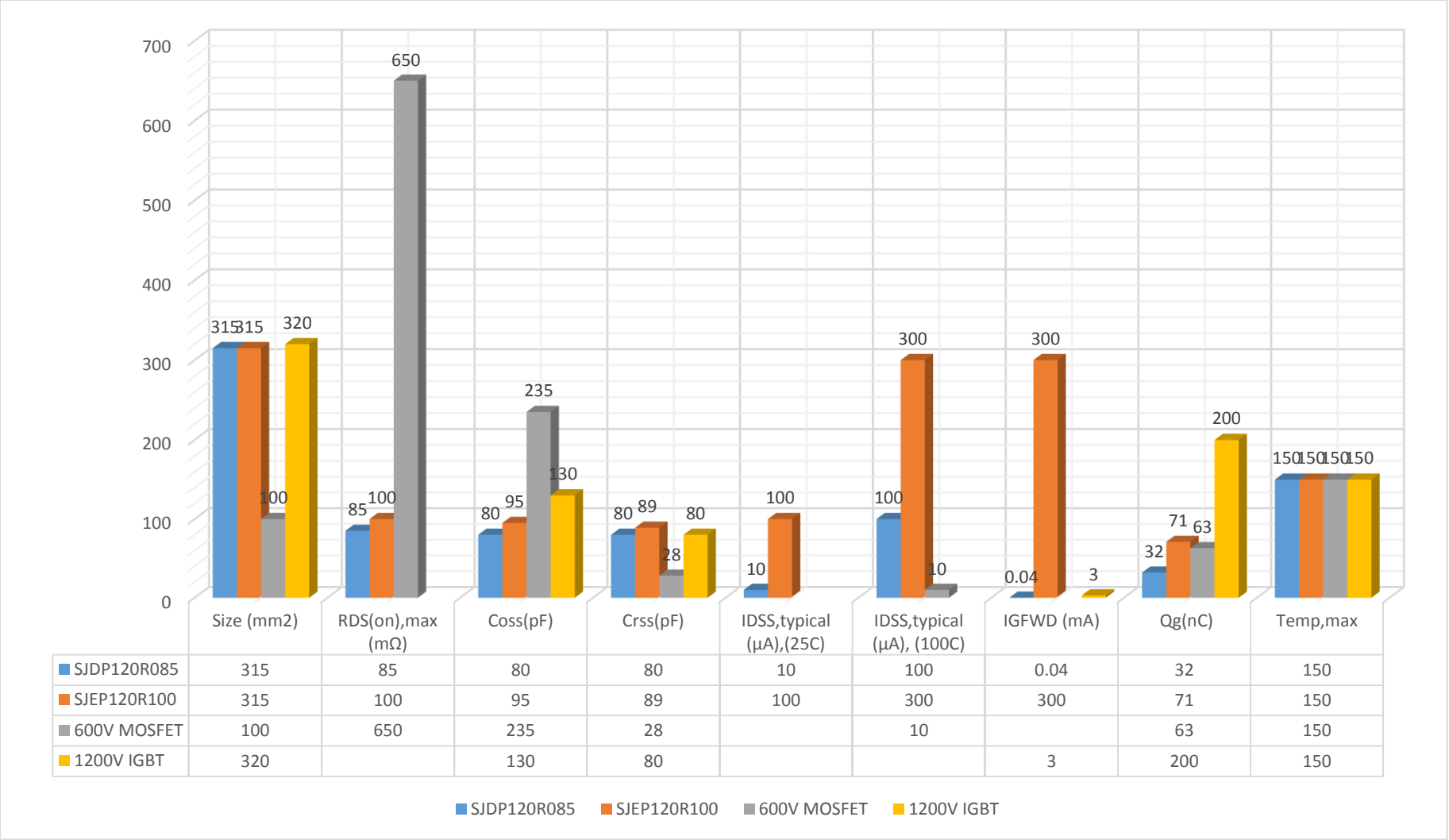


Figure 14. Graphical comparison of the two types of VT SiC JFET (SJDP120R085, SJEP120R100), 600V Si MOSFET (FQPF12N60C) and 1200V Si IGBT (FGA25N120).

Figure 15. Graphical comparison of the two types of VT SiC JFET (SJDP120R085, SJEP120R100), 600V Si MOSFET (FQPF12N60C) and 1200V Si IGBT (FGA25N120).



	Size (mm2)	RDS(on),max (mΩ)	Coss(pF)	Crss(pF)	IDSS,typical (μA),(25C)	IDSS,typical (μA), (100C)	IGFWD (mA)	Qg(nC)	Temp,max
SJDP120R085	315	85	80	80	10	100	0.04	32	150
SJEP120R100	315	100	95	89	100	300	300	71	150
600V MOSFET	100	650	235	28		10		63	150
1200V IGBT	320		130	80			3	200	150

Figure 16. Graphical comparison of the two types of VT SiC JFET (SJDP120R085, SJEP120R100), 600V Si MOSFET (FQPF12N60C) and 1200V Si IGBT (FGA25N120).

2.2 Forward Conduction

2.2.1 *Linear region*

In this operation the JFET works like a simple resistor which value is controlled by the applied voltage in V_{GS}. Depending on this value, the depletion layers penetrates in the channel more or less which leads in the changing of the value of the conduction resistance and in greater or smaller drain current capabilities [Figure 20, Figure 21]. From the figures the value of the on-resistance is found 85mΩ (DM) and 100mΩ (EM) by calculating the slope of the output characteristics.

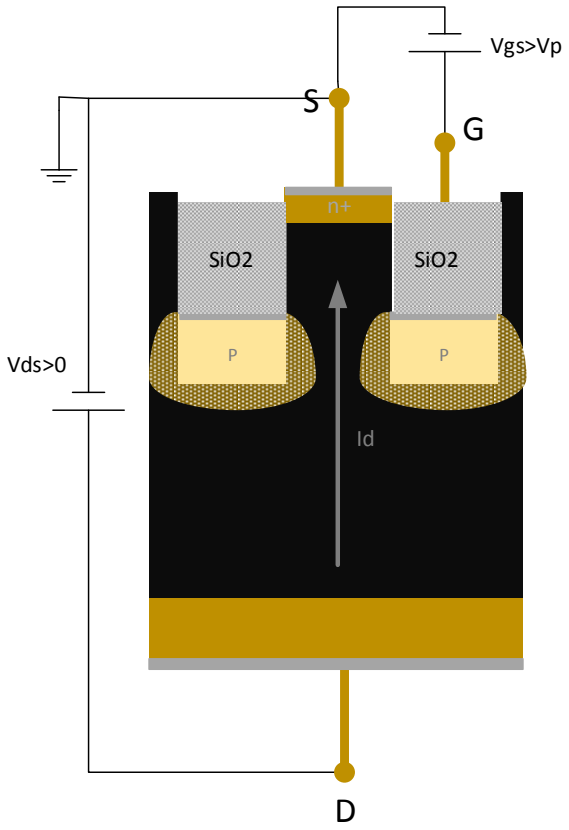


Figure 17. Graphical representation for forward conduction, triode region.

When the value of V_{GS} is greater than V_p by applying a voltage between the drain and the source junction, there will be a current flowing through the channel. For the normally-on device it should $V_{GS} > -7$ and for the normally-off $V_{GS} > 1$. It is noted that the DM JFET can conduct for zero gate voltage. As V_{DS} is growing so does I_D and as long as V_{DS} remains low the channel is not depleted in the drain side and we can conduct larger levels of current.

The most significant voltage drop is noticed around the depletion regions in the point where the channel is becoming narrower which results in high values of resistances. So growing the V_{DS} the depletion layer in the drain part is entering gradually more and more into the channel which leads to significant voltage drop. Consequently the drain current stops growing in a linear way with V_{DS}.

For this region $V_{GS} > V_p$ and since we consider small values for V_{DS}, it results that

$$V_{DS} \leq V_{GS} - V_p \Leftrightarrow V_{GD} > V_p \quad (6)$$

So the drain current increases linearly

$$I_D = I_{DSS} \cdot \left[2 \cdot \left(1 - \frac{V_{GS}}{V_p} \right) \left(\frac{V_{DS}}{-V_p} \right) - \left(\frac{V_{DS}}{V_p} \right)^2 \right] \quad (7)$$

2.2.2 *Saturation region*

As V_{DS} continues to grow, the depletion region extends into the channel until the point when it is saturated in the drain side [Figure 18]. This results to inability of further current increasing. In this case we have a saturation current while V_{DS} is taking larger values comparing to before.

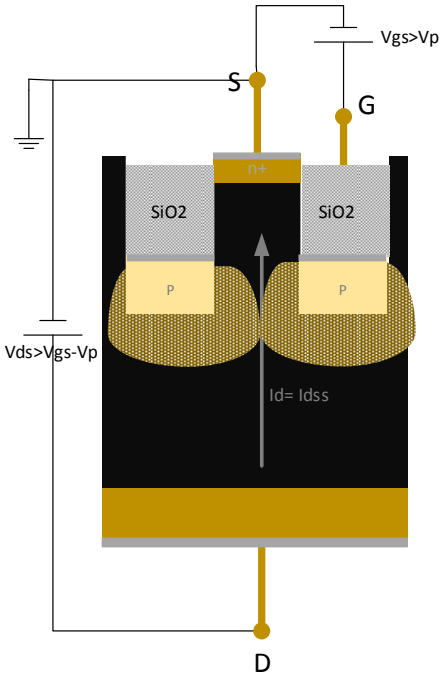


Figure 18. Graphical representation for forward conduction, saturation region.

This happens because

$$V_{DS} > V_{GS} - V_p \Leftrightarrow V_{GD} < V_p \qquad (8)$$

The voltage V_p is called pinch-off voltage. The drain current in the saturation region grows according to the equation:

$$I_D = I_{DSS} \cdot (1 + \lambda V_{DS}) \cdot \left(1 - \frac{V_{GS}}{V_p}\right)^2 \qquad (9)$$

In the next figures the experimental DC characteristics of the Depletion and Enhancement mode for the forward conduction are depicted. The test circuit in order to extract these plots we used was the following [Figure 19]. For each different V_{GS}, we change the value of V_{DS} and take values for various drain current and so we made the plots in Figure 20, Figure 21.

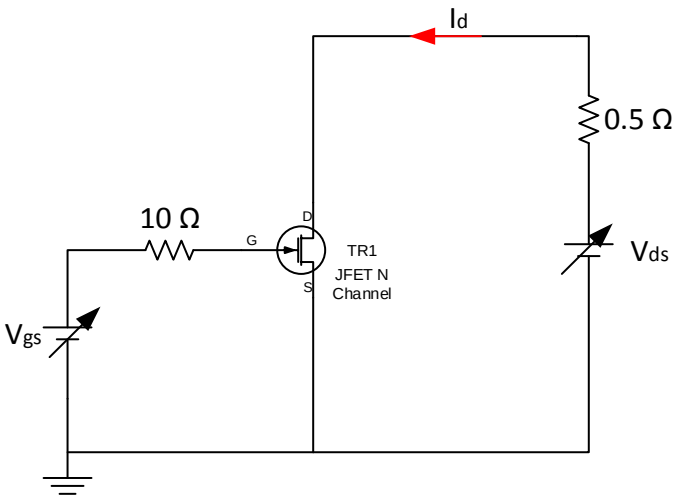


Figure 19.Test circuit for DC characteristics.

For both devices it is shown that it is an advantage to have large gate-source values (V_{GS} >0) as the saturation current is greater and V_{DS} is smaller for the same magnitude of current which results to lower power losses. The limit for how large V_{GS} we can apply in each device is matter of gate driving and it will be discussed in the next chapter.

The current capability is significantly larger for the normally-on device with a maximum of 47 A whereas the normally-off can withstand up to 37 A. The saturation region for DM was found in greater V_{DS} comparing to the EM which is translated to less conduction losses for the same current requirements.

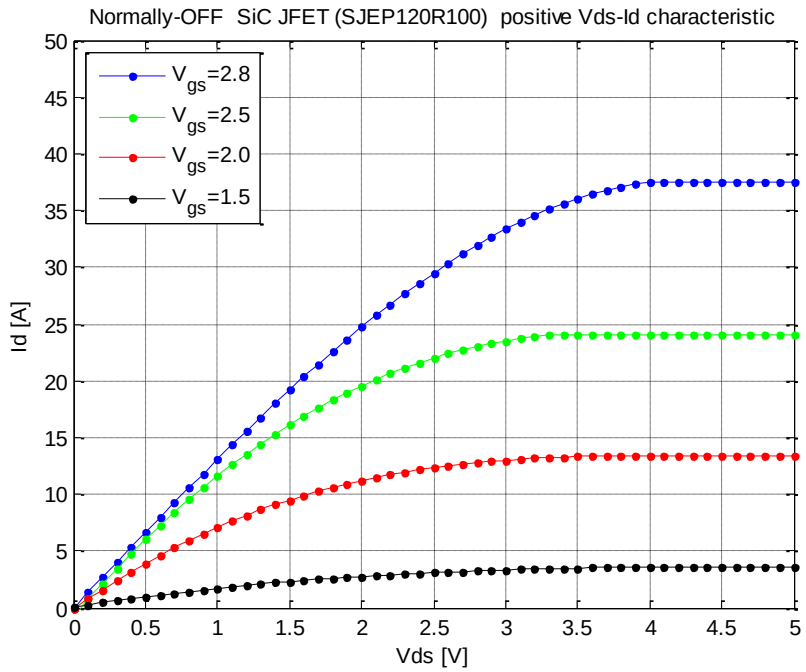


Figure 20.DC forward characteristics for EM SJEP120R100

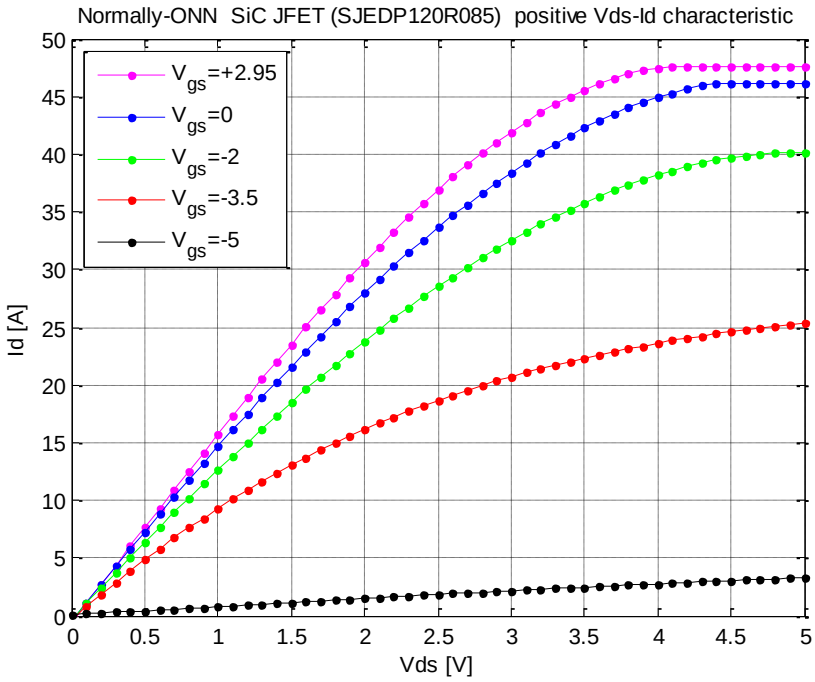


Figure 21. DC forward characteristics for DM SJDP120R085

2.3 Blocking operation

To achieve this operation the channel must be completely depleted in both contacts (Gate-Source and Gate-Drain) of the SiC JFET. By applying V_{GS} = -15V the channel is pinched-off and no current can pass through it. The rated blocking capability of our devices is 1200V.

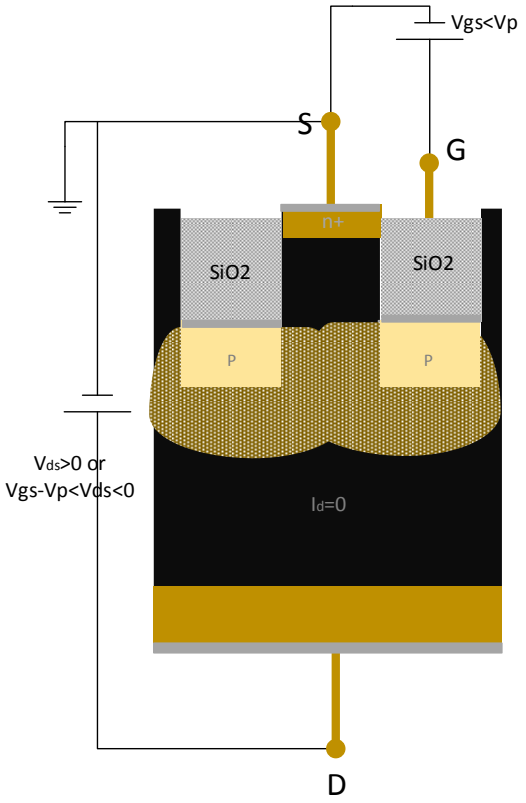


Figure 22. Graphical representation for the blocking operation

As long as the device is working properly which means that there is no fault in our power system the device remains in blocking state. But if V_{DS} begins to increase rapidly there is the danger of the opening of the gate-drain junction which leads to current flow through the channel. This will happen if

$$V_{GD} > V_p \Leftrightarrow V_{DS} < V_{GS} - V_p \qquad (10)$$

$$Normally-on: \qquad V_{DS} < -8 \qquad (11)$$

$$Normally-off: \qquad V_{DS} < -16 \qquad (12)$$

From the above equation it is evident that as long as $V_{DS} > 0$, V_{GD} will never be greater than the pinch off voltage. But in the case of applying negative voltage $V_{DS} < 0$ if it will take large

values, the channel will have the ability to conduct current. More details in the case that the reverse conduction is desirable and when it is achieved are given in the next section.

2.4 Reverse Conduction

From various documents it has been shown that the structure and performance of the SiC Vertical trench JFET is advantageous in operational modes where traditional high voltage MOSFET or IGBTs require the use of an external freewheeling diode. The manufacturers provides little specific information regarding the nature of the SiC JFET's reverse conduction characteristics on the datasheets and only recently there are references by Semisouth confirming this operation [4].

On this section we will focus on the reverse conduction of vertical-channel SiC-JFET and the possibility of eliminating the external antiparallel diodes in the power electronics applications. Firstly we introduce the mechanisms and the characteristics of the semiconductor during its operation on the third quadrant and then we evaluate the usefulness of this feature.

The VT SiC JFET is a symmetric device as can be seen by the cross section of the device [Figure 11] which means that it can conduct and block current in both directions. In order to investigate the reverse conduction capabilities of the SiC-JFET we apply a gate-drain voltage and a negative drain-source voltage according to Figure 23. By this experiment and the following plots we confirm the reverse properties of the semiconductor.

On this point it is noted that the DC characteristics of the diode D_{GD} are the same as D_{GS} and so the gate driving requirements apply here in the same way [*Figure 24*].

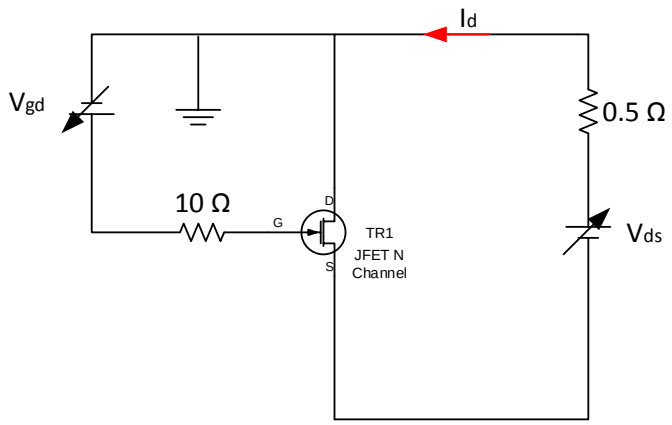


Figure 23.Circuit for DC characteristics during reverse operation.

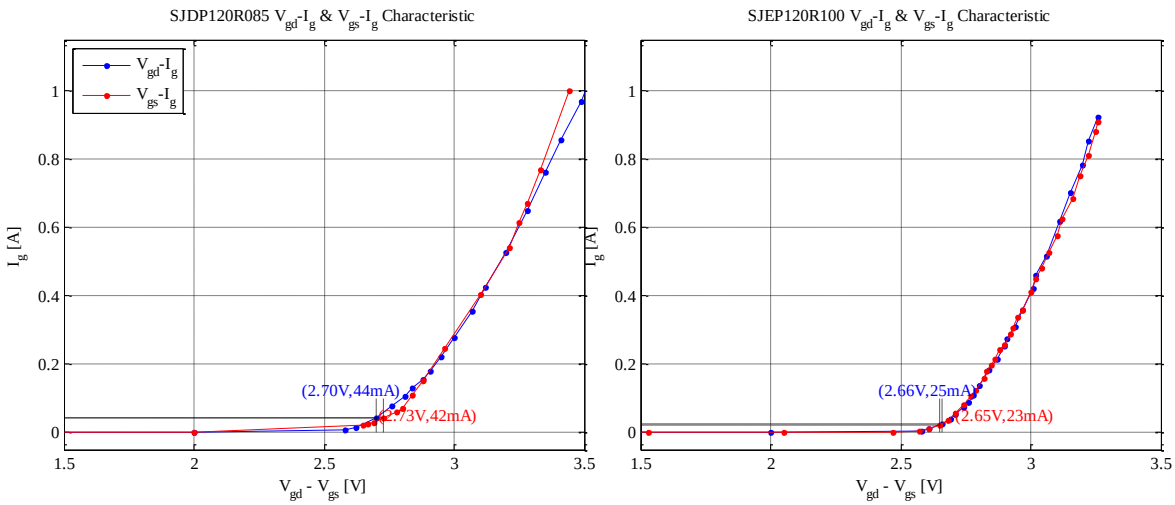


Figure 24. DC characteristics of D_{gs} and D_{gd} for DM and EM mode JFET necessary for the gate driving of V_{gs} and V_{gd}.

2.4.1 *Linear region*

As we have mentioned for various gate-drain voltages we extract the I-V plots for different V_{DS} values. Due to the symmetry of the device the same results as for the forward conduction apply here.

Like in the linear region in the first quadrant, by changing the gate-drain voltage we determine the penetration of the depletion layer in the channel which affects the value of the resistance and the volume of the saturation current.

On this region the current is growing linearly and the slope of the plot defines the reverse resistance which appears to be 95mΩ for DM and 110mΩ for EM. Since the applied gate drain voltage is greater than the threshold one (-7 for normally-on and +1 for normally-off) and the drain-source takes very small values, the following equations are satisfied.

$$V_{GD} > V_p \qquad (13)$$

$$V_{DS} \leq V_{GD} - V_p \Leftrightarrow V_{GS} > V_p \qquad (14)$$

$$I_D = I_{DSS\_r} \cdot \left[2 \cdot \left(1 - \frac{V_{GD}}{V_p} \right) \left(\frac{V_{DS}}{V_p} \right) - \left(\frac{V_{DS}}{V_p} \right)^2 \right] \qquad (15)$$

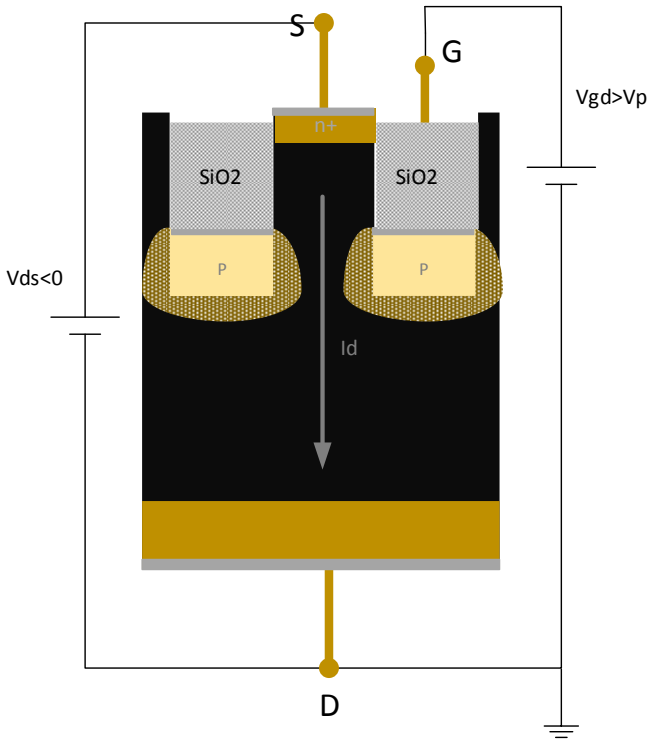


Figure 25. Graphical representation for reverse conduction in linear region.

2.4.2 *Saturation region*

While the drain-source voltage is increasing the equation (14) is not satisfied anymore and the gate-source diode is depleted. Therefore the current is saturated and we can conduct no longer larger currents. The voltage on which we have the "knee" on our plot is the reverse saturation voltage $V_{DS,sat,rev}$.

$$V_{GD} > V_p \qquad (16)$$

$$V_{DS} > V_{GD} - V_p \Leftrightarrow V_{GS} < V_p \qquad (17)$$

$$I_D = I_{DSS\_r} \cdot (1 + \lambda V_{DS}) \cdot \left(1 - \frac{V_{GD}}{V_p}\right)^2 \qquad (18)$$

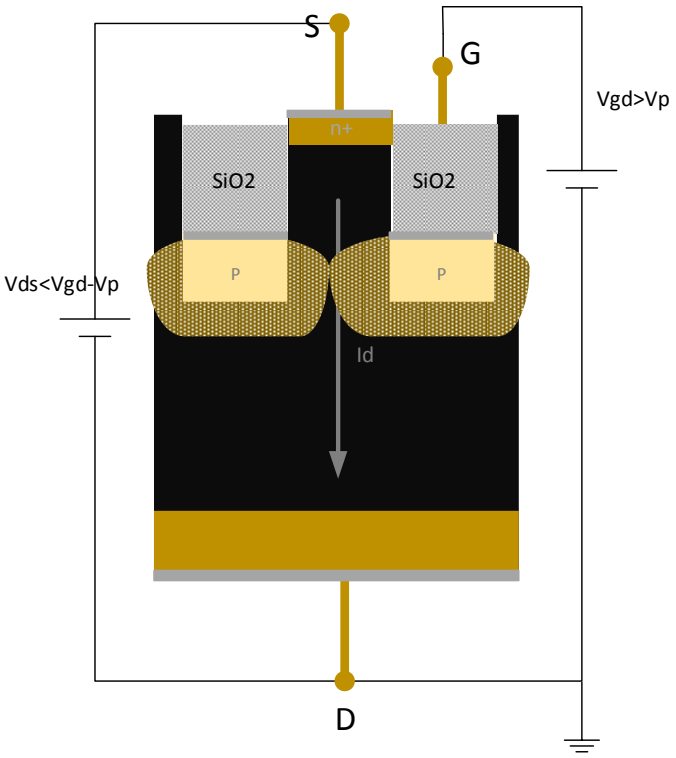


Figure 26. Graphical representation of reverse conduction during saturation.

Drain current saturates with increased source bias, as a higher reverse bias across the GS P–N junction close to source side causes a wider depletion region. This is reflected clearly in Figure 26 : pinch-off happens in the channel close to source side when current is increased and depletion region extends across the channel gradually.

On the next plots we present our results for the reverse drain current as a function of drain-source voltage for various gate-drain voltages [Figure 27, Figure 28].

To begin with it is shown that normally-off maximum saturation current (17A) is significant smaller than the one on the forward conduction (37 A). In the case of the DM JFET the difference is not so big (44A instead of 47A). Moreover, the saturation voltage is smaller for both devices comparing to before which leads to higher power losses during reverse operation. Finally, the channel resistance extracted from the slope of the waveforms has approximately the same values with the forward conduction (the maximum difference for both devices is about 13%).

On this paragraph we described the current capabilities for the VT SiC JFET and confirmed that it can conduct reverse current due to its symmetric design. On the next section we are referring to real applications that these results can be applied.

Our analysis so far was based on the control of the gate-drain voltage but in reality we are changing only the gate-source one. So it will be shown how these plots can be used and what losses we pay by not placing a freewheeling diode.

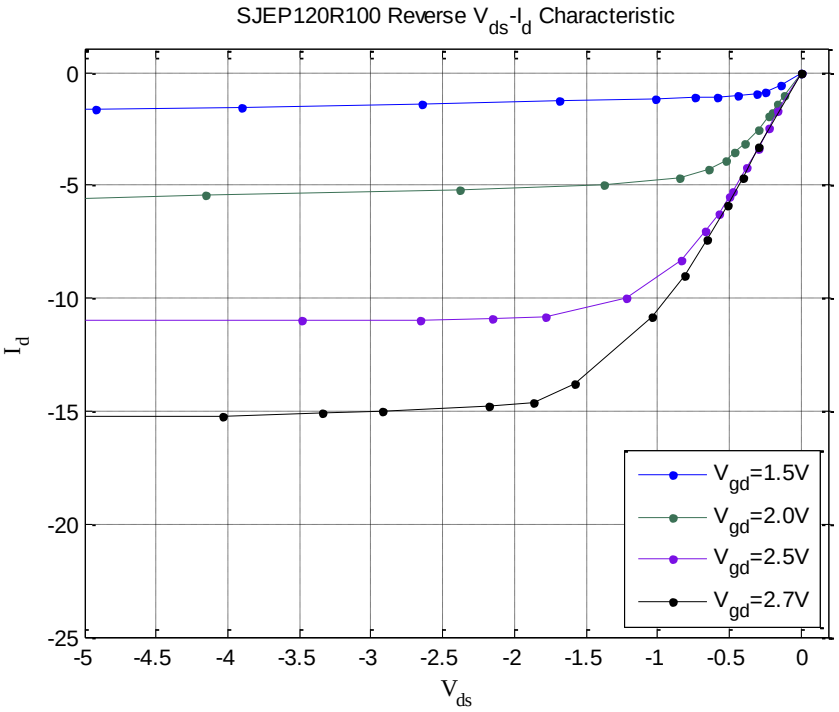


Figure 27. Reverse current capability for normally-off.

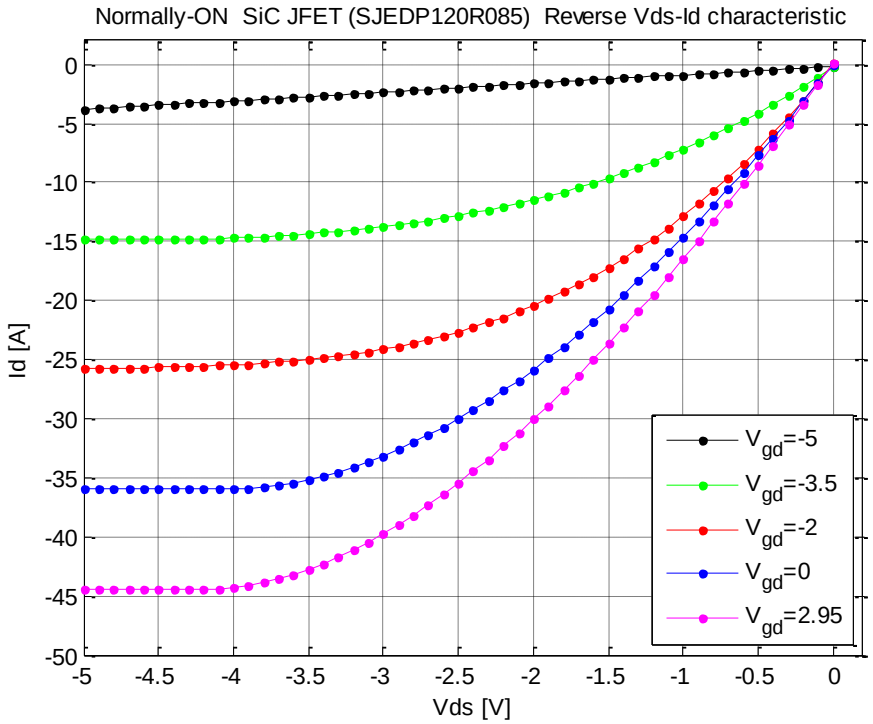


Figure 28. Reverse current capability for normally-on.

2.5 Comparison and application in real circuits

The SiC JFET is able to conduct reverse if the channel is not depleted in either the gate-drain or gate-source side. This means that as long as both sides are open the drain current increases linearly. When one region is depleted, we reach to the limit of the saturation current.

If we apply gate-source voltages larger than the threshold ones the channel is free and there is a current flow. The more positive gate-drain voltage we apply in the interval $V_T<V_{GS}<3V$ the less conduction resistance we have and hence less voltage drop [Figure 29, Figure 30]. Theoretically the reverse conduction I-V curves do not saturate like forward characteristics since with the increase of $V_{SD}>0$ the channel is never pinched-off ($V_{GS} > V_T$ and $V_{GD} = V_{GS}+V_{SD}> V_T$). As a result, when V_{GS} is higher than the channel threshold voltage, the channel is never "pinched-off" with the increase of V_{SD}. When V_{GS} is less than V_{TH}, the channel is always "pinched-off" at its source end but its drain end opens up as V_{SD} increases [equation 10, 11, 12].

Consequently, as the current conduction is in reverse direction, V_{GD} is increasing and channel close to drain side always opens up wider. As a result, Figure 29 and Figure 30 show that the JFET reverse conduction $I - V$ curves look just like a diode. It is hence possible to use this JFET for freewheeling purpose despite the fact that no parasitic diode is contained from source to drain.

In contrast to what we expected we reach to a saturation point for the current which is due to the *parasitic gate-to-drain diode*. When the source-drain voltage is increased so that the gate-drain voltage equals to the threshold of D_{GD} (2.7V – Figure 24) the diode begins to conduct and a notable current will flow through the gate-to-drain diode (D_{GD} in Figure 12). Hence the drain and the gate form a short-circuit and as a result the gate-source junction is pinched-off which leads to the saturation of the channel. When conducting a relatively high load current the gate potential will be pulled down by the drain terminal through the gate-to-drain diode (D_{GD}). This reduces V_{GS}, restricts the JFET channel and increases voltage drop across source-to-drain terminals. The result will be a rapid decrease of gate potential to a point whereby the gate-to-source junction breaks down, and possibly cause device destruction.

While the device is capable of conducting high reverse current, it comes with the cost/requirement of high gate-to-drain voltage/current in order to provide a low on-state resistance. In a practical application, such a voltage/current has to be provided by the gate driver circuit. When conducting a relatively high load current, if the gate driver circuit is unable to provide the required current, the gate potential will be "pulled down" by the drain terminal through the gate-to-drain diode (D_{GD}). This effectively reduces V_{GS}, narrowing down the JFET channel and increases voltage drop across source-to-drain terminals. This acts to decrease drain potential which in turn brings down gate potential even further.

It should be noted that while this problem is valid for all vertical trench JFETs, it is not as severe in the case of normally-on JFETs as the normally-off versions (reverse saturation current for DM 47A, for EM 15A - Figure 29, Figure 30).

Thus the reverse behavior of the semiconductor is summarized in the next equations.

Requirements for reverse conduction		Equations
$\boldsymbol{V_{GS} > V_P}$ **or** $\boldsymbol{V_{GD} > V_p \Leftrightarrow V_{DS} < V_{GS} - V_p}$ $\longrightarrow$ **N-off :** $\boldsymbol{V_{DS} < V_{GS} - 1}$ **(19)** **N-on :** $\boldsymbol{V_{DS} < V_{GS} - 7}$ **(20)**	$\left.\begin{matrix} I_D \\ V_{SD} \end{matrix}\right\}$ *small values such that* $V_{DS} > V_{GS} - 2.7 \Leftrightarrow V_{GD} < 2.7V$	$I_D = I_{DSS\_r}\left(e^{\frac{qV_d}{nkT}} - 1\right)$ (21)
	$\left.\begin{matrix} I_D \\ V_{SD} \end{matrix}\right\}$ *large values such that* $V_{DS} < V_{GS} - 2.7 \longrightarrow D_{GD}$ *conducts* $\longrightarrow$ *GS junction is pulled down* $\longrightarrow$ *GS is pinched − off*	$I_D = -I_{DSS\_r}\left[1 - \frac{V_{GD}}{V_p}\right]^2$ (22)

Table 2. Reverse conduction summary.

According to the above equations it is evident that equivalent diode within the vertical channel JFET can conduct current in reverse direction even when the gate of the device is not turned ON. Thus it results to the advantage of DM-mode versus EM-mode SiC VT JFET; for the same V_{GS} (e.g. -15V) the normally-on device begins to conduct in a reverse way for $V_{DS} = -8V$ in contrast with normally-off V_{DS}=-16V. This yields less power losses during the current flow for the first device.

A reverse conduction curve of the SiC-JFET is measured by sweeping V_{SD} from zero to a positive voltage while keeping V_{GS} at a constant value. By varying the V_{GS} bias, a group of such curves are obtained. Such a group of curves for the tested device are plotted in Figure 29 and Figure 30.

From the following plots the reverse current abilities of the design are confirmed. It is shown that through the channel of DM JFET can be conducted a maximum current of -48A enough for our application. The resistance during this operation was also found to be 95mΩ. The measured currents for the EM were smaller (14A) while the on-resistance 110mΩ. . In cases where V_{GS}<V_p, a relatively high voltage drop is recorded especially in a EM SiC JFET due to its positive threshold voltage.

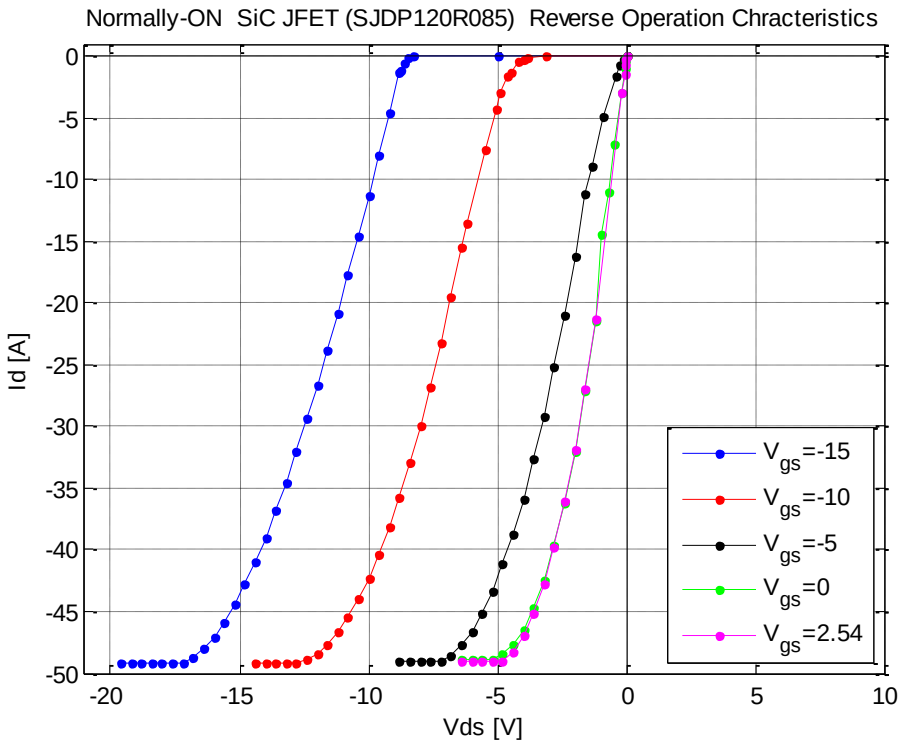


Figure 29.Normally-on I-V reverse characteristics for various V_{GS}.

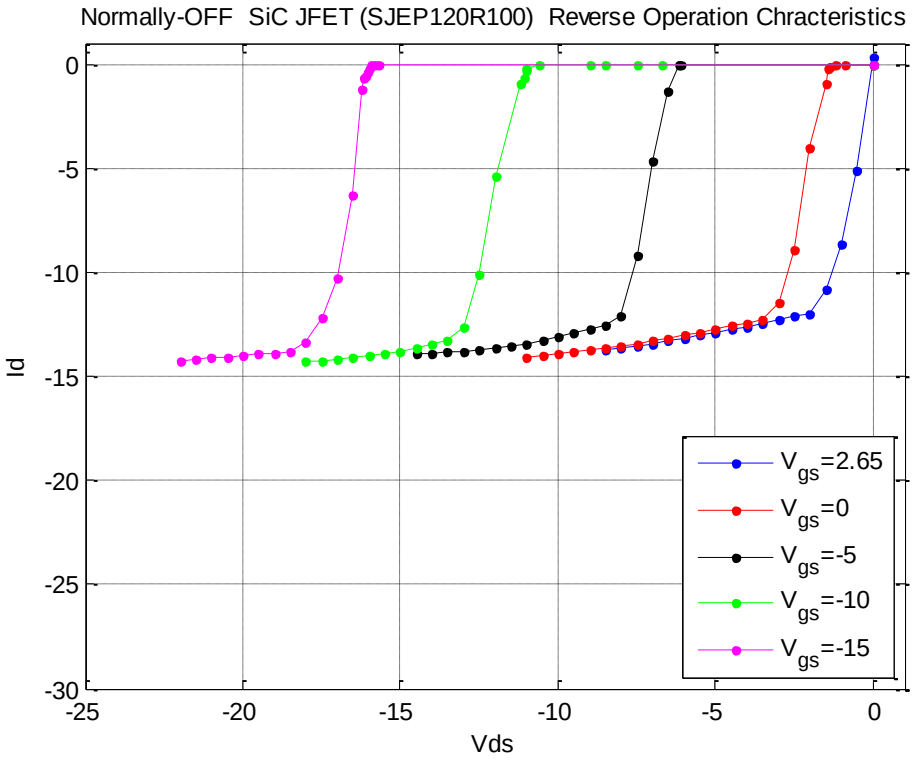


Figure 30. Normally-off I-V reverse characteristics for various V_{GS}.

Furthermore, in Figure 31, Figure 32, the reverse conduction of the VT SiC DM and EM JFET with V_{GS}=3V and V_{GS}=-15V are compared with a typical SiC-SBD, the body diode of a Si MOSFET and the antiparallel diode of an IGBT.

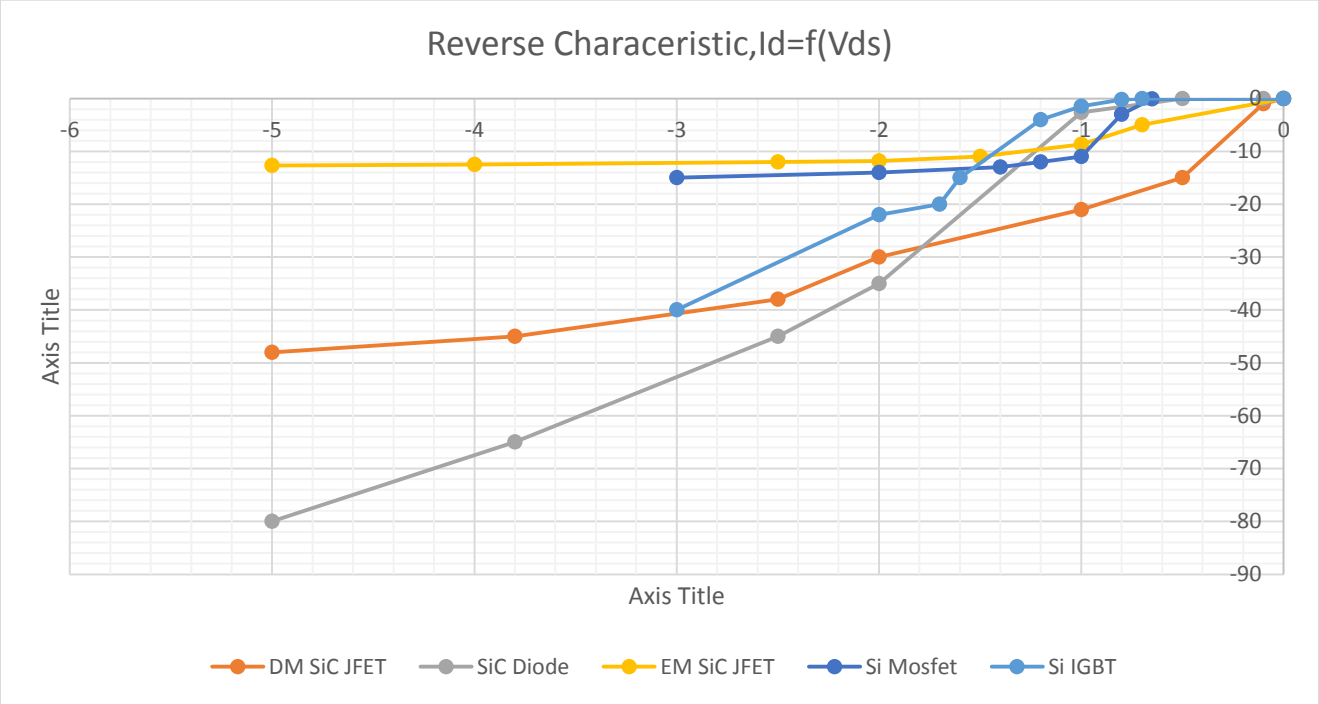


Figure 31.Comparison between reverse characteristics for Normally-on (SJDP120R085), Normally-off (SJEP120R100) for V_{GS}=3V, Si MOSFET and Si IGBT versus forward current of the SiC Power Schottky Diode (SDP30S120).

In the case where V_{GS}=3V, the reverse characteristic of the Normally-on SiC JFET outperforms all the other devices. It has the lowest voltage drop and thus the lowest power losses. Until the 30A its behavior is even better than the classical diode.

For small currents (I<15A) we can say that both the new devices can stand better than silicon ones as they exhibit lower voltage drop. For larger currents the normally-off is comparable with the body diode of the MOSFET while normally-on is still a better option than an IGBT. Of course the SiC diode can conduct larger currents with less losses.

On the other hand when V_{GS}=-15V the voltage-drop for the normally-off is the largest one. In order to conduct reverse current we need to wait until the opening of the channel in the drain side which leads to significant voltage drop. But the loss in the efficiency is not so big as long as this interval is kept small enough.

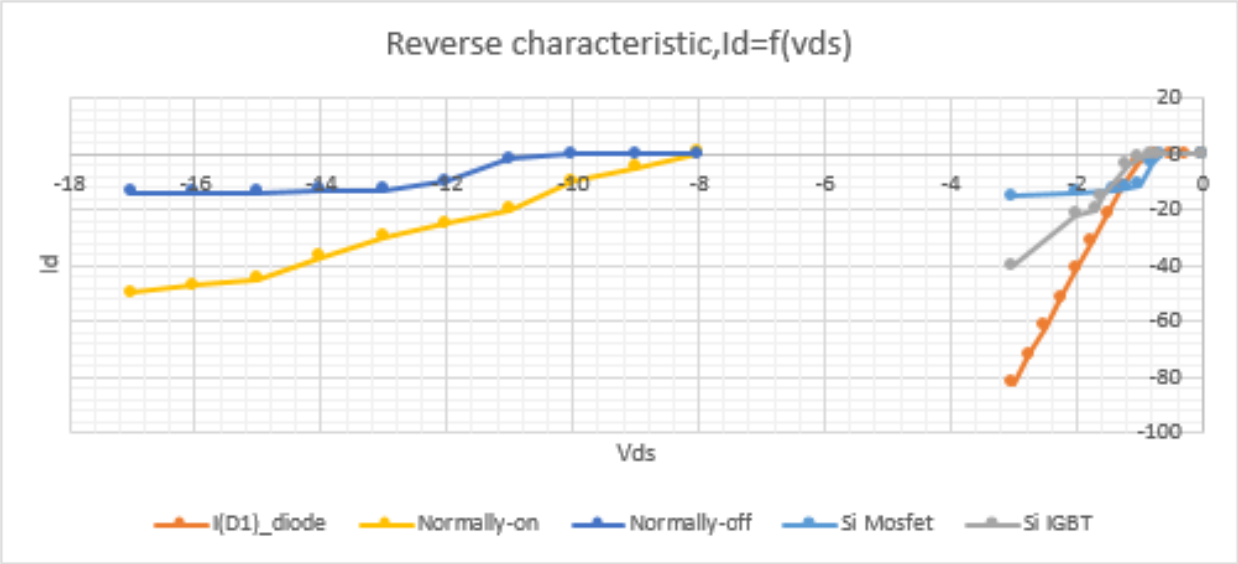


Figure 32. Comparison between reverse characteristics for Normally-on (SJDP120R085) and Normally-off (SJEP120R100) for V_{GS}=-15V versus forward current of the SiC Power Schottky Diode (SDP30S120) and Si MOSFET and Si IGBT

Finally some usual applications are presented where we apply the previous results in order to investigate the need of a freewheeling diode.

- *During Dead Time*

In phase-leg-based applications, to prevent shoot-through between devices at high side and low side, dead time is introduced between the falling-edge and the rising-edge of drive signals in the same phase-leg. During the dead time, a negative voltage is applied to the gate terminal of both JFETs to turn them OFF reliably.

The freewheeling diode only needs to conduct during the short dead time period. The higher VF of the diode will force a higher amount of the current through the reverse conducting JFET. Including an antiparallel diode is helpful in reducing this voltage drop during this short period. Furthermore, reverse voltage's dependency on gate voltage is verified.

In order to simulate this case, new models of SiC VT Depletion-mode (SJDP120R085), Enhancement-mode (SJEP120R100) JFET and SiC Power Schottky Diode (SDP30S120) were constructed using Pspice Model Editor. Details on the modelling procedure will be given in the next section. A half bridge inverter was simulated with V_{GS} = -15V, V_{DC}=200V, R=47Ω and L=150mH.

In Figure 33, output waveforms are zoomed out to evaluate the performance of JFETs during this interval along with the gate voltage. It is clear that during the dead time, because of the negative gate bias, the JFET reverse conduction voltage drop is for DM JFET V_{DS}=8V, EM JFET V_{DS}=16V and Power SiC Diode V_F=1V as explained in equations 19, 20 in table 2. If

we use lower gate values for depleting the channel according to these equations the voltage drop would be even smaller.

The results show that while the JFET-only version may lead to somewhat increased losses during the dead time period, overall device dynamic loss increase is limited to a level around 10% in the case of the DM JFET and 15% for the EM. Thus the antiparallel diodes can be considered redundant as long as the dead band is kept small.

Detailed device loss in a full-bridge 1-phase inverter will be given in chapter 5.

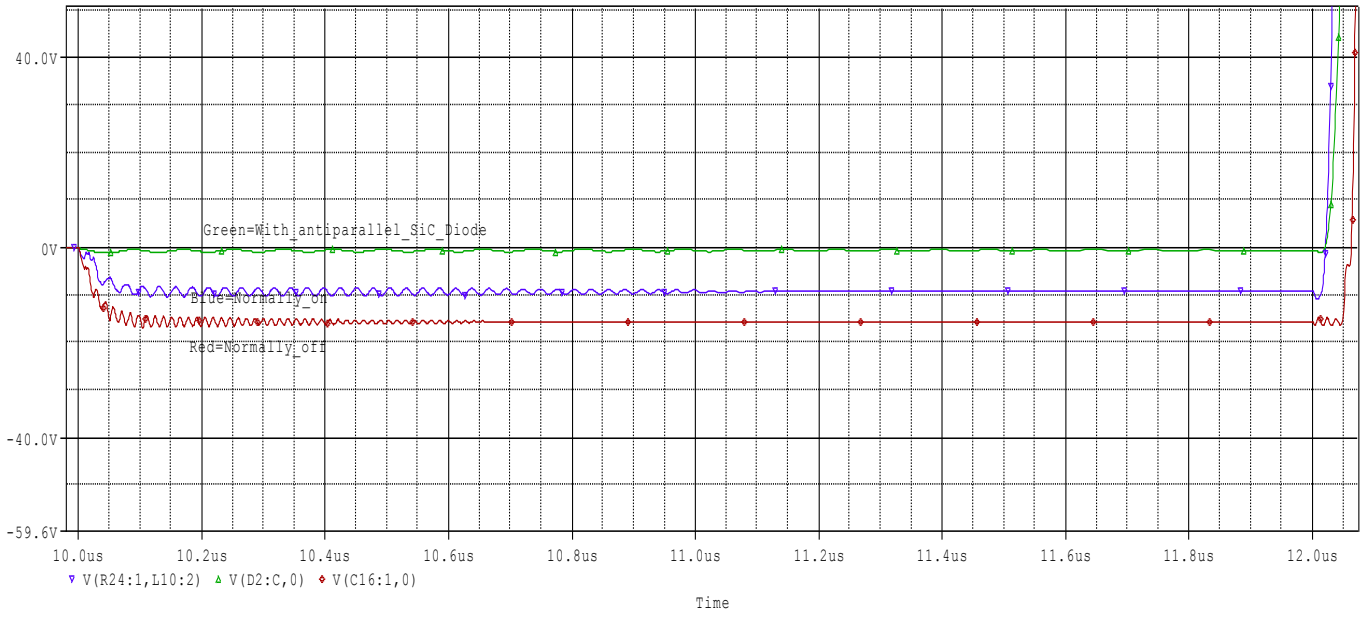


Figure 33. Voltage drop comparison during dead time in a phase leg topology. Green is with SiC Power Schottky Diode SDP30S120, blue is DM JFET SJDP120R085 and red EM JFET SJEP120R100

- *Reverse Recovery Time*

While correctly driving the SiC JFETs can force an external diode to carry reverse currents, characterization of the JFETs' own reverse recovery behavior is useful in determining the necessity of such an external diode. The reverse recovery characteristics of the SiC JFET were measured in the documents [23], [24] and [6] their results are presented here.

Device	Reverse Recovery time
SJDP120R085	28ns
SJEP120R100	38ns

SDP30S120	25ns
SJEP120R100 + SiC Diode	46ns
Si MOSFET (600V)	420ns
Si Ultra-fast diode	24.5ns
FGA25N120ANTD (Si IGBT+Diode)	300ns

Table 3.Reverse recovery time comparison.

The reverse recovery time of the SiC JFET was found to be significantly smaller than that of the silicon MOSFET. In combination, an EM SiC JFET and SiC diode also achieved far superior reverse recovery times than those exhibited by the silicon MOSFET. The reverse recovery of the DM SiC JFET itself was also found to be significantly fast and comparable with a single SiC Diode. The lack of any performance advantage being achieved in this test by the addition of an antiparallel diode to the SiC JFET, suggests that such an external diode is likely to be unnecessary in a majority of applications.

2.6 Conclusions

The mechanism of reverse conduction during both on-state and off-state is an inherent nature of JFET channels, which exist in every JFET. Tests demonstrated that the VT SiC JFET conducts well in the reverse direction with only a small voltage drop across the channel. Application of a negative gate-source bias was found to result in an increase in the channel voltage drop of a similar magnitude.

Typically the body diodes of silicon MOSFETs exhibit very poor reverse recovery characteristics, limiting the switching speeds in hard-switched constant inductor current applications. The reverse recovery of the SiC JFET itself was also found to be significantly faster than that of silicon MOSFETs, removing the motivation to use a fast external anti-parallel diode. The SiC JFET is thus well suited to high-speed synchronous rectification and bidirectional switching applications where the reverse recoveries of silicon MOSFET body diodes typically limit switching performance.

Designers that want to include a freewheeling path can add a SiC Schottky diode and for the aggressive designs, we have shown that no antiparallel diode is required for reverse conduction for both normally-on and normally-off devices with only minimal impact on dynamic losses.

There are also other references [4], [6], [7], [8], [9], [10] which confirm the superiority of the SiC JFET against Si semiconductors and propose the elimination of the freewheeling diode. Through their applications and their conclusions they proved the uselessness of such diode due to the special reverse properties of SiC JFET. We are also going to apply the results discussed on this section on our converter in chapter 5 in order to verify the correctness of them.

The structure and performance of the SiC Vertical Trench JFET have been shown to be advantageous in operational modes where traditional high voltage MOSFET or IGBTs require the use of an external freewheeling diode. The reverse recovery of the SiC JFET itself was also found to be significantly faster than that of silicon MOSFETs. In conclusion, when the vertical-channel JFETs are used for freewheeling purpose, the reverse-recovery currents are only caused by the depletion charge of the device and no minority injection is involved. This is different and superior to devices with parasitic reverse P–N junction diodes like MOSFETs or lateral–vertical JFETs.

Both devices are capable of conducting reverse current with minimal power losses. They are compared with SiC diodes and as it is seen they seem to have the same behavior. Due to the exceptional property of SiC JFET of not having reverse recovery current they make them superior power semiconductors compared to the conventional MOSFET that are widely used.

MOSFETs have the disadvantage of large recovery time which may lead to short-circuits in bridge configurations especially when we use high frequencies. This limitation in the switching speed is not met in the SiC JFETs making them competitive commercial semiconductors. Furthermore, in high voltage applications (1200V) such as hard switched inverters, high voltage MOSFETs (> 600 V) are typically not used because of the poor recovery characteristics of the body diode.

At higher voltages using IGBTs or cascode LV JFET topologies, it is common to place an antiparallel diode across the device to commutate the reverse current in bridge circuits. The 1200 V SiC trench JFET however, can be used in reverse mode without the complication of a body diode, enabling significant power and BOM cost savings in applications such as solar inverters and UPS.

The DM JFET can conduct larger currents than the EM JFET and as it shown with less voltage drop in the drain source junction. The drain-source voltage must be kept low and the operating point must be kept within a safety region in the output characteristics so as to avoid the conduction of the intrinsic gate-drain diode.

In many applications, the conventional Si IGBTs in power electronic converters have been directly replaced by the SiC power devices, leading to the increased power efficiencies and switching frequencies. For example, by directly replacing the employed Si IGBTs of an inverter for solar energy conversion with the enhanced mode SiC JEFTs, Semi-south has validated that both conduction losses and switching losses of the inverter are reduced by 50% [13]. For power converters in middle switching frequency conditions (around *20 kHz*), very high efficiency were achieved [14-15].

As a result, the antiparallel diodes can be eliminated with minimal performance sacrifice for many converter applications. This can reduce the component count and cost of the whole system.

2.7 Spice Model of SiC elements for Circuit Simulations

2.7.1 *Spice Models for the SiC JFET: SJDP120R085 and SJEP120R100*

On this paragraph we provide information about the procedure of the construction for the two high voltage transistors, 1200V, 27A DM (SJDP120R085) and 1200V, 17A EM (SJDP120R100) SiC JFET for circuit simulations in Spice using Spice Model Editor. The model parameters have been extracted from experimental plots. Simulations are used afterwards to verify the developed compact models.

Spice in order to model the JFET is using an intrinsic FET with an ohmic resistance (R_D) in series with the drain, and with another ohmic resistance (R_S) in series with the source like Figure 12 but without the parasitic inductances L_G, L_D, L_S. Positive current is current flowing into a terminal. The capacitances are non-linear and are depended by the voltages V_{GS}, V_{GD}, V_{DS}. There is no p-n junction between source and drain and therefore the JFET has no body diode.

The drain current is described by the equations [1], [2], [3]. We are going to use the Spice Model Editor. The parameters we need to compute for this Spice utility, either by experimental plots or trial and error until we approach the datasheet plots, are the following.

Model parameters	Description	Units	SJEP120R100	SJDP120R085
AF	Flicker noise exponent		1	1
ALPHA	Ionization coefficient	volt	1e-006	1e-006
BETA	Transconductance coefficient	Amp/volt	27	3.4685
BETATCE	BETA exponential temperature coefficient	%/°C	-1.25	-1.6
CGD	zero-bias gate-drain p-n capacitance	farad	9.19e-10	9.7e-010
CGS	zero-bias gate-source p-n capacitance	farad	6.1e-10	5.8e-010
FC	forward-bias depletion capacitance coefficient		0.5	0.5
IS	gate p-n saturation current	amp	1e-14	1e-014

ISR	gate p-n recombination current parameter	amp	0	0
KF	flicker noise coefficient		1e-18	1e-018
LAMBDA	channel-length modulation	volt	0.005066	0.014173
M	gate p-n grading coefficient		0.92	0.59
N	gate p-n emission coefficient		4.5	3.5
NR	emission coefficient for isr		1	1
PB	gate p-n potential	VOLT	2.5	2.5
RD	drain ohmic resistance	Ohm	0.25	0.2
RS	source ohmic resistance	ohm	0.25	0.2
VK	Ionization knee voltage	volt	2000	2000
VTO	Threshold voltage	volt	1.0718	-5.4069
VTOTC	VTO temperature coefficient	Volt/^{o}C	-0.0022	-0.02
XTI	IS temperature coefficient		86	86

- *BETA and BETATCE calculation*

Firstly we compute the BETA parameter. We extract this value from the plot gFS-I_{DS}, the transconductance of the JFET as a function of the drain current. More specifically gFS = dI_D/dV_{GS} and defines the sensitivity of the device in the gate-source voltage changing.

For this we use the plot I_D, V_{GS} [11] [Figure 34, Figure 35] and from the linear part of the plot we calculate the slope which gives us the value of gFS [Figure 36, Figure 37].

Transconductance exponential temperature coefficient BETATCE determines the limit of saturation current level at elevated temperature. It can be expressed and extracted by the equation below

$$\beta(T_2) = \beta(T_1) \times 1.01^{BETATCE(T_2 - T_1)}$$

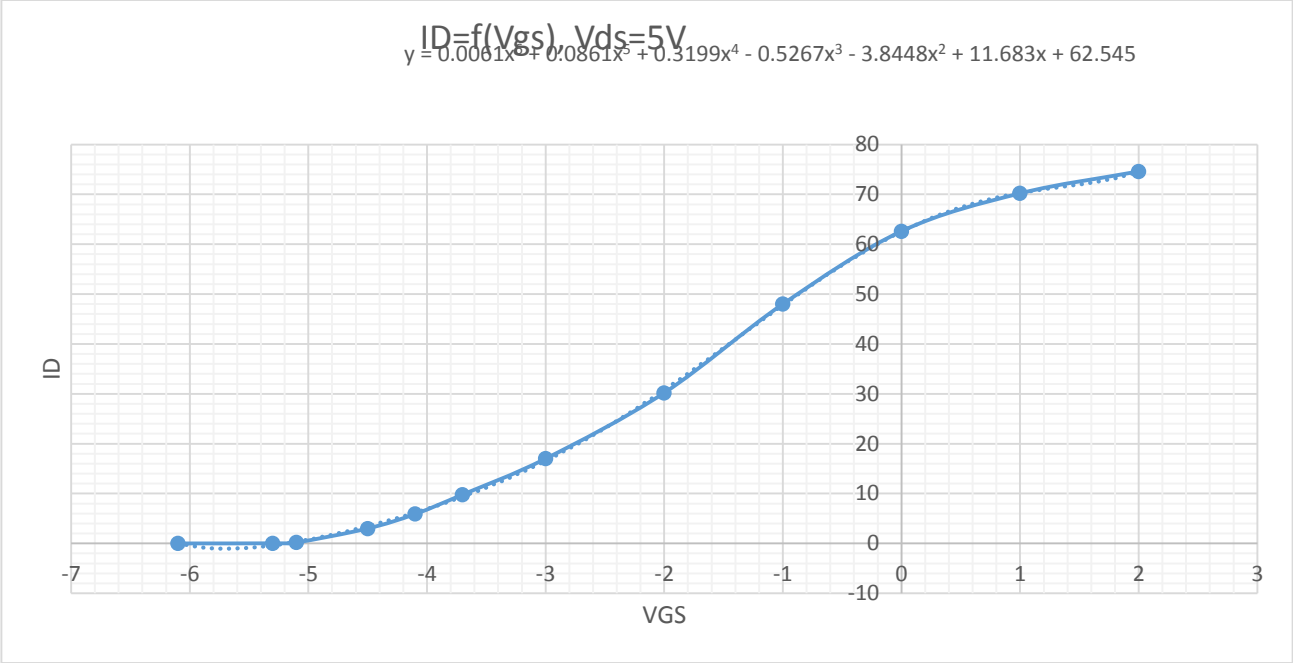


Figure 34. $I_D=f(V_{GS})$ of SJDP120R085, for g_{FS} computing.

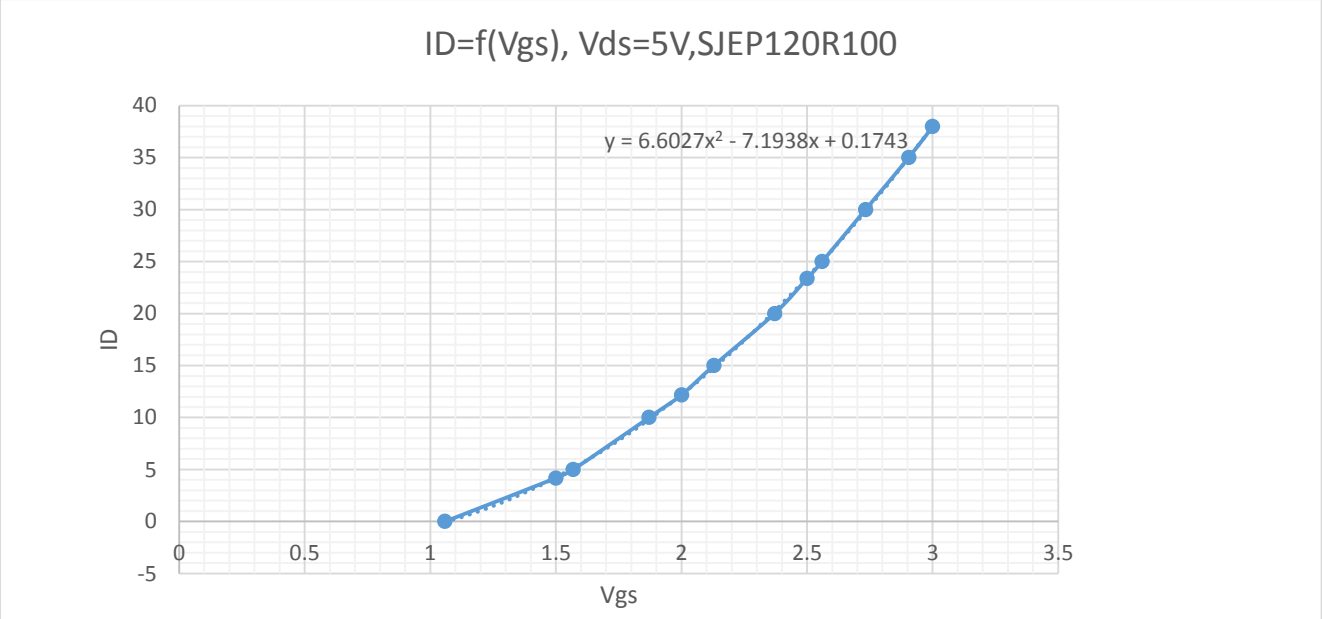


Figure 35 $I_D=f(V_{GS})$ of SJDP120R100, for g_{FS} computing.

By inserting the values from the following plot in the $g_{FS}=f(I_D)$ characteristic that the Model editor asks, the BETA is calculated.

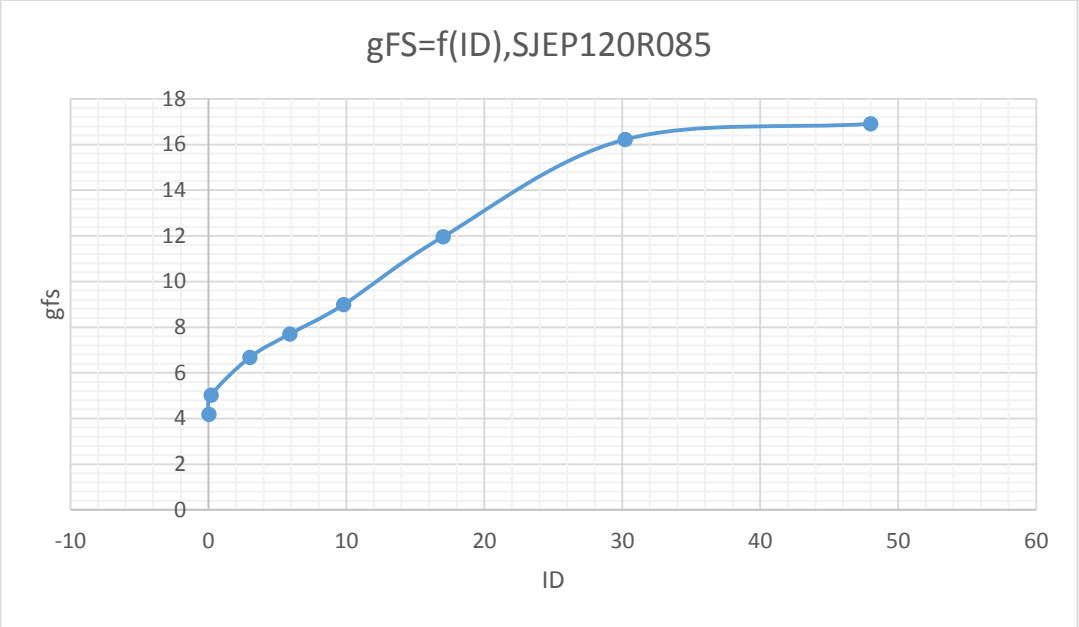


Figure 36. g_{FS} calculation for SJDP120R085.

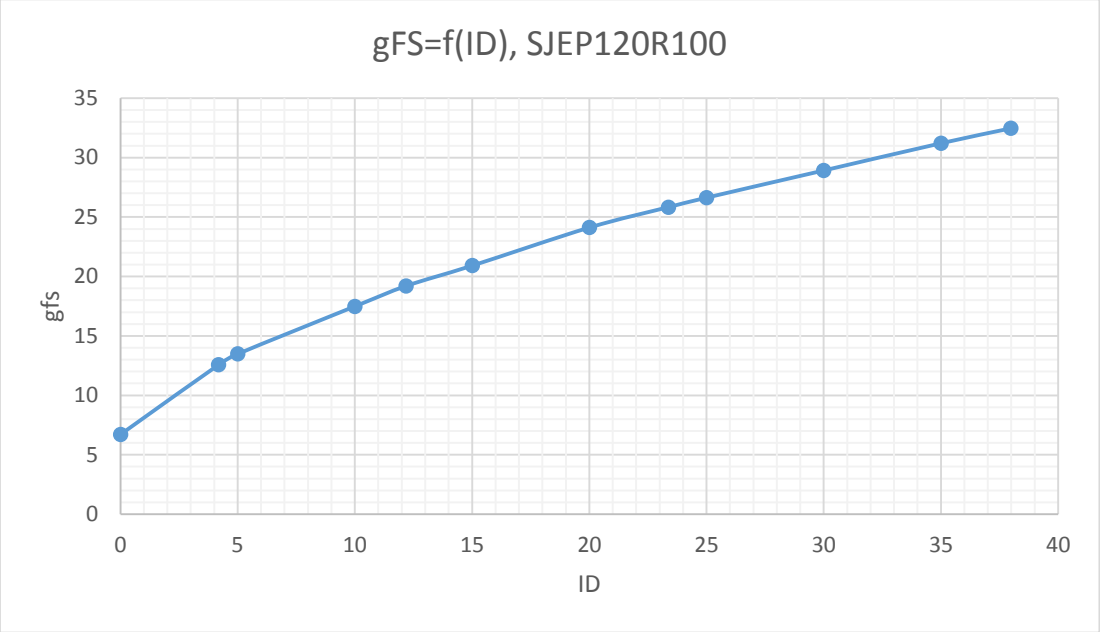


Figure 37. gFS calculation for SJDP120R100.

- *LAMBA calculation*

The second plot that must be inserted in the program is the g_{OS}-I_{DS}. This is the output conductance as a function of the drain current. This plot is used for the estimation of the

LAMBA parameter. g_{OS} is the slope of the drain current as a function of the drain-source voltage. So for each V_{GS} we compute a different g_{OS}, which values are shown in Figure 38.

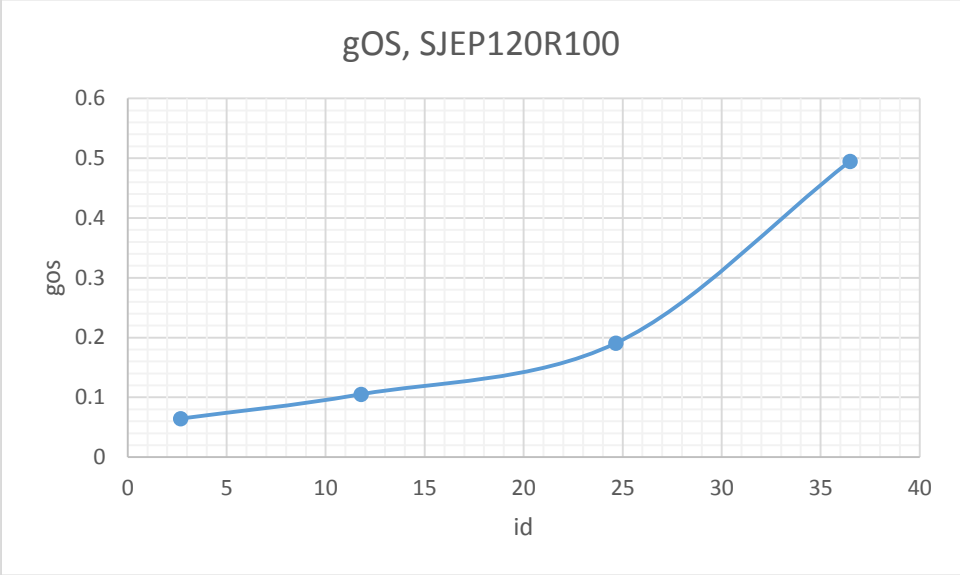


Figure 38. g_{OS} =f(I_D) for LAMBA calculation for SJEP120R100.

- *VTO and VTOTC calculation*

Next we insert the V_{GS} – I_D plot for a specific V_{DS} in the saturation region. By this plot the threshold voltage is extracted. The VTOTC defines the effect of the temperature in V_{TH}.

The threshold voltage VT0 varies with temperature according to the following equation

$$V_{T0}(T_2) = V_{T0}(T_1) + VTOTC(T_2 - T_1)$$

Thus, the parameter VTOTC can be extracted if the threshold voltage is plotted as a function of temperature.

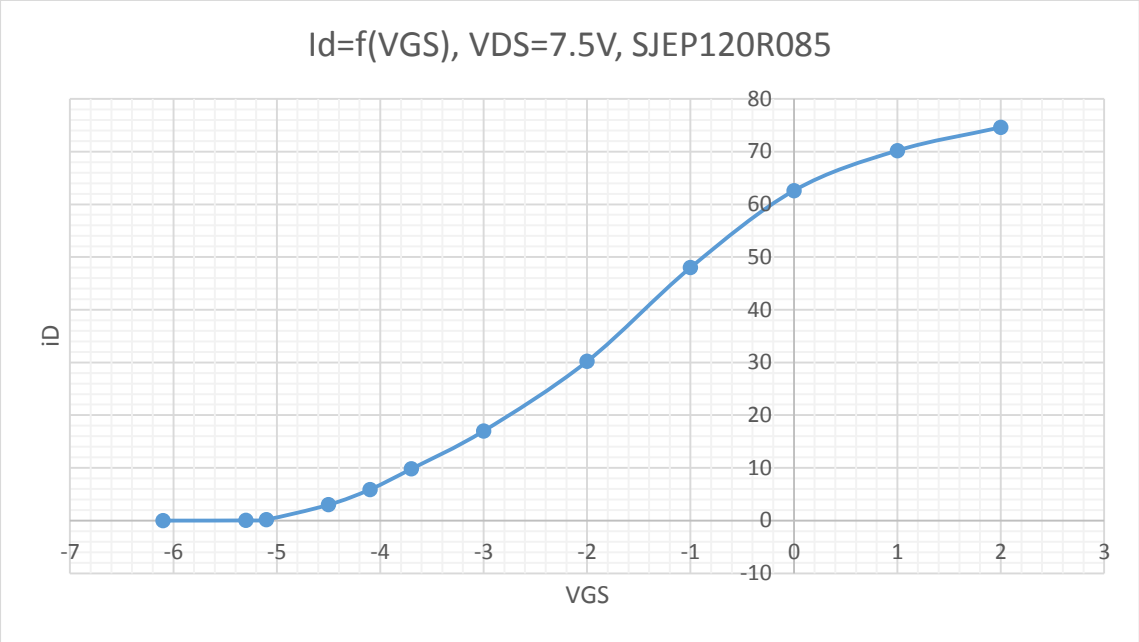


Figure 39. $I_D=f(V_{GS})$ for VTO parameter calculation for SJEP120R085.

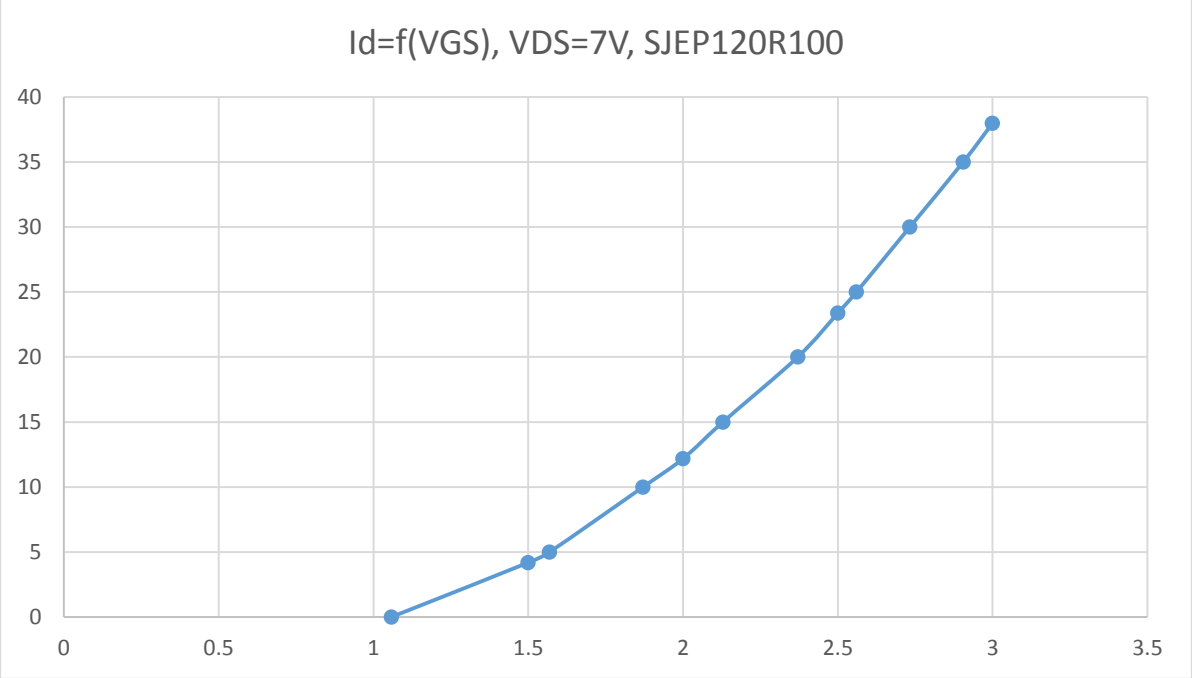


Figure 40. $I_D=f(V_{GS})$ for VTO parameter calculation for SJEP120R100.

- *Capacitances calculation*

The characteristics of the capacitances as a function of the voltages are the next ones. They exist in the datasheets in the following form.

Input capacitance : $C_{ISS} = C_{GS} + C_{GD}$

Output capacitance: $C_{OSS} = C_{DS} + C_{GD}$

Reverse transfer capacitance :$C_{RSS} = C_{GD}$

The same ones are met in the MOSFET with the difference that C_{DS} is considered negligible as it is much smaller from the others.

The capacitances are defined by the following equations

$$C_{GD} = \begin{cases} C_{GD} \times \left(1 - \frac{V_{GD}}{PB}\right)^{-M} & V_{GD} \leq FC \times PB \quad (23) \\ C_{GD} \times (1 - FC)^{-(1+M)} \times (1 - FC(1+M) + M\frac{V_{GD}}{PB} & V_{GD} > FC \times PB \quad (24) \end{cases}$$

$$C_{GS} = \begin{cases} C_{GS} \times \left(1 - \frac{V_{GS}}{PB}\right)^{-M} & V_{GS} \leq FC \times PB \quad (25) \\ C_{GS} \times (1 - FC)^{-(1+M)} \times (1 - FC(1+M) + M\frac{V_{GS}}{PB} & V_{GS} > FC \times PB \quad (26) \end{cases}$$

Consequently, to approach the values of the capacitances, we need to find the initial values of them C_{GS} (0), C_{GD} (0), FC and M. This happens by simulating the above functions in order to approach the datasheet plots.

- *Temperature dependence*

Temperature coefficients are especially important in power systems, since the devices might operate at high temperature. Important temperature coefficients include IS temperature coefficient (XTI), threshold voltage temperature coefficient (VTOTC), and transconductance exponential temperature coefficient (BETATCE). There parameters are extracted from temperature dependent measurements. Generally for high temperatures it is desirable to create a separate spice model for the SiC JFET in order to approach the real

values more satisfactorily. Though this is not the scope of this chapter and more details can be found in [11].

- *Parasitic elements*

Except from these values we also have the parasitics elements of the device. The resistances are chosen 0.02Ω while the inductances is more preferable to be placed in the project design as its effect can't be simulated exactly by the Model Editor.

Another important value was N (gate p-n emission coefficient) which is responsible for the correct simulation of the V-I characteristics of D_{GS} and D_{GD}. This value can be approached with the help of the *Figure 24* and the current equation of a typical diode $I = I_S e^{\frac{V_D}{N \times V_t}-1}$.

2.7.2 *Evaluation of the SiC JFET models*

In the next figures 28-33 we present the comparison plots between the Pspice Models we constructed and the datasheet values.

Firstly we show the output characteristics of the devices. Both models approach the datasheet values very good. In the case where we provide too much forward bias ($V_{GS}>2V$), our models have problem in simulating the real values but in normal conditions they are very well approached.

Secondly we show the transfer characteristics and the conduction resistance of the *JFET*. The simulation results are also satisfactory in this case.

Moreover, we have the on-resistance $R_{DS(on)}$ characteristic which is important for the simulations of the conduction losses.

Finally, we present and compare the reverse current characteristic for the Pspice model and the Figure 29, Figure 30. The voltage drop for various V_{GS} is simulated properly but as expected the current is not saturated. The Pspice JFET model is not based on a VT design and the parasitic effect of the D_{GD} can't be simulated. But still we can have satisfactory results in our converter simulations since we don't care for large currents (~5A are enough) and the reverse voltage drop is as it should which means that the power losses will be approached well enough.

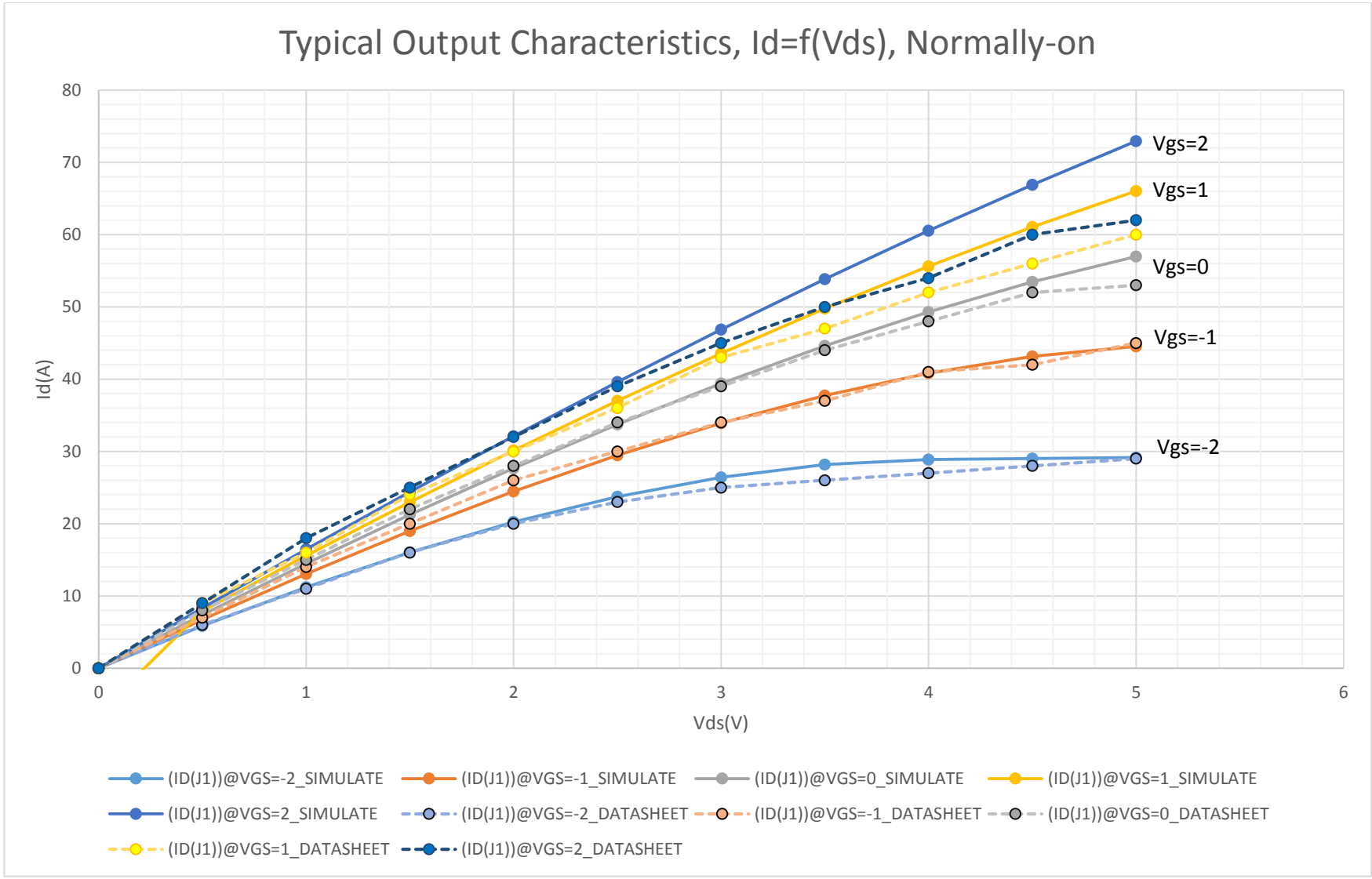


Figure 41. Output characteristics. Comparison between the simulated and datasheet values. The ones with the dashed lines are the experimental and the solid are the simulated values.

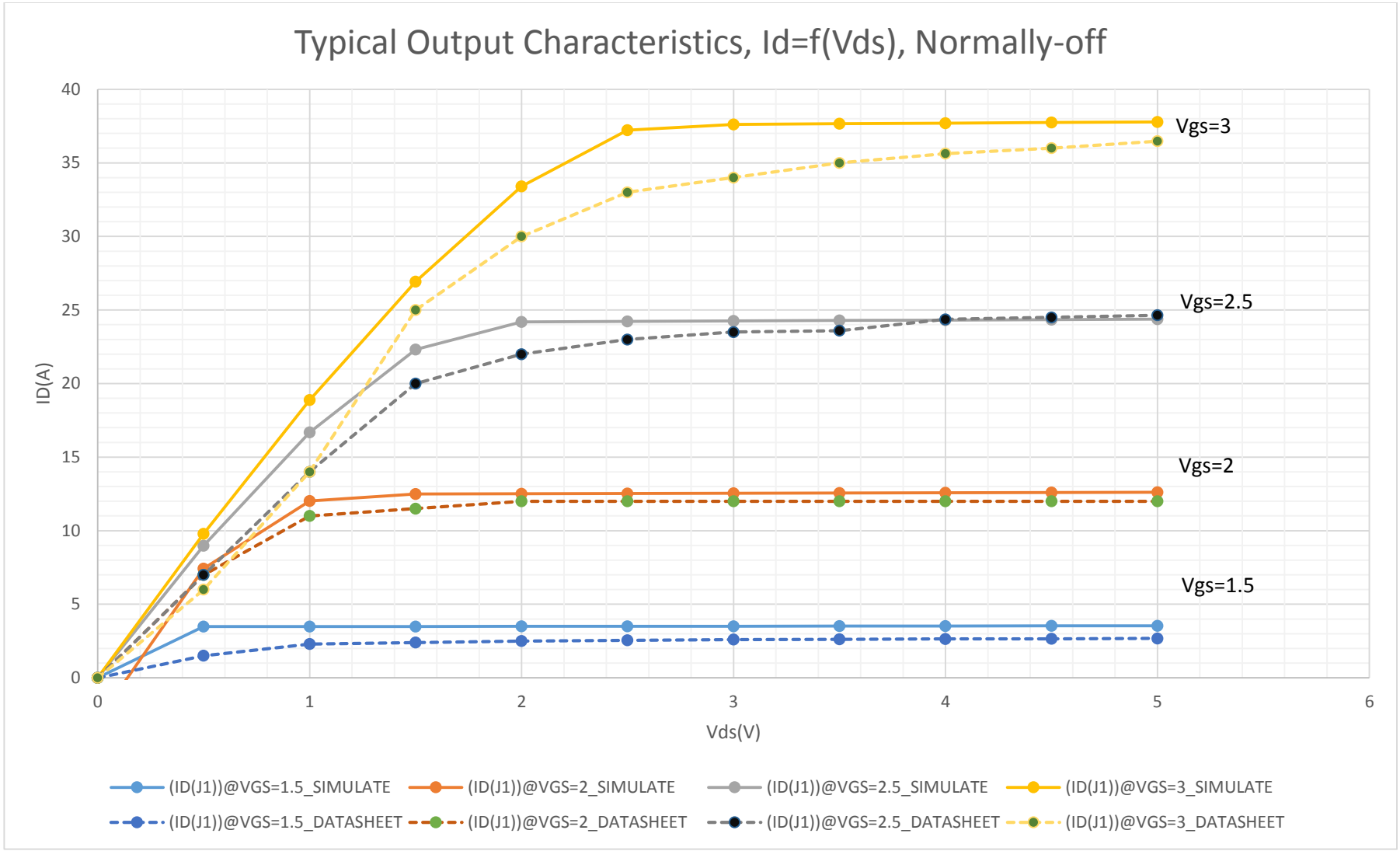


Figure 42. Output characteristics. Comparison between the simulated and datasheet values. The ones with the dashed lines are the experimental and the solid are the simulated values.

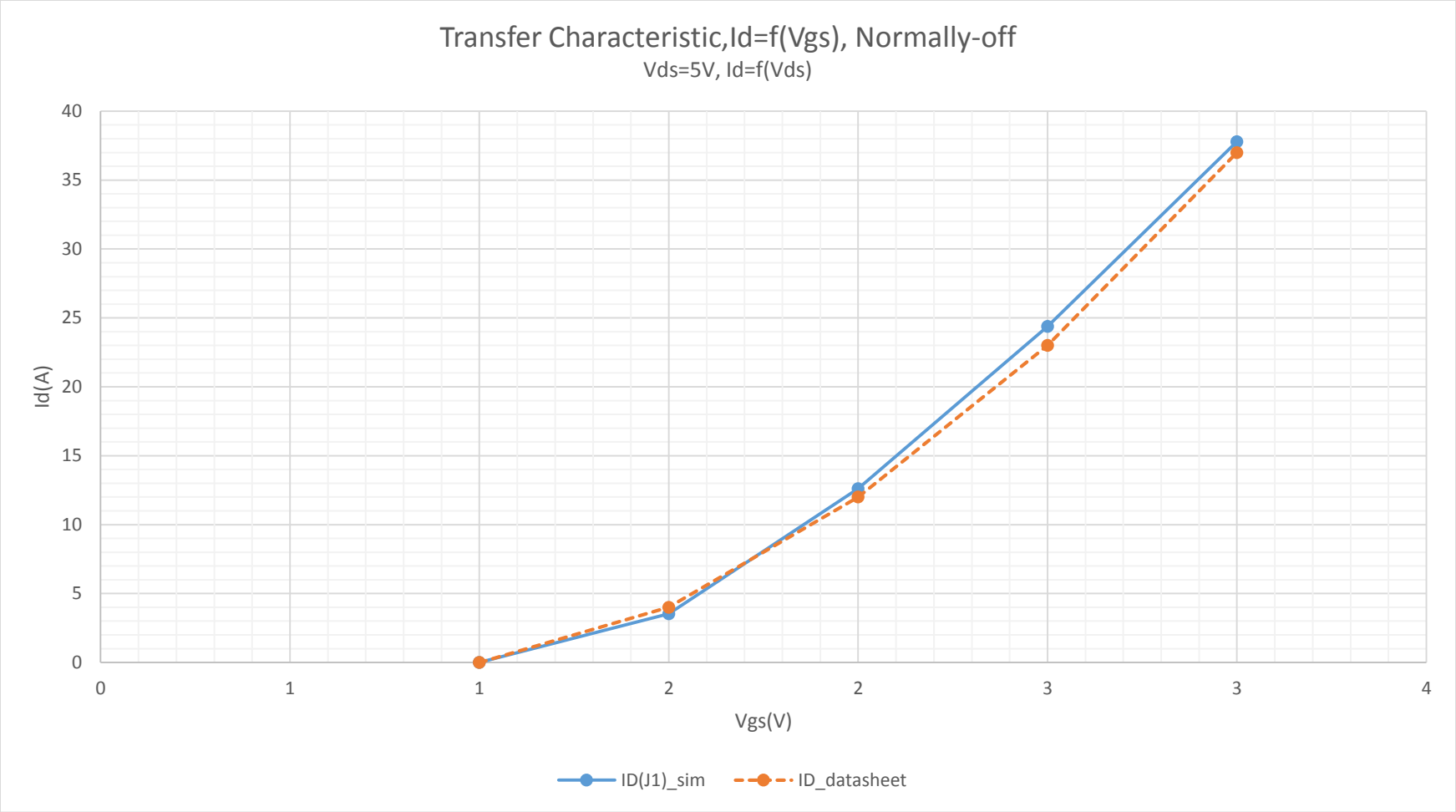


Figure 43. Comparison between the simulated and datasheet values. The ones with the dashed lines are the experimental and the solid are the simulated values.

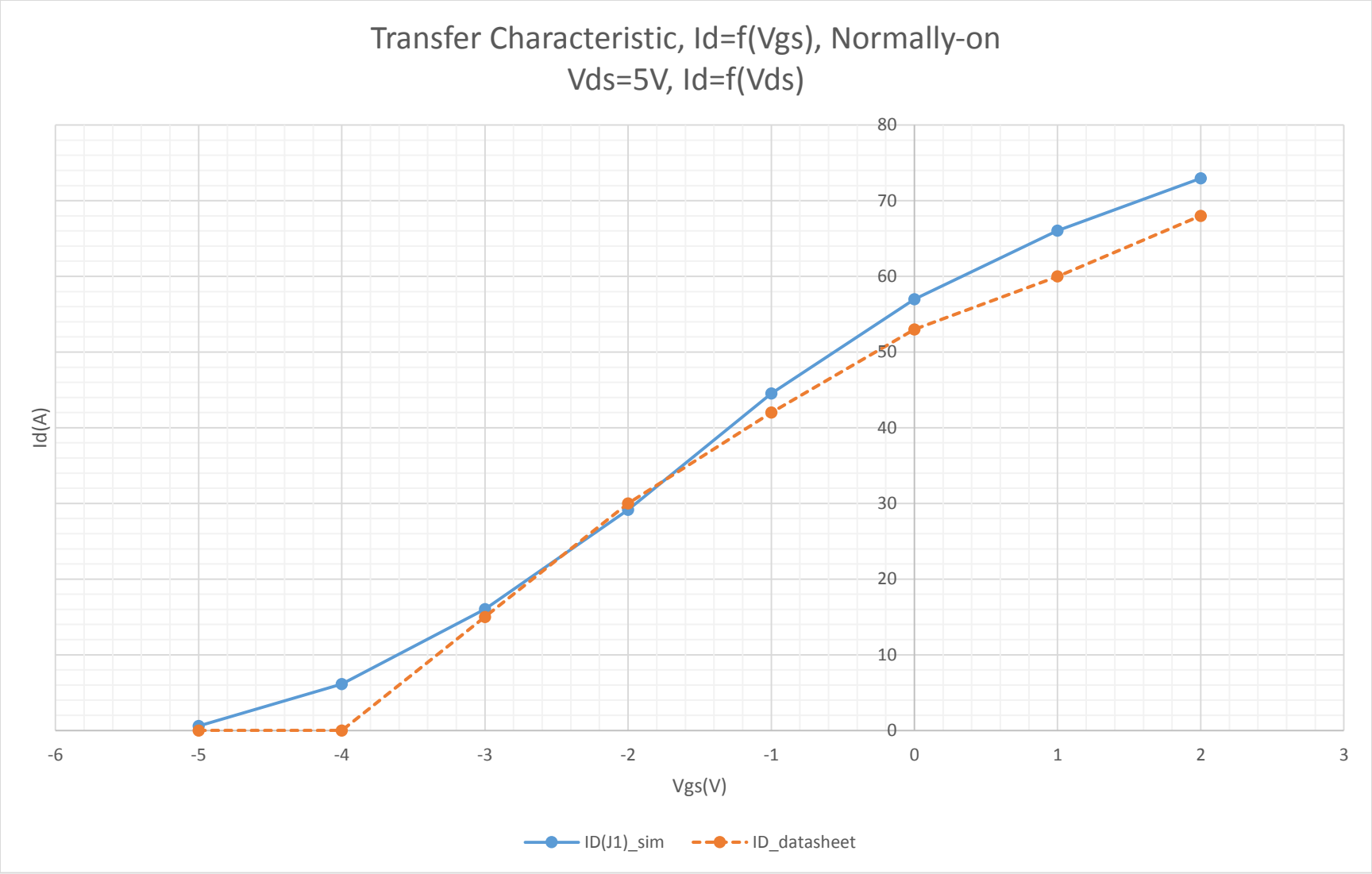


Figure 44. Transfer characteristic comparison. The ones with the dashed lines are from the datasheet and the solid are the simulated values.

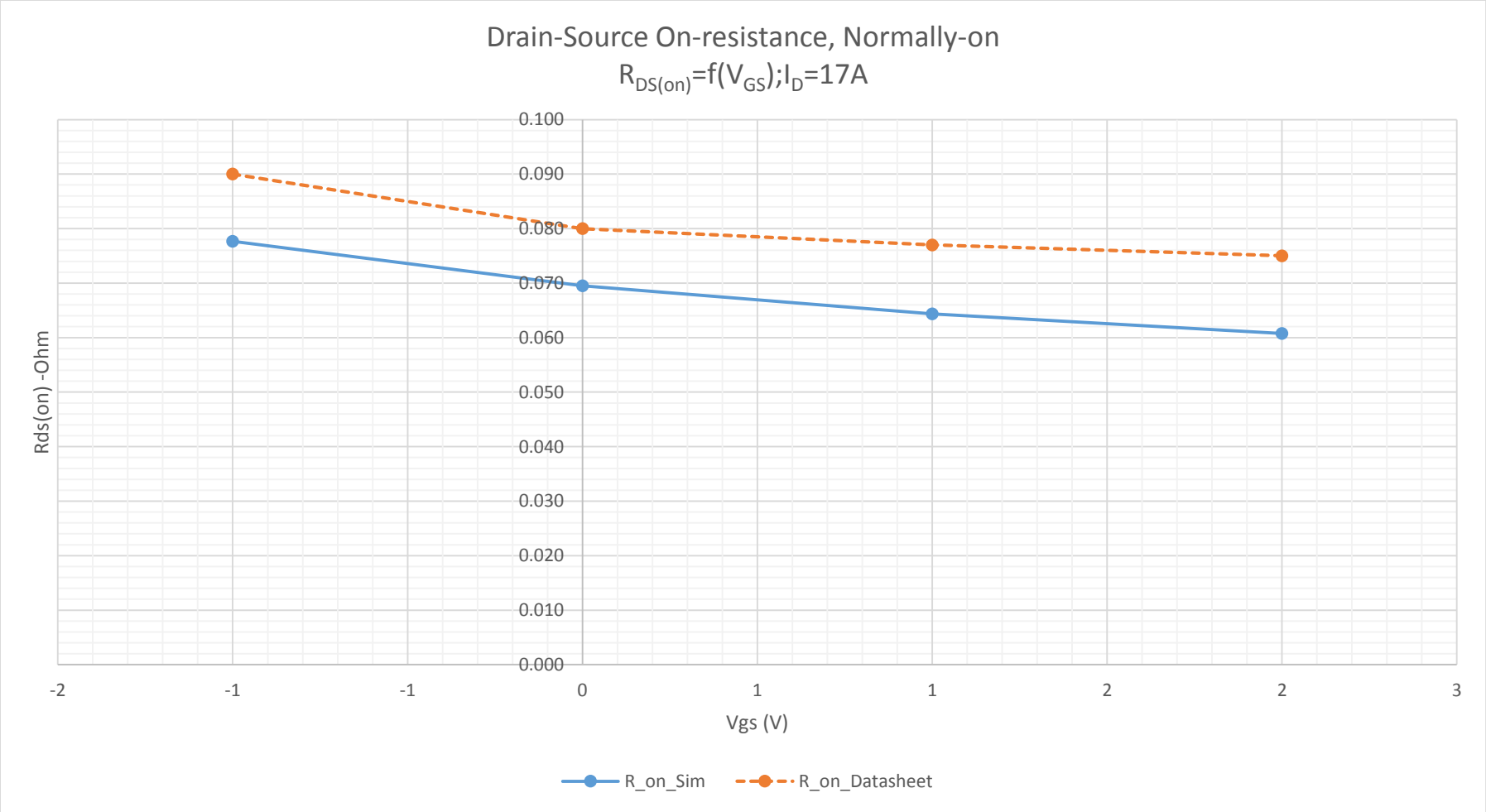


Figure 45. Transfer characteristic comparison. The ones with the dashed lines are from the datasheet and the solid are the simulated values.

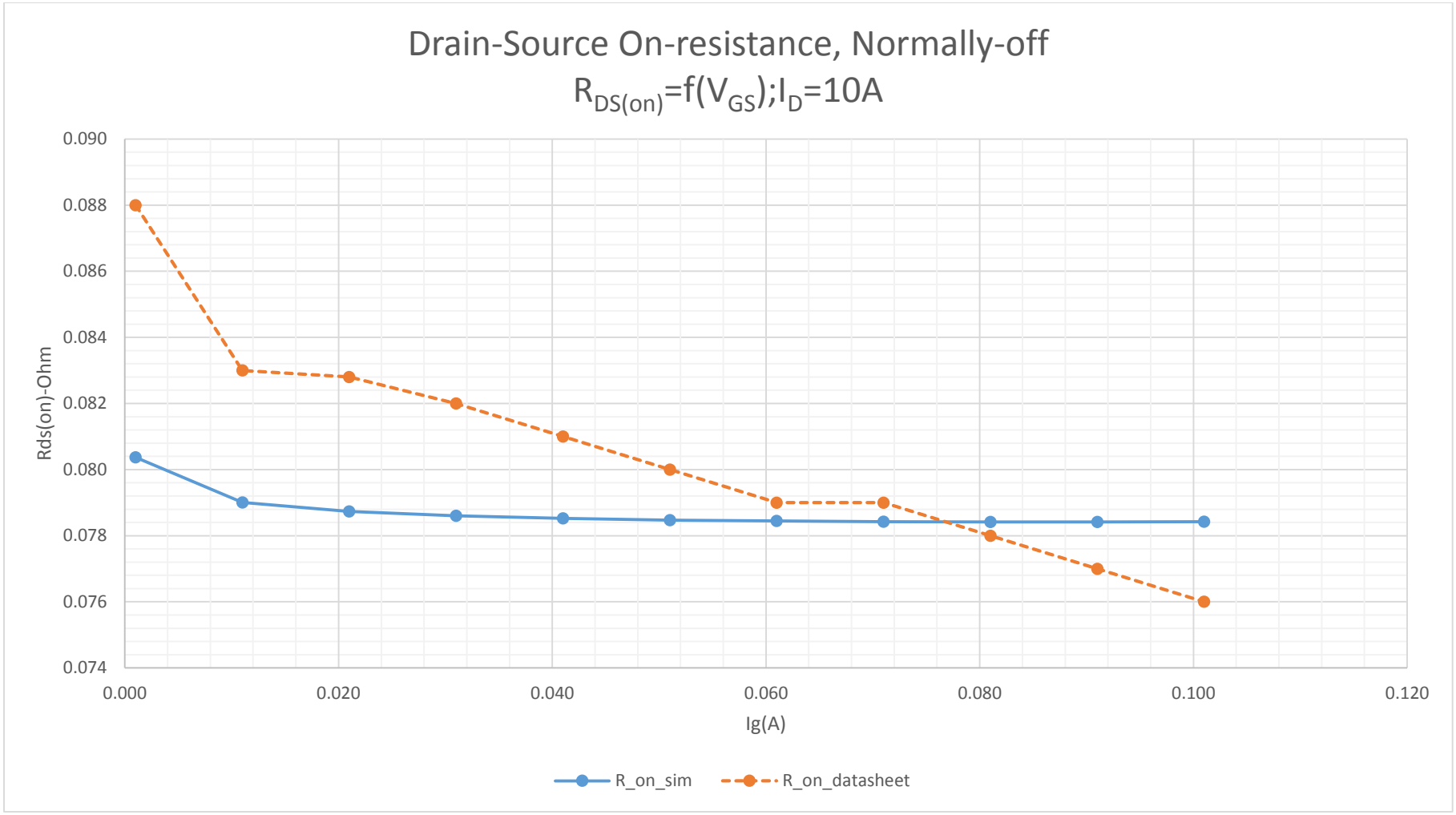


Figure 46. Drain-source on resistance comparison. The ones with the dashed lines are from the datasheet and the solid are the simulated values.

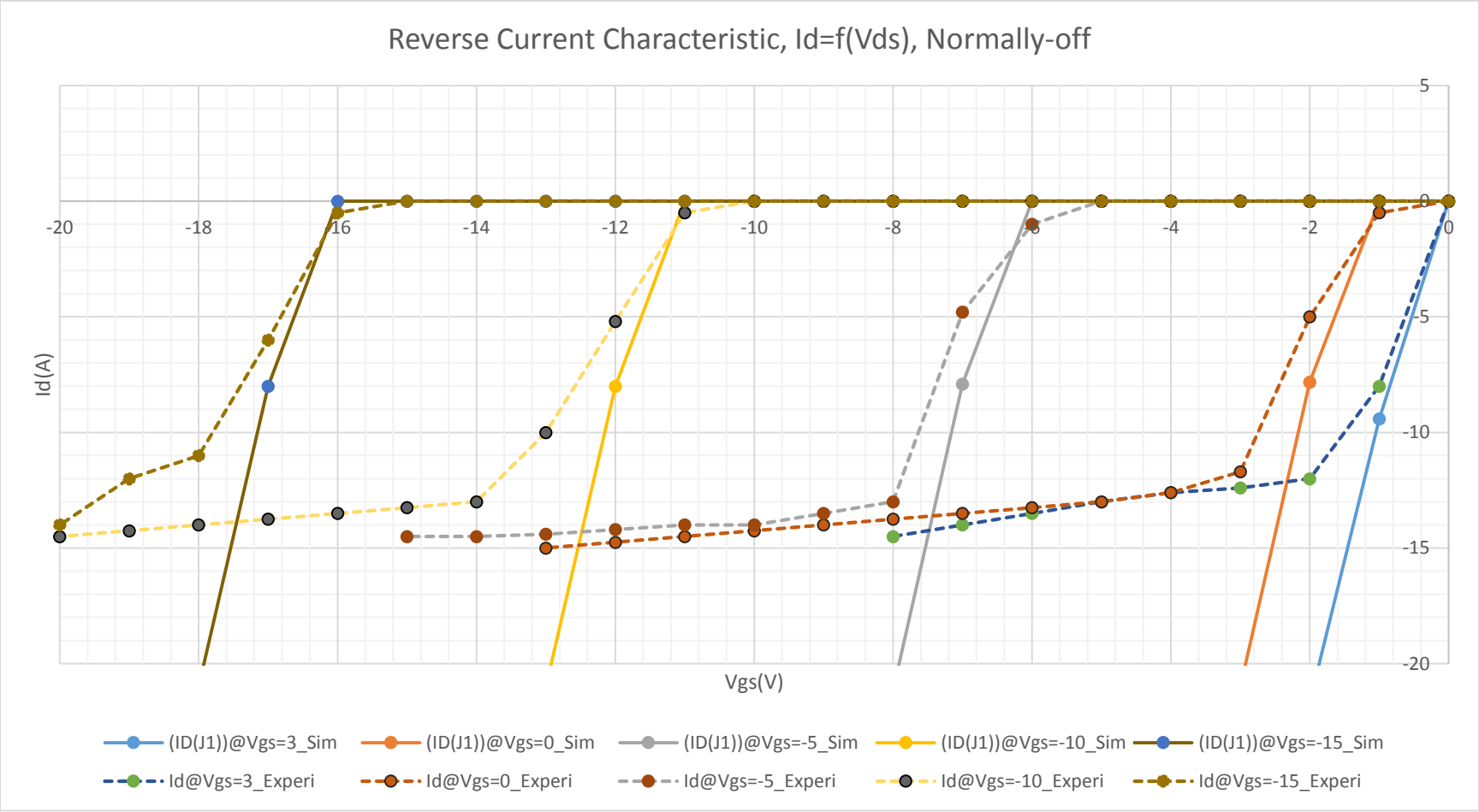


Figure 47. Reverse current characteristic comparison. The ones with the dashed lines are the experimental and the solid are the simulated values.

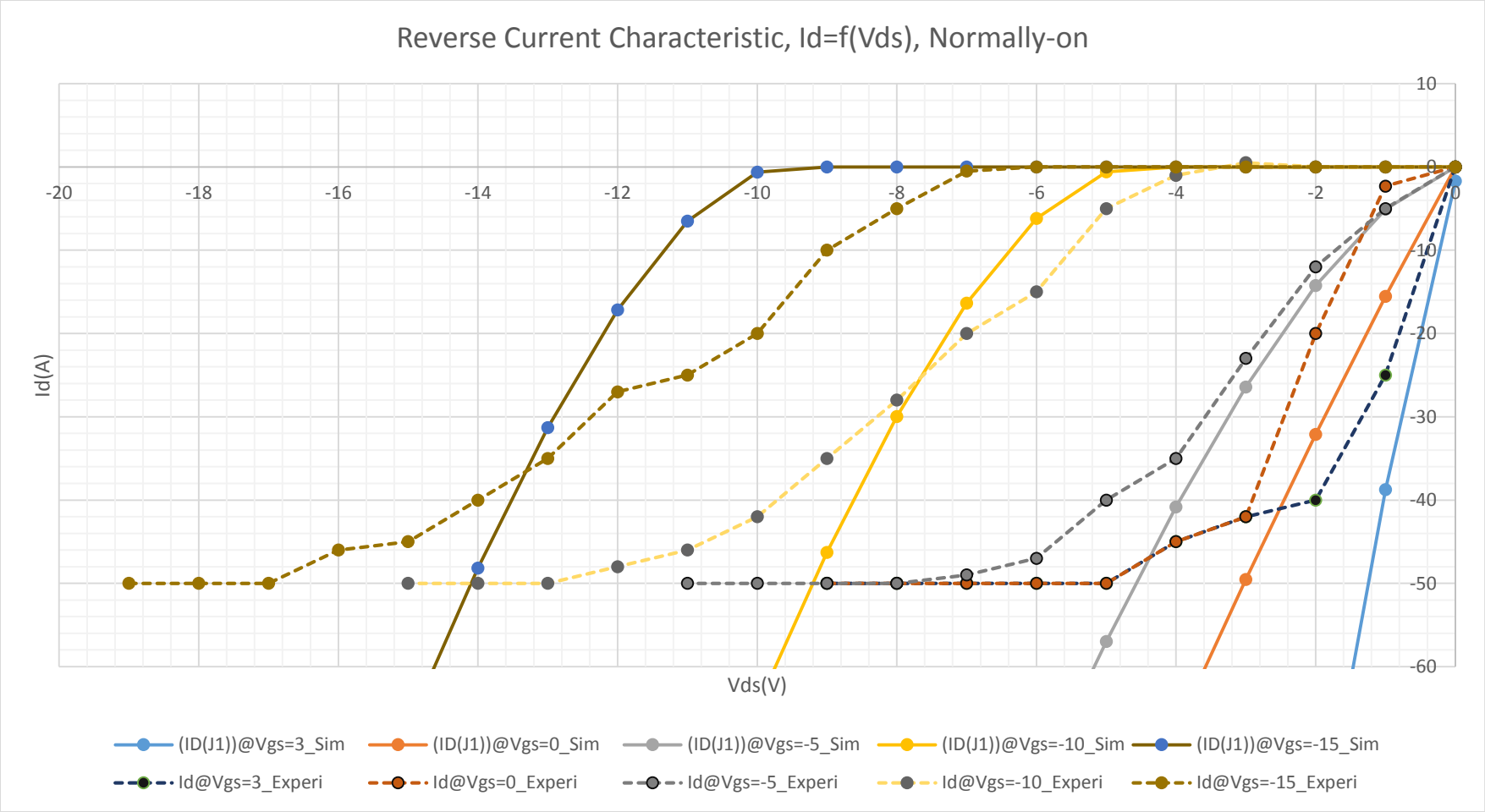


Figure 48. Reverse-current characteristic comparison. The ones with the dashed lines are the experimental and the solid are the simulated values.

2.7.3 *Spice Model for the SiC Power Schottky Diode SDP30S120*

The diode is modeled as an ohmic resistance (RS) in series with an intrinsic diode. Positive current is current flowing from the anode through the diode to the cathode.

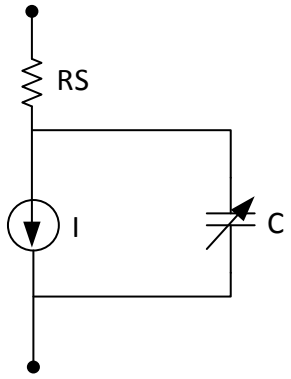


Figure 49. Electrical equivalent for Diode.

The diode model parameters which we have to define are the following.

Model parameters	Description	Units	SDP30S120
N	gate p-n emission coefficient		0.96
IS	gate p-n saturation current	amp	1e-014
RS	source ohmic resistance	ohm	0.024
IKF	high-injection knee current	A	0
XTI	IS temperature coefficient		3
EG	Bandgap voltage	eV	3.26
CJO	Zero-bias p-n capacitance	farad	3.5e-009
M	gate p-n grading coefficient		0.333
VJ	Voltage drop	V	0.75

FC	forward-bias depletion capacitance coefficient		0.5
ISR	gate p-n recombination current parameter	amp	1e-10
NR	emission coefficient for isr		2
BV	Blocking voltage	V	1200
IBV	Reverse breakdown knee current	A	0.0001
TT	Transit time	sec	5e-009

All these parameters are used by SPICE to describe the behaviour of the diode in different situations of signal. For the creation of the model we will be based on the datasheet plots because of lack of experimental measurements. Next a brief summary of the computation of these values is given.

Forward current will be:

$$I_D = I_S e^{\frac{V_D}{N \times V_t} - 1} \qquad (27)$$

where V_D is the forward voltage, $V_t = k \times \frac{T}{q}$ is the thermal voltage equal to 0.026 V at 27 degrees Celsius.
The so-called recombination current is calculated as

$$I_{rec} = I_{SR} e^{\frac{V_D}{N \times V_t} - 1} \qquad (28)$$

- Usually *IBV* is taken as equal to 10 times I_r which means ~1mA for room temperature.
- *CJO* can be directly equal to the value specified in the datasheet as C_{tot}=106pF (at 600V).
- Schottky diodes have a coefficient *M*, which typically varies from 0.3 to 0.5. In this case M= 0.33.
- The *TT* time in the case of ultrafast diodes rectifiers is up to 50ns, while for a fast rectifiers up to 250ns. This value is not given in the datasheet and it is determined after simulations.
- For *EG*, the standard value for Silicon is 1.1 eV, while it's 0.7 eV for Schottky diode and 0.67 eV for germanium diodes. For Silicon Carbide, it is 3.26 [chapter 1].
- The *N* value ranges between 1.0 and about 2.0. We extract it from the I-V characteristic.

- To determine *IS* and *RS*, we need the forward I-V characteristic curve and the eq. 27. We can estimate *RS* as voltage difference on the I-V characteristic at the point of the knee of the curve divided by the corresponding current.
- Finally, the *VJ*, voltage drop, is equal to 0.7V.

It is noted that as before we don't concern for the temperature coefficients. The omitted parameters are taken with the default values.

2.7.4 *Evaluation of the SiC Diode*

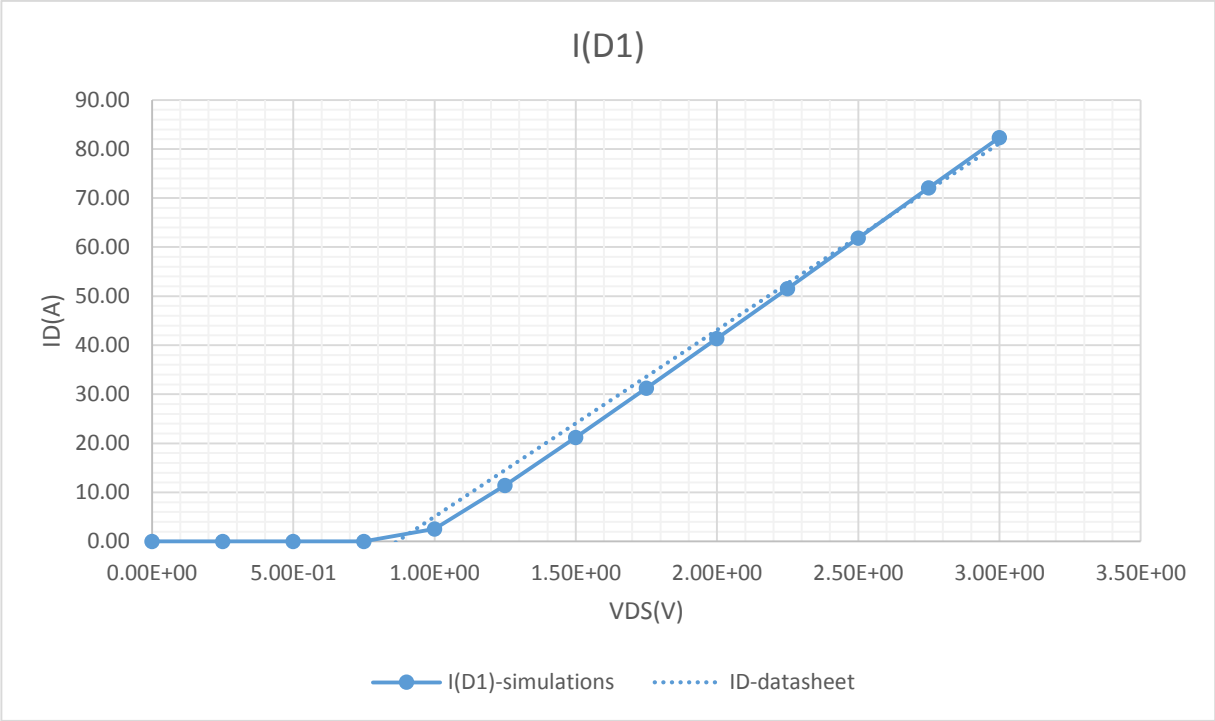


Figure 50. $V_{DS}=f(I_D)$

It is shown that the model approaches the real values and hence we can use it in circuits reliably.

2.7.5 *Conclusions*

This work presents the SPICE model of high voltage SiC JFET. Based on both static and dynamic characterizations, model for a 1200V, 27A DM SJDP120R085 and 1200V, 27A EM SJEP120R100 SiC JFET is made for power system simulations. Besides intrinsic model parameters, extrinsic components are also considered for accurate modeling. Reasonably good agreement is obtained between the modeled and experiment results of the device.

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Chapter 3

GATE DRIVING TECHNIQUES FOR SILICON-CARBIDE JFETs

Over the last years, more and more *Silicon Carbide (SiC)* power semiconductor switches have become available in order to prove their superior behavior. In the previous chapters it has been explained that new silicon carbide power semiconductors are characterized by outstanding performance concerning voltage blocking capability, on-state voltage drop, switching speed, and thermal resistance. To fully exploit the potential of the *SiC JFET*, conventional gate drivers for unipolar devices must be adapted to this device due to its special requirements. This device makes special demands on the gate driver circuit compared to other unipolar *SiC* or *Si* devices. Transition speed, turn-on and turn-off times, of the *SiC JFET* are ultimately limited by the device; however, the performance of the gate driver can impact this speed considerably. The pinch-off voltage and the reverse breakdown voltage of the gates seem to be the most important parameters which affect the switching performance of the devices. In particular, the spread in these two parameters might affect the stable off-state operation of the switches.

Its inherent fast switching speed has made it the preferred choice for high switching frequency, high power density applications [16–19] and has posited significant challenges to design engineers due to the very high *dv/dt* and *di/dt* rates that can be achieved by this device. The need to develop suitable gate drives in pursue of the full utilization of the *SiC JFET* high speed capabilities has hence become apparent, where the major obstacle faced has been the parasitic components in both circuit layout [20], and the device itself [21], [22]. These have limited the maximum switching speed due to the increase in dynamic losses associated to excessive drain-source current and voltage overshoots [16], [22], [23], due to the high *dv/dt* rate and excessive ringing on the gate-source loop. To tackle this problem, several contributions have been presented in an effort to deal with the increased dynamic interactions and design challenges posed by the *SiC JFET*. Several concepts for adapted gate drivers have been presented in the literature. The most prominent ones have been: [28], which proposed to drive the device with a negative bias close to its breakdown value using

an auxiliary circuit; [29], which proposed a simplified gate-drive version using a parallel resistor capacitor-diode (R-C-D) network—replacing the auxiliary circuit; [30], which showed that an RCD network could increase the switching speed of the *JFET* as the voltage across the capacitor forward biased the gate-source junction of the device; [24], which developed the gate-drive taking advantage of the reverse conducting capability of the *JFET* to eliminate the anti-parallel freewheeling diode from the circuit as proposed in [22]. Some still have certain limitations, with respect to switching frequencies and possible duty cycles, and some are very complex solutions with the need for several integrated circuits, their own DC/DC converters or additional cooling due to high gate driver losses [4]–[11]. Along these lines, the goal of this work has been to develop a gate-drive circuit for the normally-on (SJDP120R085) and normally-off (SJEP120R100) 1.2 kV *SiC JFET* produced by Semisouth, pursuing ultimately to determine the maximum switching capability of this device, but also focusing on developing a high *dv/dt* and *di/dt* design methodology for the gate-drive circuit.

For these reasons, in this chapter novel gate driver topologies [1], [31] are presented and compared both for normally-on and normally-off *SiC JFETs* that overcome the current limitations while still having a low circuit complexity using one or two gate driver IC and passive components only. By introducing inherently safe gate driver circuits specially designed for the *SiC JFET*, it will be possible to prove that designing applications using *SiC JFETs* is not as complicated as some may think. First, the typical switching equations, based on those developed by B. J. Baliga [53], for a *SiC JFET* are described, along with the special gate driver requirements of the *SiC JFETs* in detail together with their causes in order to reveal the differences to driving conventional power semiconductors. In addition, the classic RCD topology is introduced which is compared with the two new ones (ac-coupled and dc-coupled) developed for the *SiC* devices. Simulation and experimental results applied on a double pulse tester are presented in order to evaluate the driving techniques on the *SiC JFET*.

3.1 Principles of gate driving a Vertical Trench SiC JFET

This section defines the fundamental behavior of a *SiC JFET*. In [32], [33], [53] the main switching principles for a semiconductor are described while in this paragraph they are used for the analysis of a Silicon Carbide JFET in *JFET – snubber (J-S)* system. It is then used to study the effects of the stray inductances, gate drive resistance and snubber on the switching behaviors, power loss distribution, and voltage stress on the semiconductor in the entire *J-S* system configuration. A sequence of steps will be given to illustrate how an optimal combination of the gate drive resistance and snubber capacitance is determined, in order to minimize the overall loss of the configuration for a maximum permissible voltage stress on the device. The loss model and method of determining the gate drive resistance and snubber

capacitance are evaluated by comparing the theoretical predictions with the experimental results of a double pulse tester with 200V, 4A test bench.

3.1.1 Switching the SiC JFET in isolation

To get a fundamental understanding of the switching behavior of a *JFET*, it is best first to consider the device in isolation and without any external influences. Under these conditions, an equivalent circuit of the *JFET* gate is illustrated in *Figure 51*, where the gate consists of an internal gate resistance (R_g), and two input capacitors (C_{gs} and C_{gd}). With this simple equivalent circuit it is possible to obtain the output voltage response for a step gate voltage.

The voltage V_{GS} is the actual voltage at the gate of the device, and it is this point that should be considered when analyzing the switching behavior of the device.

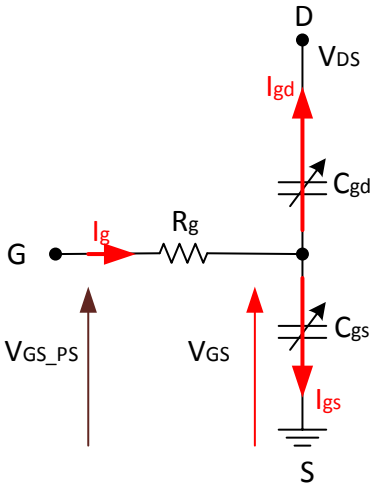


Figure 51. An equivalent JFET gate circuit showing just the Cgs, Cgd and Rg.

If a step input is applied at V_{GS_PS}, then the following holds true:

$$i_{gs} = \frac{V_{GS\_PS} - V_{GS}}{R_g} \qquad (1)$$

$$i_g = i_{gs} + i_{gd} \qquad (2)$$

$$i_{gs} = C_{gs}\frac{dV_{GS}}{dt} \qquad (3)$$

$$i_{gd} = C_{gd}\frac{dV_{GD}}{dt} \xrightarrow{V_{GD}=V_{GS}+V_{SD}} i_{gd} = C_{gd}\frac{d(V_{GS}-V_{DS})}{dt} \xrightarrow{V_{DS}\to fixed} i_{gd} = C_{gd}\frac{dV_{GS}}{dt} \qquad (4)$$

Therefore

$$\frac{V_{GS\_PS} - V_{GS}}{R_g} = C_{gs}\frac{dV_{GS}}{dt} + C_{gd}\frac{dV_{GS}}{dt} \qquad (5)$$

And

$$\frac{dV_{GS}}{V_{GS\_PS} - V_{GS}} = \frac{dt}{(C_{gs} + C_{gd})R_g} \qquad (6)$$

Giving

$$-\ln\left(V_{GS\_PS} - V_{GS}\right) = \frac{t}{\left(C_{gs} + C_{gd}\right)R_g} + k \qquad (7)$$

$$V_{GS} = V_{GS\_PS} - ke^{-\frac{t}{(C_{gs}+C_{gd})R_g}} \qquad (8)$$

at t=0, $V_{GS} = -15\ V$, therefore

$$V_{GS} = V_{GS\_PS} - (V_{GS\_PS} + 15)\, e^{-\frac{t}{(C_{gs}+C_{gd})R_g}} \qquad (9)$$

This gives an indication of how long the actual gate voltage (V_{GS}) takes to get to the threshold voltage. For illustration purposes, a more practical circuit is shown in Figure 52, where an additional resistance is placed between V_{DS} and C_{gd}. In this instance, the step response gets very complicated and the equation (equation 10) becomes very difficult to solve.

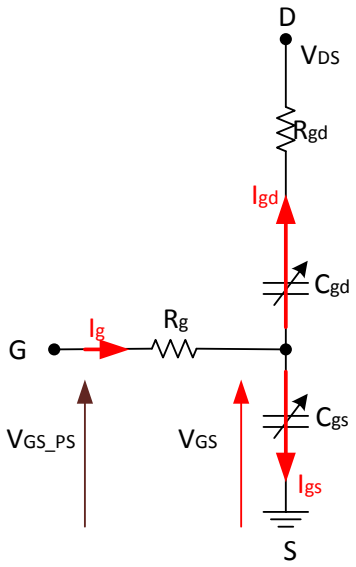


Figure 52. An equivalent JFET gate circuit showing just the Cgs, Cgd and Rg plus Rgd.

$$V_{GS} = V_{GS\_PS} - \frac{V_{GS\_PS}}{2\sqrt{k}}(A - B) \qquad (10)$$

Where

$$A = \left[\left(CR_k + \sqrt{k}\right)e - \frac{t(CR - \sqrt{k})}{2C_{gd}R_{gd}C_{gs}R_g}\right] \qquad (11)$$

$$B = \left[\left(CR_k - \sqrt{k}\right)e - \frac{t(CR + \sqrt{k})}{2C_{gd}R_{gd}C_{gs}R_g}\right] \qquad (12)$$

$$CR_k = C_{gs}R_g + C_{gd}R_g + C_{gd}R_{gd} \qquad (13)$$

and

$$k = C_{gs}^2R_g^2 + 2C_{gs}R_g^2C_{gd} - 2C_{gd}R_{gd}C_{gs}R_g + C_{gd}^2R_g^2 + 2C_{gd}^2R_{gd}R_g + C_{gd}^2R_{gd}^2 \qquad (14)$$

Investigating and plotting the equations 9 and 10 (Figure 53, Figure 54) shows that there is only a minor time difference (about a 1ns) in the time the gate voltage takes to get to the threshold voltage. Therefore it can be argued that to adopt the less complex approach does not impinge significantly on the accuracy of the gate voltage transient. However, the point has been made that any calculated switching times will be less than the actual transients seen by the *SiC JFET*. As shown above, when the device is considered with additional parasitics, it

becomes increasingly difficult to manipulate these equations manually for such a practical circuit. Therefore a method of analysing a practical circuit is required. If these second order, or parasitic, components are ignored, then it is possible to come up with formulas for the turn-on and turn-off time periods.

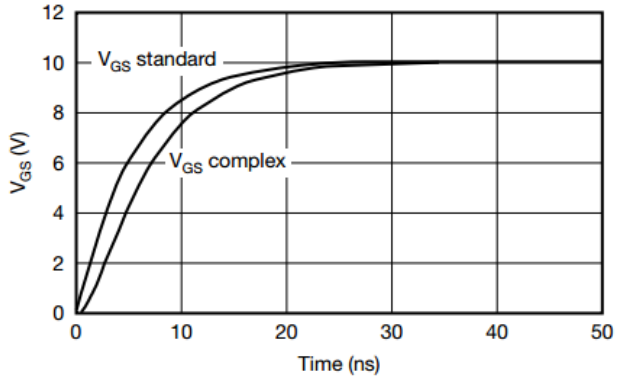


Figure 53. Graph plots for equation 9 (standard) and 10 (complex).

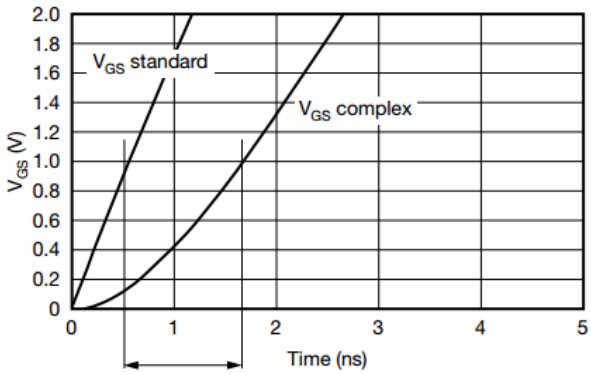


Figure 54. Graph plots in zoom for equation 9 (standard) and 10 (complex).

Consequently, in the following of the section the simple electrical scheme of the device is adopted while it is analysed in a classical *JFET-snubber (J-S)* application in order to investigate further the switching times and losses in a gate driving circuit.

3.1.2 Switching the SiC JFET in a JFET-snubber configuration

In reality, stray inductances cannot be totally eliminated and become especially important in determining the performance in high-frequency operation. In high-frequency applications, the stray inductances introduce an important concern of high voltage stress on the switching device. Thus, the faster the *JFET* is turned OFF, the higher the voltage induced across the stray inductances will be, resulting in a high voltage stress across the *JFET*.

It is shown in [33] and in chapter 4 that a voltage stress of 25% higher than its OFF-state voltage can be induced across the *JFET* if no snubber circuit is used. When the applied voltage stress exceeds the inherent capability of the switching device, either degradation or a failure will be precipitated. Besides, such a high $\frac{dv}{dt}$ effect will also generate electromagnetic interference. To assure system reliability, the driving and the main circuit must be carefully designed.

The voltage induced across the stray inductances can be limited by reducing the value of the stray inductances. Although the inductances from the internal bonding wire and external leads of the *JFET* and other electronic components cannot be changed, the PCB layout and

copper thickness can be designed to minimize the stray inductances. However, certain amount of stray inductances is unavoidable. When the switching speed is increased, the voltage stress problem will still exist. A direct solution to tackle the voltage stress problem is to select a *JFET* of higher voltage rating, but the cost of high voltage *JFETs* is generally higher than that of the low voltage ones.

A more practical solution is to connect a simple RC snubber, resistor–capacitor (RC) snubber across the *JFET* to limit the rate of change of the drain current and, thus, reduce the voltage induced by the stray inductances. This will then reduce the voltage stress on the *JFET*. Therefore the entire switching unit should have the snubber included, namely *JFET–snubber (J-S)* configuration. Its performance should be evaluated by considering the loss distribution in the entire configuration and the voltage stress on the *JFET*.

Based on the derived loss model, a sequence of steps will be given to illustrate how an optimal value of the gate drive resistance is determined, in order to minimize the overall loss of the *J-S* configuration, while the voltage stress on the *JFET* is within the permissible range.

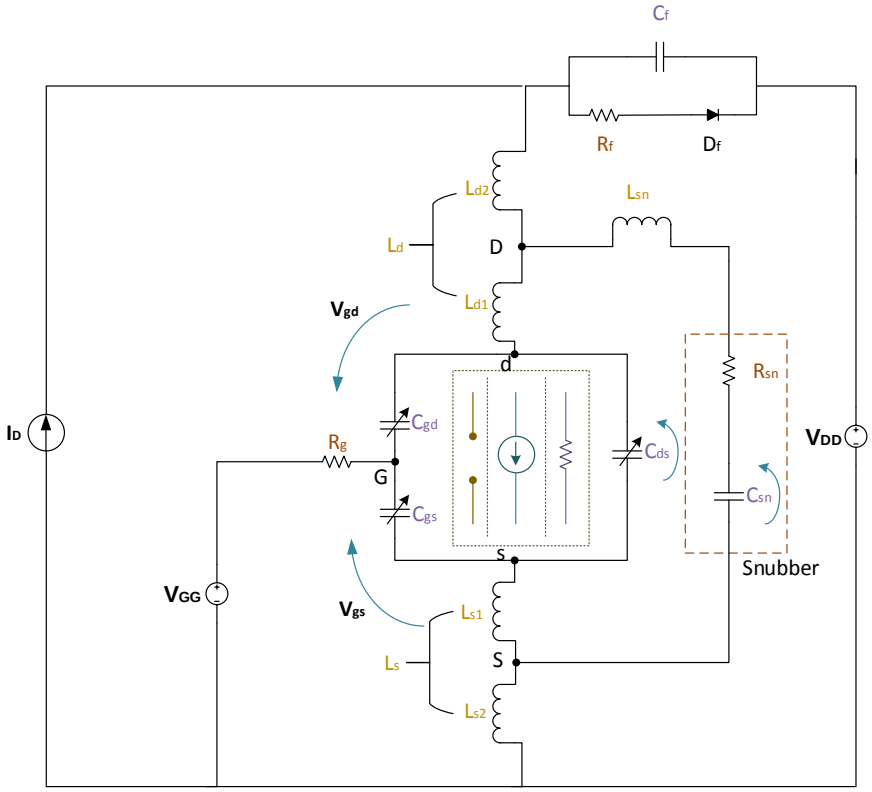


Figure 55. Typical inductive-switching circuit: a JFET-snubber configuration.

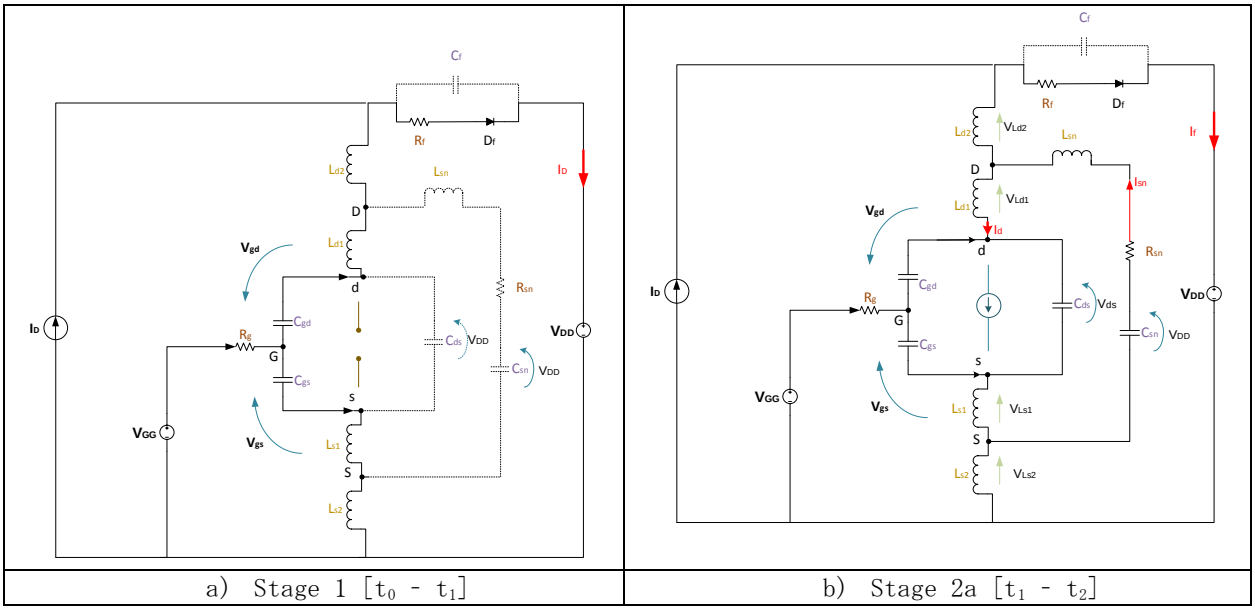
The snubber is of *Resistor-Capacitor (RC)*[1] type, which is widely adopted in many industrial applications. Critical parasitic elements that are considered in the *JFET* model include gate–source capacitance C_{gs}, gate–drain capacitance C_{gd}, drain–source capacitance C_{ds}, source

[1] Further details on the choice and the techniques of the snubber circuits for our application in order to minimize the voltage stress on the semiconductor may be found in chapter 4.

inductance L_{s1}, and drain inductance L_{d1} . $C_{iss} = C_{gs} + C_{gd}$ and $C_{oss} = C_{ds} + C_{gd}$ are denoted as the input and output capacitances of the *JFET*, respectively. In some cases when the gate drive is strong, the gate inductance L_g and the input capacitance C_{iss} can cause undesired oscillation. However, as the gate drive resistance R_g limits the gate current as well as its slew rate, the effect of L_g can be neglected and is not considered in this chapter. All stray inductances in the power loop and external to the *JFET* are lumped and represented by L_{s2} and L_{d2}, which are at the source and drain terminal of the *JFET*, respectively. $L_s = L_{s1} + L_{s2}$ and $L_d = L_{d1} + L_{d2}$ are denoted as the total inductances at the source and drain terminals of the *JFET*, respectively.

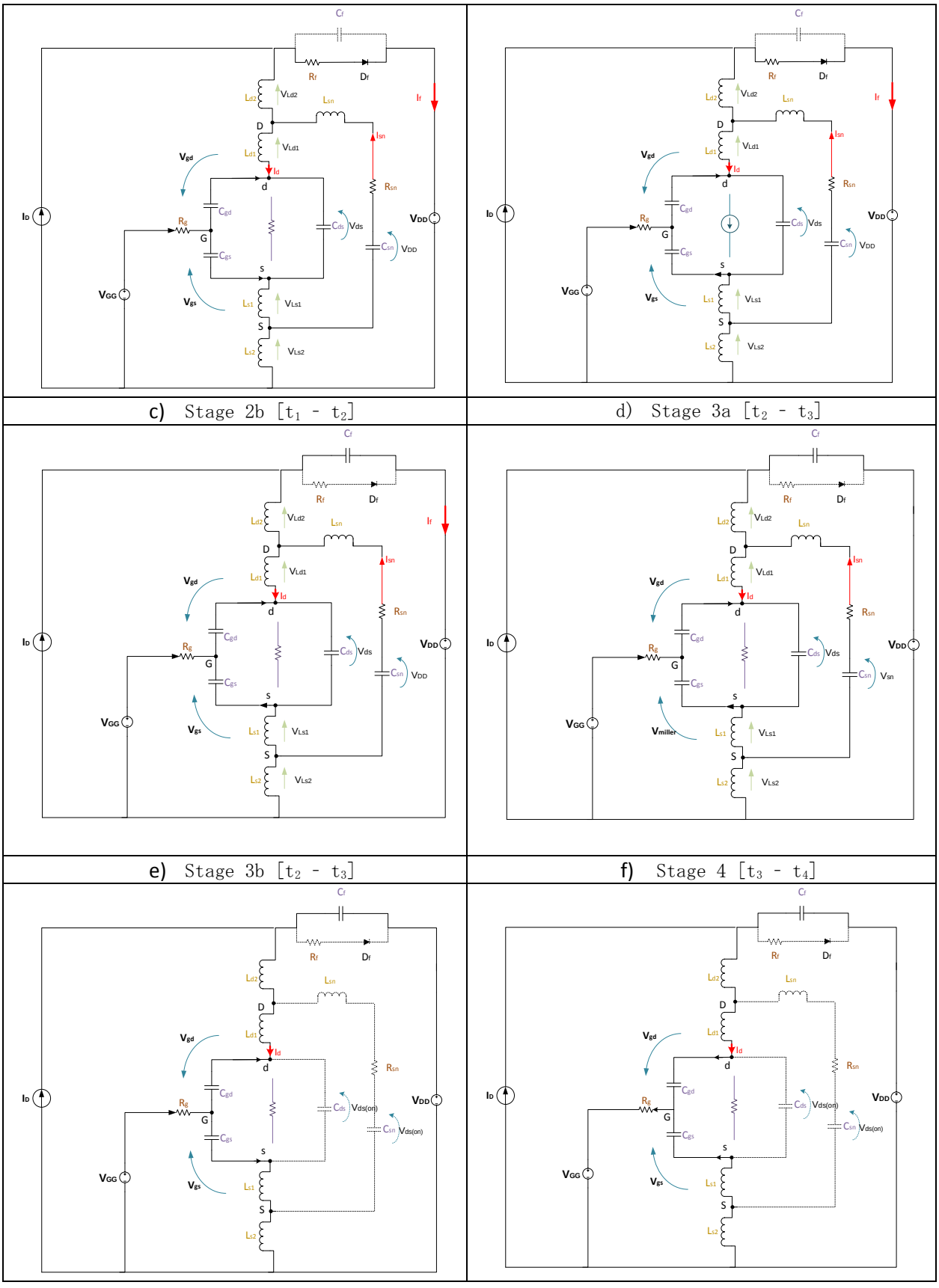
The function of the *RC* snubber is to alleviate voltage stress of the *JFET*. The snubber capacitor will discharge down through the snubber resistor at turn-ON in order to be effective at the next turn-OFF. Such a discharging current will incur extra current stress on the *JFET*. The voltage across the snubber capacitor V_{sn} is assumed to stay constant at the output voltage V_{DD} before the drain–source voltage drops to a low level so as to simplify the analysis. It is a reasonable assumption in that the time constant $R_{sn}C_{sn}$ of the snubber circuit is far larger than the switching time of the *JFET*. The inductance L_{sn} represents the stray inductance associated in the snubber circuit. However, it can be neglected in the analysis for the sake of simplicity. Figure 56 (a)–(g) and (h)–(l) shows the stages in the turn-ON and turn-OFF transitions, respectively. Figure 57 and Figure 58 illustrate the turn-ON and turn-OFF timing diagram of the switching transients.

The purpose on the following analysis is to extract the drain current equations as well as the snubber and diode behavior and show the procedure during the transitions to the various stages of Figure 57 and Figure 58.



a) Stage 1 [t_0 - t_1]

b) Stage 2a [t_1 - t_2]



c) Stage 2b [t_1 - t_2]

d) Stage 3a [t_2 - t_3]

e) Stage 3b [t_2 - t_3]

f) Stage 4 [t_3 - t_4]

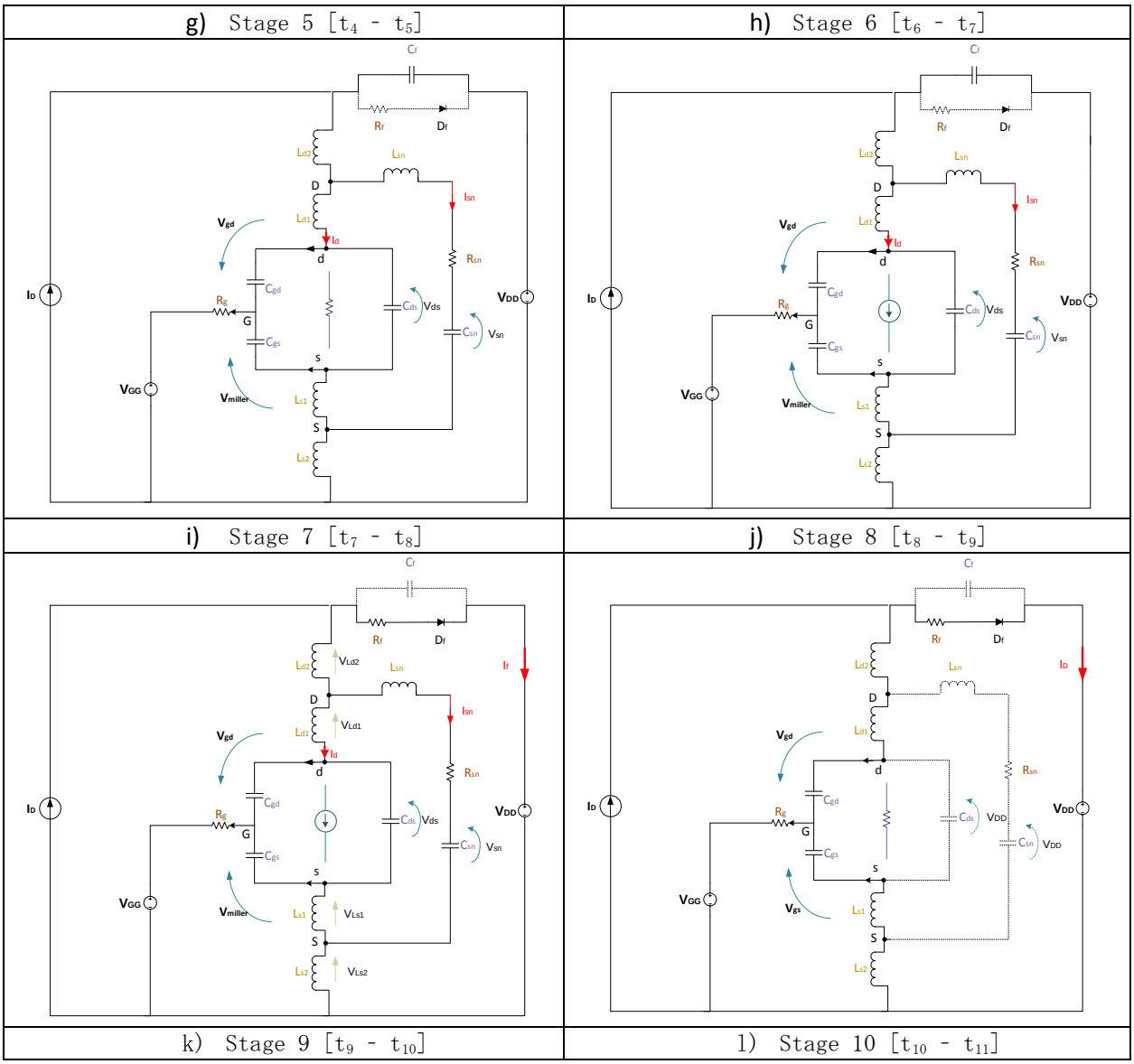


Figure 56. Operating modes of the J-S configuration. (a) Stage 1 [t_0 –t_1], (b) Stage 2a [t_1 –t_2], (c) Stage 2b [t_1 –t_2], (d) Stage 3a [t_2 –t_3], (e) Stage 3b [t_2 –t_3], (f) Stage 4 [t_3 –t_4], (g) Stage 5 [t_4 –t_5], (h) Stage 6 [t_6 –t_7], (i) Stage 7 [t_7 –t_8], (j) Stage 8 [t_8 –t_9], (k) Stage 9 [t_9 –t_{10}], (l) Stage 10 [t_{10} –t_{11}].

Turn-on Switching Transients

Stage 1 [t_0–t_1], turn-ON delay time: When a gate signal V_{GG} is applied to the *JFET* through the gate drive resistance R_g , the input capacitance C_{gs} and C_{gd} are charged up. The *JFET* will not leave the cut-off region until v_{gs} reaches the threshold voltage V_{th}, thus the input reverse current still circulates through a freewheeling diode D_f or the body of the *JFET* as explained in chapter 2. The gate–source voltage as explained before with the simplified model is given by

$$V_{GS} = V_{GG} - (V_{GG} + 15)\, e^{-\frac{t-t_0}{(C_{gs}+C_{gd})R_g}} \qquad (15)$$

Stage 2 [t_1–t_2], in this stage, v_{gs} goes beyond V_{th} and the drain current i_d starts to increase from zero to its peak value I_{d_peak} which is larger than the input current I_D. The rise in V_{GS} during t_2 (Figure 57) is brought about by charging C_{gs}. During the time period [t_0–t_2] V_{DS} does not change very much and as such C_{gd} and C_{ds} stay relatively constant, since they vary as a function of V_{DS}. At this time C_{gs} is generally larger than C_{gd} and therefore the majority of drive current flows into C_{gs} rather than into C_{gd}. This current, through C_{gd} and C_{ds}, depends on the time derivative of the product of the capacitance and its voltage. The gate charge can therefore be assumed to be Q_{gs}.

The portion that exceeds I_D is contributed by the reverse current of the *JFET* channel and the snubber discharging current. In the case that no reverse diode is used, the plots are quite worse since the reverse current and the reverse recovery time of the *SiC JFET* channel are significant larger. Due to the $L\frac{di}{dt}$ effect, the drain–source voltage v_{ds} decreases by $v_{Ls} + v_{Ld}$, which is the voltage drop induced by the rising drain current across the inductances L_s (v_{Ls}) and L_d (v_{Ld}). This voltage drop $v_{Ls} + v_{Ld}$, defined by the parasitic inductances, deserves special attention, as it determines whether v_{ds} will drop to $v_{gs} - V_{th}$ before or after i_d rises to its full value I_D. As $v_{gs} - V_{th}$ is the boundary condition for the *JFET* to switch into the ohmic region, it can further determine the operating mode of the *JFET* in this and the following stages. This can be seen in *Figure 56*, stage 2a and 2b where in the first one the JFET will operate in its saturation region and in the second one in its ohmic region.

Equations in the saturation region

If the *JFET* works in the saturation region, i_d is governed by

$$i_d(t) = g_{fs}[v_{gs}(t) - V_{th}] \qquad (16)$$

where g_{fs} is the transconductance of the *JFET* which is used here for the sake of simplicity on the premise that the current through the parasitic capacitors C_{ds} and C_{gd} are negligible compared to the input current. Due to the $L\frac{di}{dt}$ effect, a voltage drop v_{Ls} is generated across the source inductance L_s , which counteracts the gate– source voltage v_{gs}. During this period, the drain current is assumed to be increasing at a constant rate $\frac{di}{dt}$ and v_{Ls} stays constant at $L_s\frac{di}{dt}$. The circuit equations can be expressed as

$$R_g i_g(t) = V_{GG} - v_{gs}(t) - L_s\frac{di_d}{dt} \qquad (17)$$

$$i_g(t) = C_{gs}\frac{dv_{gs}(t)}{dt} + C_{gd}\frac{dv_{gd}(t)}{dt} \qquad (18)$$

$$v_{gs}(t) = v_{gd}(t) + v_{ds}(t) \qquad (19)$$

$$v_{ds}(t) = V_{DD} - (L_s + L_d)\frac{di_d}{dt} \qquad (20)$$

By performing the Laplace transformation of (16)–(19), $v_{gs}(s)$ is expressed as

$$v_{gs}(s) = \frac{V_{GG}(s)}{\tau_m^2 s^2 + \tau_n s + 1} \qquad (21)$$

Where

$$\tau_m^2 = R_g C_{gd} g_{fs}(L_s + L_d) \qquad (22)$$

$$\tau_n = R_g\left(C_{gd} + C_{gs}\right) + g_{fs}L_s \qquad (23)$$

If $\tau_n^2 > 4\tau_m^2$, v_{gs} will increase according to

$$v_{gs}(t) = V_{GG} - \frac{V_{GG} - V_{th}}{\tau_a - \tau_b}\left(\tau_a e^{-\frac{t-t_1}{\tau_a}} - \tau_b e^{-\frac{t-t_1}{\tau_b}}\right) \qquad (24)$$

Where $\tau_a = \frac{\left(\tau_n + \sqrt{\tau_n^2 - 4\tau_m^2}\right)}{2}$, $\tau_b = \frac{\left(\tau_n - \sqrt{\tau_n^2 - 4\tau_m^2}\right)}{2}$

If $\tau_n^2 > 4\tau_m^2$, v_{gs} will increase according to

$$v_{gs} = V_{GG} - (V_{GG} - V_{th})e^{-\frac{t-t_1}{\tau_e}} \times \left(\frac{\tau_d}{\tau_c} sin\frac{t-t_1}{\tau_d} + cos\frac{t-t_1}{\tau_d}\right) \qquad (25)$$

Where $\tau_c = 2\frac{\tau_m^2}{\tau_n}$, $\tau_n = 2\frac{\tau_m^2}{\sqrt{4\tau_m^2 - \tau_n^2}}$

Now that v_{gs} is obtained, i_d can be given according to (16).

Accordingly the average current slew rate $\frac{di_d}{dt}$ is determined as

$$\frac{di_d}{dt} = \frac{I_D}{t_{r\_a}} \qquad (26)$$

v_{ds} in this stage can be given by

$$v_{ds}(t) = V_{DD} - (L_s + L_d)\frac{di_d}{dt} = V_{DD} - \frac{I_D(L_s + L_d)}{t_{r\_a}} \qquad (27)$$

where t_{r_a} is the time duration when i_d increases from zero to I_D is intercepted and estimated by either (24) or (25), depending on whether $\tau_n^2 > 4\tau_m^2$ or not.

Equations in the ohmic region

If the *JFET* works in ohmic region, the drain current will increase at a rate dependent on the stray inductances in the circuit instead of on the gate–source voltage. Assume v_{ds} is much smaller than V_{DD} and can be neglected. With V_{DD} entirely dropping on L_s and L_d, the drain current will rise at a constant rate

$$\frac{di_d}{dt} = \frac{V_{DD}}{L_s + L_d} \qquad (28)$$

The drain current i_d and the time duration of this stage can be approximated by

$$i_d(t) = \frac{V_{DD}}{L_s + L_d}\,(t - t_1) \qquad (29)$$

Snubber and diode behavior

Considering the snubber circuit, the snubber capacitor voltages v_{sn} and v_{ds} remain constant at V_{DD}, the discharging current of the snubber capacitor i_{sn} is given by

$$i_{sn} = \frac{v_{sn} - v_{ds} - v_{Ls1} - v_{Ld1}}{R_{sn}} = \frac{L_{s2} + L_{d2}}{R_{sn}}\frac{di_d}{dt} \qquad (30)$$

where v_{Ls1} and v_{Ld1} are voltage drop across L_{s1} and L_{d1} , respectively. The effect of the snubber inductance L_{sn} is neglected in the calculation as the time constant formed by L_{sn} and R_{sn}, which is equal to L_{sn}/R_{sn} , is very small. Due to the existence of i_{sn}, the current flowing through the diode/body channel of *JFET* i_f is

$$i_f = I_D - i_d + i_{sn} = I_D - \frac{di_d}{dt}(t - t_1) + \frac{L_{s2} + L_{d2}}{R_{sn}}\frac{di_d}{dt} \qquad (31)$$

In (30) and (31), if the *JFET* works in saturation region, $\frac{di_d}{dt}$ is given by (26), otherwise, by (28).

Once i_f reaches zero, the diode current will reverse its polarity and start the reverse recovery process, which will result in a corresponding change in the drain current of the JFET. Even if the silicon carbide (*SiC*) diode nearly features non reverse recovery charge, its junction capacitance will also introduce reverse current. The diode current and referring to the definition of such parameters, reverse recovery time t_{rr} , maximum reverse current $I_{rr,max}$, reverse recovery charge Q_{rr} , and snappiness factor S can be given by

$$t_{rr} \qquad (32)$$

$$I_{rr,max} = \left|\frac{di_{f\_1}}{dt}\right| t_{rr} \qquad (33)$$

$$Q_{rr} = \frac{1}{2} I_{rr,max} t_{rr} \qquad (34)$$

So, t_{rr} and $I_{rr,max}$ are

$$t_{rr} = \sqrt{\frac{2Q_{rr}t_{rr}(S+1)}{I_D}} \qquad (35)$$

$$I_{rr,max} = \sqrt{\frac{2Q_{rr}I_D}{(S+1)t_{rr}}} \qquad (36)$$

The peak value of the drain current I_{d_peak} can be determined

$$I_{d,peak} = I_D + I_{rr,max} + I_{sn} = I_D + \sqrt{\frac{2Q_{rr}I_D}{(S+1)t_r}} + \frac{L_{s2} + L_{d2}}{R_{sn}} \frac{I_D}{t_{rr}} \qquad (37)$$

If the *JFET* works in saturation region, v_{gs} will go higher than V_{miller} . V_{gs_peak} that is in accordance with I_{d_peak} can be given by

$$V_{gs\_peak} = \frac{I_{d,peak}}{g_{fs}} + V_{th} \qquad (38)$$

Stage 3 [t_2–t_3], the next part of the waveform [t_2–t_4] is the Miller Plateau. It is generally accepted that this point, [t_2–t_3], at which the gate charge figure goes into the plateau region coincides with the peak value of the peak current. However, the knee in the gate charge actually depends on the product ($C_{gd}V_{GD}$) with respect to time. This means if there is a small value of drain current and large value of output impedance, then I_D can actually reach its maximum value after the left knee of the gate voltage occurs.

In this stage, the freewheeling diode current i_f returns to zero from $I_{rr,max}$ and begins to go to the blocking state; therefore, i_d and v_{ds} simultaneously start to decrease.

Equations in the saturation region

If stage 2a is the case for the previous stage, v_{ds} will resume decrease in the saturation region and, thus, the snubber discharging current will no longer stay constant. By applying Kirchhoff's Current and Voltage Law for the snubber, the following equation can be derived:

$$R_{sn}i_{sn}(t) = V_{DD} - (L_{s1} + L_{d1})\frac{di_d}{dt} - v_{ds}(t) \qquad (39)$$

After mathematical manipulation combined with [16], [19]

$$v_{gs}(s) = \frac{V_{GG}(s)}{\tau_q^2 s^2 + \tau_q s + 1} \qquad (40)$$

Where

$$\tau_p^2 = R_g C_{gd} g_{fs}(L_{1s} + L_{d1}) \qquad (41)$$

$$\tau_q = \left[\left(C_{gd} + C_{gs}\right) + g_{fs}R_{sn}C_{gd}\right]R_g + g_{fs}L_{s1} \qquad (42)$$

If $\tau_q^2 < 4\tau_p^2$, v_{gs} will decrease as

$$v_{gs}(t) = V_{gs\_peak}\left[1 - e^{-\frac{t-t_2}{\tau_e}}\left(\frac{\tau_f}{\tau_e}sin\frac{t-t_2}{\tau_f} + cos\frac{t-t_2}{\tau_f}\right)\right] \qquad (43)$$

Where $\tau_e = \frac{2\tau_p^2}{\tau_q}$, $\tau_f = \frac{2\tau_p^2}{\sqrt{4\tau_p^2 - \tau_q^2}}$

If $\tau_q^2 > 4\tau_p^2$, v_{gs} and i_d can be derived

$$v_{gs}(t) = \frac{V_{gs\_peak}}{\tau_g - \tau_h}\left(\tau_g e^{-\frac{t-t_2}{\tau_g}} - \tau_h e^{-\frac{t-t_2}{\tau_h}}\right) \qquad (44)$$

$$i_d(t) = g_{fs}\left[\frac{V_{gs\_peak}}{\tau_g - \tau_h}\left(\tau_g e^{-\frac{t-t_2}{\tau_g}} - \tau_h e^{-\frac{t-t_2}{\tau_h}}\right) - V_{th}\right] \qquad (45)$$

Where $\tau_g = \frac{\left(\tau_q + \sqrt{\tau_q^2 - 4\tau_p^2}\right)}{2}$, $\tau_h = \frac{\left(\tau_q - \sqrt{\tau_q^2 - 4\tau_p^2}\right)}{2}$

As determined by the parameters, normally $\tau_q^2 > 4\tau_p^2$ will be the case, it is considered for the following analysis. Linearizing drain current using the same method as in stage 2

$$\frac{di_d}{dt} = -\frac{I_{d\_peak} - I_D}{t_d} \qquad (46)$$

$$i_d(t) = I_{d_{peak}} + \frac{di_d}{dt}(t - t_2) \qquad (47)$$

where I_{d_peak} is given by (37), and t_d , which is the time duration for i_d to decrease from I_{d_peak} to I_D is estimated by (43). Further calculation gives the result

$$\frac{dv_{ds}}{dt} = -R_{sn}\left(\frac{di_d}{dt} + \frac{di_f}{dt}\right) = -R_{sn}\left(-\frac{I_{d_{peak}} - I_D}{t_d} + -\frac{I_D}{St_{r\_a}}\right) \qquad (48)$$

At the end of this stage, v_{ds} will fall to $V_{miller} - V_{th}$ and take next move to the ohmic region.

Equations in the ohmic region

If the previous stage is stage 2b, the JFET will still work in ohmic region with $v_{ds} = V_{ds(on)}$. The snubber discharging current is now given by

$$i_{sn}(t) = C_{sn}\frac{V_{DD} - V_{ds(on)}}{\tau_{sn}} e^{-\frac{(t-t_2)}{\tau_{sn}}} \qquad (49)$$

Where $\tau_{sn} = R_{sn}C_{sn}$

So the drain current will decrease according to

$$i_d(t) = I_{d,peak} - i_f + i_{sn} = I_{d,peak} - \frac{V_{DD}}{S(L_s + L_d)}(t - t_2) + C_{sn}\frac{V_{DD} - V_{ds(on)}}{\tau_{sn}} e^{-\frac{(t-t_2)}{\tau_{sn}}} \qquad (50)$$

In this case, the JFET will skip stage 4 and directly enter stage 5 after stage 3 finishes.

Stage 4 [t_3–t_4], the slope of the Miller Plateau is generally shown to have a zero, or a near-zero slope, but this gradient depends on the division of drive current between C_{gd} and C_{gs}. If the slope is non-zero then some of the drive current is flowing into C_{gs}. If the slope is zero then all the drive current is flowing into C_{gd}. This happens if the $C_{gd}V_{GD}$ product increases very quickly and all the drive current is being used to accommodate the change in voltage across C_{gd}. As such, Q_{gd} is the charge injected into the gate during the time the device is in the Miller Plateau. It should be noted that once the plateau is finished (when V_{DS} reaches its on-state value), C_{gd} becomes constant again and the bulk of the current flows into C_{gs} again. The gradient is not as steep as it was in the first period (t_2), because C_{gd} is much larger and closer in magnitude to that of C_{gs}.

Once v_{ds} reaches the boundary $v_{gs} - V_{th}$, the JFET will come out of the saturation region and go into the ohmic region. The drain current is no longer controlled by the gate–source voltage of the JFET. v_{gs} now changes sufficiently close to V_{miller} to allow the assumption that $v_{gs} = V_{miller}$. With C_{gd} turning into the smaller value $\frac{dv_{ds}}{dt}$ can be approximated as

$$\frac{dv_{ds}}{dt} = -\frac{V_{GG} - V_{miller}}{R_g C_{gd}} \qquad (51)$$

where $V_{miller} = I_D / g_{fs} + V_{th}$ is defined as the gate–source voltage when the drain current rises to its full value I_D. At the end of this stage, v_{ds} will arrive at its ON-state value $V_{ds(on)}$. In the previous stages, the voltage across the snubber capacitor is assumed to stay constant at V_{DD} so as to simplify the calculation. Since the variation in v_{ds} is quite small in this stage, the discharging process of the snubber circuit should be further considered

$$i_{sn} = -C_{sn}\frac{dv_{sn}}{dt} \qquad (52)$$

$$R_{sn} i_{sn}(t) = v_{sn} - \frac{di_d}{dt}(L_{s1} + L_{d1}) - V_{ds(on)} \qquad (53)$$

Formulating the characteristic equations using the Laplace transformed equations, $v_{sn}(s)$ can be obtained as

$$v_{sn}(s) = \frac{\left(V_{DD} - V_{ds(on)}\right)/s}{\tau_u^2 s^2 + \tau_v s + 1} \qquad (54)$$

Where $\tau_u^2 = (L_{s1} + L_{d1})C_{sn}$ and $\tau_v = R_{sn}C_{sn}$. Since $\tau_v^2 > 4\tau_u^2$ always holds, performing inverse Laplace transform, $v_{sn}(t)$ can be expressed as

$$v_{sn}(s) = V_{ds(on)} + \frac{\left(V_{DD} - V_{ds(on)}\right)}{\tau_i - \tau_j}\left(\tau_i e^{-\frac{(t-t_3)}{\tau_i}} - \tau_j e^{-\frac{(t-t_3)}{\tau_j}}\right) \qquad (55)$$

Where $\tau_i = \frac{\left(\tau_v + \sqrt{\tau_v^2 - 4\tau_u^2}\right)}{2}$, $\tau_j = \frac{\left(\tau_v - \sqrt{\tau_v^2 - 4\tau_u^2}\right)}{2}$ and i_d is given by

$$i_d(t) = I_D + C_{sn}\frac{\left(V_{DD} - V_{ds(on)}\right)}{\tau_i - \tau_j}\left(e^{-\frac{(t-t_3)}{\tau_j}} - e^{-\frac{(t-t_3)}{\tau_i}}\right) \qquad (56)$$

These two equations imply that the drain current will not reach its steady-state value until the snubber capacitor is fully discharged.

Stage 5 [t_4–t_5], ON-state operation: Once the discharging of the snubber capacitor finishes, i_d keeps constant at I_D and v_{ds} remains $V_{ds(on)}$. v_{gs} increases again so as to compensate the increase in negative voltage across C_{gd}. By KVL, $v_{gs} - v_{gd} = v_{ds}$. v_{gs} will reach V_{GG} at t_5.

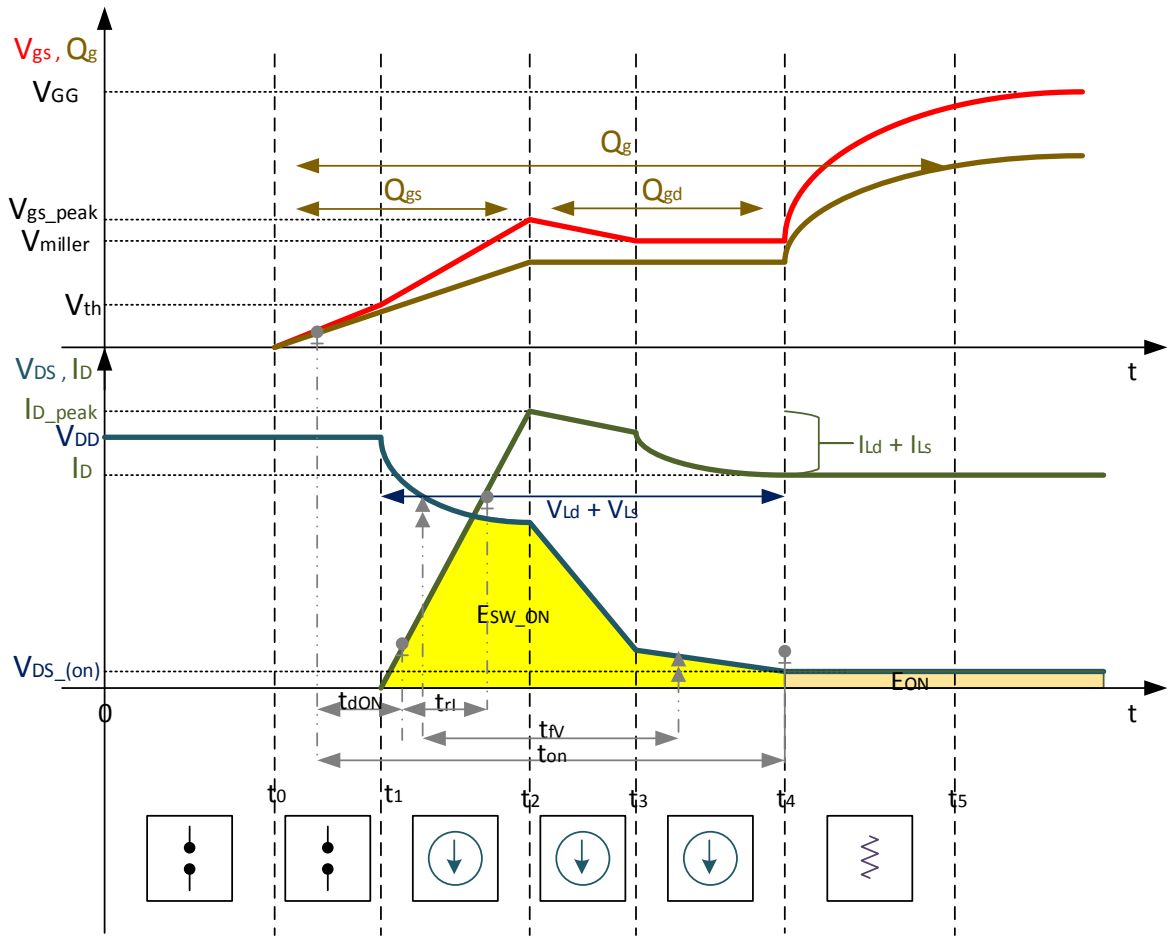


Figure 57. Switching transients of the JFET in the J-S configuration at turn-ON.

Turn-OFF Switching Transients (Stages 6–10)

The turn-OFF switching transients are a reversely symmetrical process of the turn-ON switching transients. The major function of the RC snubber takes on in this period. In order to study the effect of snubber circuit a comparison will be made between the turn-OFF switching process with and without the RC snubber.

Stage 6 [t_6–t_7] turn-OFF delay time: The gate signal is set to zero and the *JFET* operates in the ohmic region. v_{ds} will not increase and the snubber circuit will not begin to work until v_{gs} reduces to V_{miller} . As the snubber is OFF and has no current flowing through, the voltage across C_{sn} is still equal to $V_{ds(on)}$. C_{iss} is being discharged through R_g and L_s . Since the drain

current remains unchanged, the effect of L_s can be neglected. The gate–source voltage is given by

$$v_{GS}(t) = V_{GG}\, e^{-\frac{t-t_0}{(C_{gs}+C_{gd})R_g}} \qquad (57)$$

Stage 7 [t_7–t_8] voltage rise time I: Stage 7 and 8 are the rise time of the drain–source voltage. The snubber circuit begins to operate with the increase in v_{ds}. The snubber capacitor C_{sn} , which is connected in parallel with the *JFET*, is being charged up with the same voltage slew rate as $\frac{dv_{ds}}{dt}$. It slows down $\frac{dv_{ds}}{dt}$ and lengthens the voltage rise time. The resonant period formed by L_{sn} and C_{sn} is much shorter than the rising time of v_{ds} if L_{sn} is minimized. As a result, the effect of L_{sn} can be neglected. Besides, in the presence of the snubber circuit, the input current I_D will be shared by the *JFET* and the snubber capacitor. By using KCL and rearranging the equation, the drain current that remains constant at I_{D1} is given in

$$I_{D1} = I_D - C_{sn}\frac{I_D + V_{th}g_{fs}}{g_{fs}R_gC_{gd} + C_{sn}} \qquad (58)$$

It can be seen from this equation that the larger C_{sn} is, the smaller I_{D1} is. With C_{sn} large enough, the drain current may drop to a very low level that is close to zero, and v_{gs} will fall to V_{th} . Ideally the drain current stays constant and v_{gs} remains at its Miller voltage. As the gate voltage steps down to zero during the turn-OFF transients, the following relationships can be given

$$i_g = \frac{v_{GS}}{R_g} \qquad (59)$$

$$\frac{dv_{ds}}{dt} = \frac{i_g}{C_{gd}} = \frac{v_{gs}}{R_gC_{gd}} \qquad (60)$$

Where $v_{gs} = V_{miller}$

At t_8 , v_{ds} rises and the *JFET* begins operating in the saturation region.

Stage 8 [t_8–t_9] voltage rise time II: The *JFET* begins to operate in the saturation region in this stage. v_{ds} continues to rise until it reaches V_{DD} with $\frac{dv_{ds}}{dt}$ given by (60). As C_{gd} changes to a smaller value as it is in reverse relation with v_{ds} according to the datasheet, the voltage slew rate will be faster than in the previous stage. The drain current falls to I_{D1} in presence of the snubber circuit according to (58). This decreases in the drain current gives rise to a second Miller plateau voltage $V_{miller1} = V_{th} + \frac{I_{D1}}{g_{fs}}$, which is smaller than $V_{miller} = V_{th} + \frac{I_D}{g_{fs}}$. In other

words, the voltage rise time in presence of the snubber circuit will be longer than in absence of snubber circuit. It should also be noted that, in practice, there is an extra current drop in i_d during these two stages even if no snubber circuit is added. It is because the rise in v_{ds} also leads to voltage change in the parasitic capacitor of the diode and the current source, which as the snubber capacitor, requires current shared from the input current and results in the drop in i_d.

Stage 9 [t_9–t_{10}] current falling time: This is the stage when voltage overshoot occurs, and the snubber circuit takes effect to suppress this extra voltage stress on the JFET. According to the law of energy conservation, the voltage overshoot can be approximated by

$$\frac{1}{2}(L_s + L_d)I_D^2 = \frac{1}{2}(C_{oss} + C_{sn})V_{os}^2 \qquad (61)$$

$$V_{os} = \sqrt{\frac{L_s + L_d}{C_{oss} + C_{sn}}}\, I_D \qquad (62)$$

The voltage overshoot is oscillating in the power stage and damped by the stray resistance R_{stray} in the current conducting path. The drain–source voltage can be approximated by

$$v_{ds}(t) = V_{DD} + V_{os}cos\left[\omega(t - t_9) + \frac{\pi}{2}\right]e^{-a(t-t_9)} \qquad (63)$$

Where $\omega = \sqrt{\frac{1}{(L_s+L_d)(C_{oss}+C_{sn})} - a^2}$, $a = \frac{r_{ac}}{2(L_s+L_d)}$ and V_{os} is given by (62).

As v_{ds} rises to V_{DD} at t_9, the diode conducts, and the input current begins to divert from the JFET to the diode. Voltage overshoot due to L_s+L_d is greatly reduced, whose energy gets transferred to C_{sn}. v_{gs} reduces from V_{miller} to V_{th} . At t_{10}, i_d=0 and i_f=I_D. Using the same analytical method as stage 3 in the turn-ON transients, the gate–source voltage will decrease as

$$v_{GS}(t) = V_{miller1}\, e^{-\frac{t-t_9}{\tau_r}} \qquad (64)$$

The drain current during this current falling period is given by

$$i_d(t) = (I_{D1} + g_{fs}V_{th})e^{-\frac{t-t_9}{\tau_r}} - g_{fs}V_{th} \qquad (65)$$

As a comparison, the drain current in this period if there is no snubber circuit is

$$i_d(t) = (I_D + g_{fs}V_{th})e^{-\frac{t-t_9}{\tau_r}} - g_{fs}V_{th} \qquad (66)$$

Where $\tau_r = R_g\left(C_{gs} + C_{gd1}\right) + L_s g_{fs}$

Stage 10 [t_{10}–t_{11}] OFF-state operation: Eventually, the voltage overshoot in the power stage is damped by the stray resistance of the circuit. After the input current flows entirely through the diode, v_{gs} reduces from V_{th} to zero and the *JFET* operates in the cutoff region.

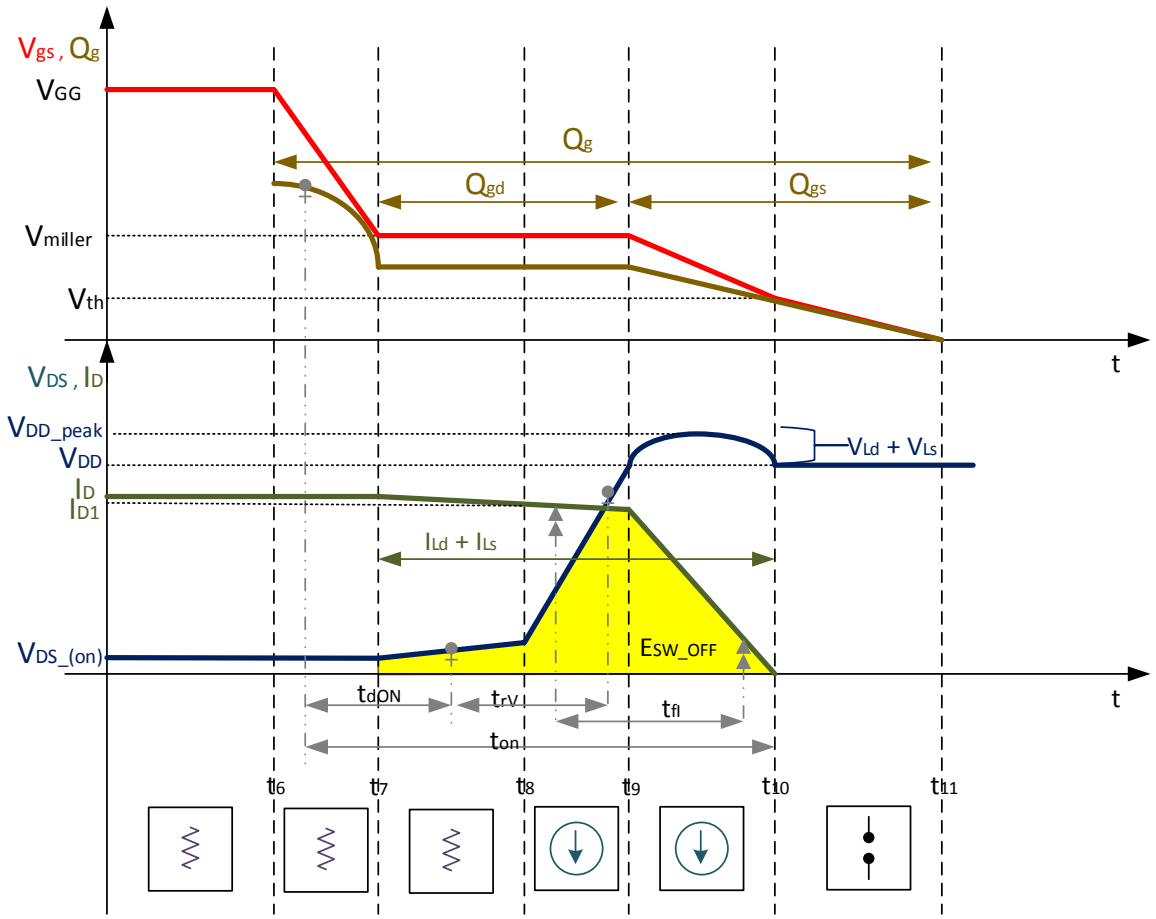


Figure 58. Switching transients of the JFET in the J-S configuration at turn-OFF.

3.1.3 Power losses and Conclusions

In the previous section, the switching characteristics of the *J-S* configuration have been carefully studied with consideration of interaction among the main power circuit, gate circuit, and snubber circuit. Parameters that can affect the voltage stress and total power loss are identified and will be designed to meet the requirement of a specific application. It was

shown that the voltage stress and the total loss of the *J-S* configuration are closely related to the gate drive and snubber conditions.

The current changing rate without snubber circuit during turn-OFF can be derived from (65) as

$$\frac{di_d}{dt} = \frac{I_D}{\left[R_g\left(C_{gs} + C_{gd}\right) + g_{fs}L_s\right]\ln\left(\frac{V_{miller}}{V_{th}}\right)} \qquad (67)$$

Voltage stress induced during MOSFET turn-OFF process without snubber circuit can be obtained by substituting (67) into

$$V_{Ls} + V_{Ld} = (L_s + L_d)\frac{di_d}{dt} \qquad (68)$$

The value of stray inductances $(L_s + L_d)$ and stray resistance R_{stray} are supposed to be determined experimentally. As the voltage overshoot occurs when the *JFET* works in the saturation region, $C_{oss}=C_{gd}+C_{ds}$. The snubber capacitance is dedicated to store the energy of stray inductances and in this way limit the voltage stress. Taking this energy into consideration

$$\frac{1}{2}(L_s + L_d)I_D^2 = \frac{1}{2}C_{oss}(V_{Ls} + V_{Ld})^2 = \frac{1}{2}(C_{oss} + C_{sn})\left((k-1)V_{DD}\right)^2 \qquad (69)$$

the value of snubber capacitance can be obtained

$$C_{sn} = C_{oss}\frac{(V_{Ls} + V_{Ld})^2 - [(k-1)V_{DD}]^2}{[(k-1)V_{DD}]^2} \qquad (70)$$

where k is the normalized desirable value for the voltage stress of the JFET.

Two important factors must be met on the selection of the elements of the snubber system. The first one is to ensure that the snubber capacitor is fully discharged before the JFET turns ON and secondly, the discharge current at turn-ON must not exceed 20% of the input current as not to increase the current stress of the JFET.

The snubber loss is denoted as P_{sn} , the switching loss as P_{sw}, the gate drive loss as P_{gate} , and the conduction loss P_{cond} are given as the following four equations, respectively. To calculate the switching loss of the MOSFET, $v_{ds}(t)$ and $i_d(t)$ that have been derived stage by stage are integrated in a switching cycle

$$P_{sn} = \frac{C_{sn}(kV_{DD})^2 f_s}{2} \qquad (71)$$

$$P_{sw} = f_s \int_0^{t_{sw}} v_{ds}(t) i_d(t)\, dt \qquad (72)$$

$$P_{gate} = Q_G V_{GG} f_s \qquad (73)$$

$$P_{cond} = I_D^2 R_{ds(on)} D \qquad (74)$$

Where Q_G is the total gate charge and t_{sw} is the switching transient time of the JFET and D is the duty cycle ratio.

By adding them together, the equation for total loss P_T can be derived.

$$P_T = P_{sn} + P_{sw} + P_{gate} + P_{cond} \quad (75)$$

Now that the voltage stress and total loss can be determined for each and every given gate drive resistance, the optimization aiming at minimizing total loss within a permitted voltage stress will be carried out. The voltage overshoot V_{os} is required to be limited to 10% of V_{DD}. Generally, the gate drive and conduction losses do not vary significantly with gate drive resistance, and snubber loss descends while switching loss ascends with the increase of gate drive resistance. It can be explained physically that a larger gate drive resistance will lengthen the switching process and thereby increasing the switching loss. Moreover, it can also reduce the voltage stress without snubber, which is proportional to the turn-OFF switching speed. Thus, less snubber capacitance is needed to limit the voltage stress to the designed value and thereby less snubber loss will be dissipated. In this knowledge, it is expected that there will be a lowest point on the curve of total loss against gate drive resistance, which is supposed to be the optimal condition. Set the of Rg ∈ [Rmin, Rmax], (typically 0–50 Ω), for each value of Rg , the snubber capacitor is calculated by using (67), (68), and (70). Then, P_T is calculated by (71)–(75) corresponding to each available value of the gate resistance. Thus, after studying the power loss with respect to the gate resistance, the minimum total loss is located thereby the optimal value of the gate resistance is determined. In this way, the optimal combination of gate drive resistance (analysed in the following sections) and snubber capacitance (analysed in chapter 4) can be obtained for different restriction on voltage overshoot.

In conclusion, this section provides a switching model and investigation into the effect of the gate resistance on the losses of the *JFET-snubber* configuration at length. The effect of the snubber circuit has been studied together with the switching transients. The differences between the experimental waveforms on the next section and the calculation results will give some deviation from the measurement, which is mainly due to the linearization of some transistor parameters. The effect of the gate drive resistance on the loss distribution is clearly demonstrated that under the design constraints, the increase in the gate drive resistance will monotonically result in an increase in the switching loss and a decrease in the snubber loss.

3.2 Requirements of gate driving a VT SiC JFET

This device makes special demands on the gate driver circuit compared to other unipolar *SiC* or Si devices. To fully exploit the potential of *VT SiC JFETs*, conventional gate driver circuits for unipolar switches need to be adapted for use with these switches: during on-state, the gate–source voltage must not exceed 3 V, while a current of around 300 mA (depending on the desired on-resistance) must be fed into the gate for the *Normally-off SiC JFET* and 2V with a minor gate current (<5mA) for the *Normally-on SiC JFET*; and during switching operation, the transient gate voltage should be around ±15 V. Special attention must be given in the Normally-off device because the low threshold voltage of less than 0.7 V requires a high noise immunity which is a severe challenge as the device has a comparably low gate–source but high gate–drain capacitance.

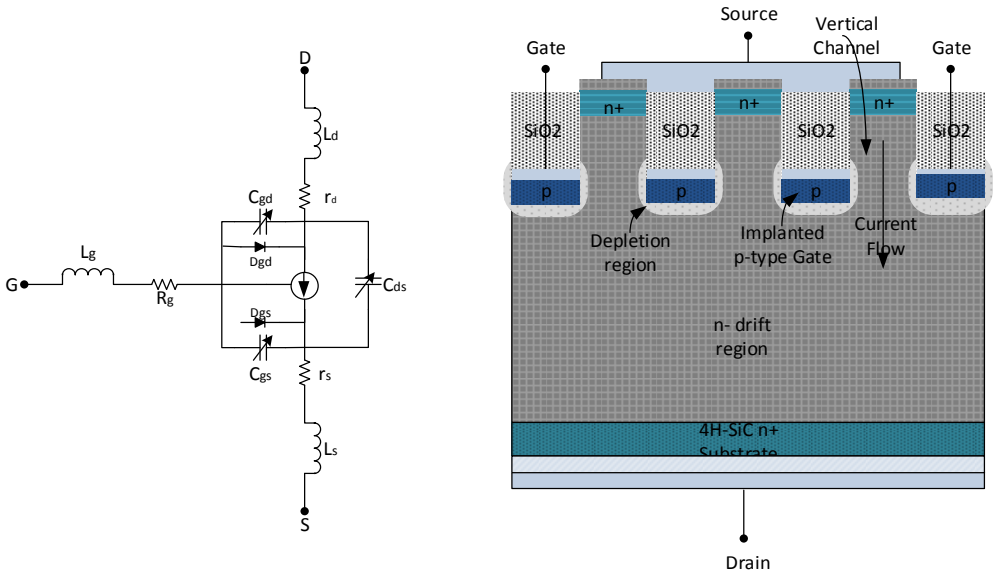


Figure 59. SiC VT JFET: cross section and equivalent circuit diagram.

Figure 59 shows the cross section and equivalent circuit diagram of the *SiC VT JFET*. Compared to conventional power semiconductors such as MOSFETs and IGBTs, the structure of the investigated device involves special requirements for its gate driver, as will be shown in this section.

The specific gate requirements of the *SiC JFET* are mainly the dynamic charge for charging/discharging the total gate capacitance and the sustainability of steady state voltage/current requirements of the gate-source diode throughout the duration of the conduction state. Even though the device requires a DC current be sustained to maintain conduction, the *SiC JFET* is not a current controlled device. The differential voltage between

the applied gate voltage and the device threshold, $V_{GS} - V_{TH}$, is the variable that controls the device channel width. Because the gate-source structure is a p-n diode a forward current can be expected anytime the structure is forward biased; however, this forward current is significantly lower than that of a power BJT. This is because the recommended operating point of the gate-source diode remains low on the gate diode forward curve. Any application of a potential beyond +3V on the gate during the steady-state conduction period no longer yields a significant gain in forward conduction characteristics. Thus steady state voltages beyond the recommended +3V will only drive excessive and unnecessary values of gate current through the gate-source diode.

3.2.1 Requirements during on-state

From the cross section in *Figure 59* it can be seen that the major difference between a junction and a MOSFET is that the gate is not insulated from the channel by an oxide, but forms a p-n junction with the source, diode D_{GS} and the drain D_{GD}, respectively. Forward biasing the gate–source p-n junction reduces the width of the space charge region. The threshold gate–source voltage $V_{GS,th}$ of the *Normally-off* device is typically around 1 V and of the *Normally-on* -7V, decreasing with temperature at the rate of approximately 1.5 mV/◦C. If V_{GS} exceeds the built-in potential of the p-n junction 2.5V<V_{bi}<3V (for both devices) at room temperature, a significant amount of holes are injected into the channel. The consequence for the gate driver is the limitation that during the on-state, no more than 3 V should be applied to the JFET's gate with respect to the source (or to the drain, e.g., during synchronous rectification) to avoid large currents and thus unnecessarily high power flowing into the gate.

In *Figure 60*, *Figure 61*, *Figure 62* the typical output characteristics of the SJDP120R085 (Normally-on) are presented as were taken in experiments from ITE (Ιδρυμα Ερευνας και Τεχνολογιας- Institute of Research and Technology) and the Power Electronics and Electric Machines laboratory in NTUA and in *Figure 63*, *Figure 64*, *Figure 65* the equivalent plots for the SJEP120R100 (Normally-off) from its datasheet.

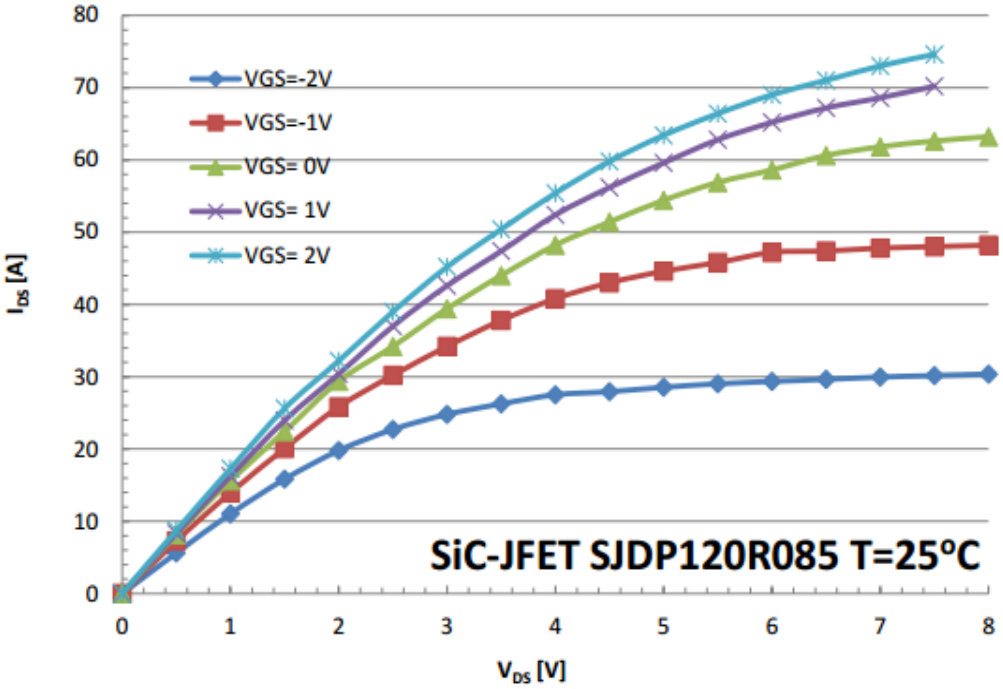


Figure 60. Typical Output Characteristics for the SJDP120R085 (Normally-on). $I_D=f(V_{DS})$; $T_J=25^oC$; parameter V_{GS}.

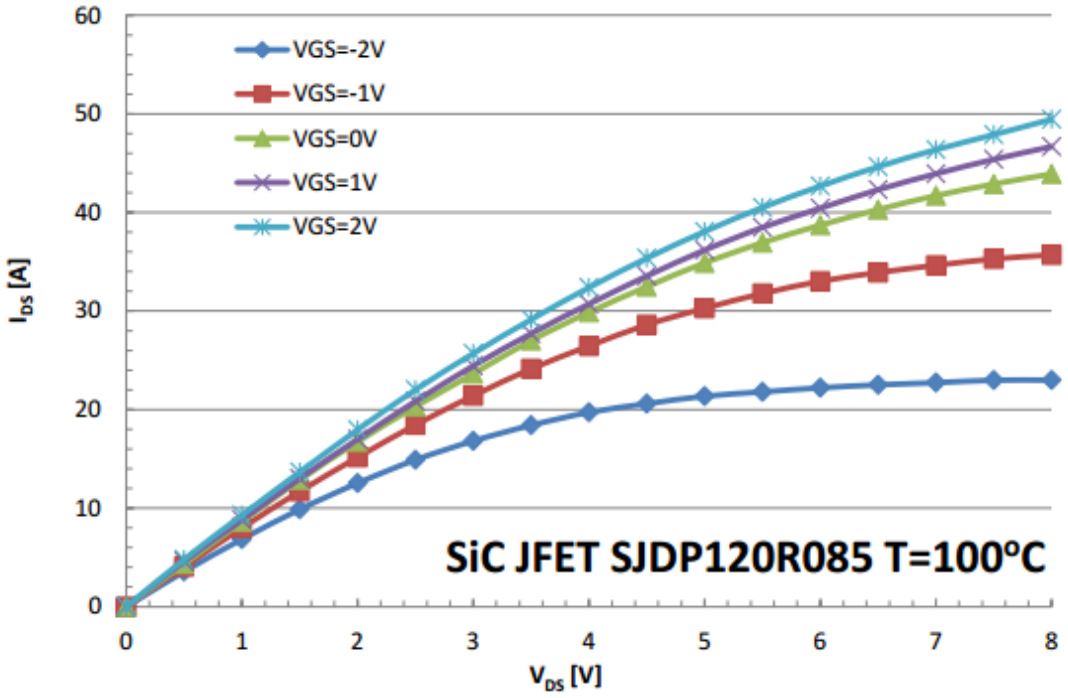


Figure 61. Typical Output Characteristics for the SJDP120R085 (Normally-on). $I_D=f(V_{DS})$; $T_J=100^oC$; parameter V_{GS}.

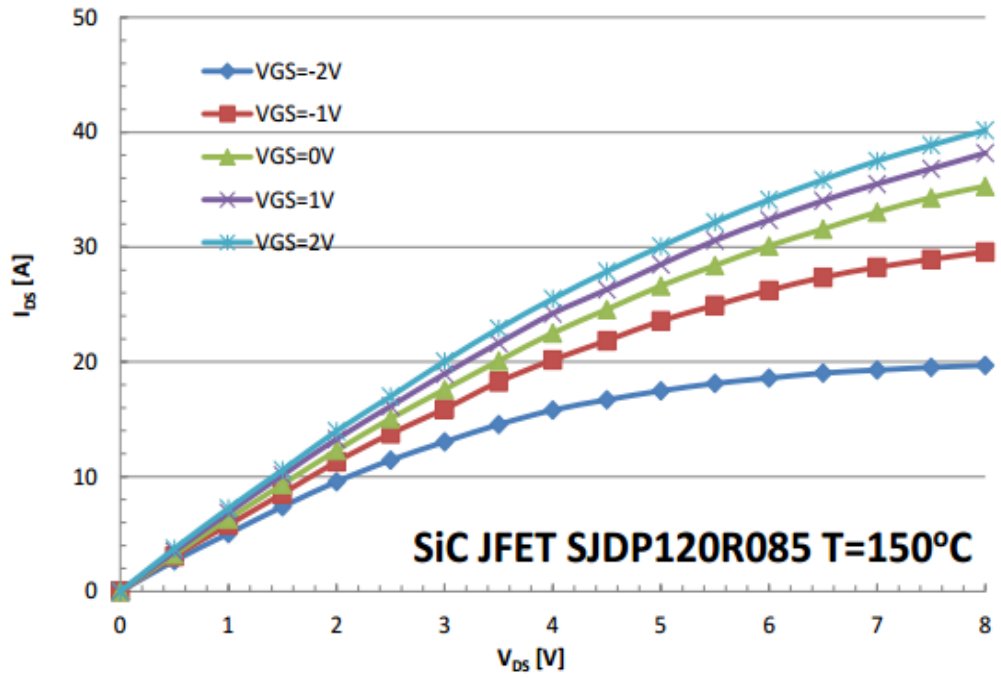


Figure 62. Typical Output Characteristics for the SJDP120R085 (Normally-on). $I_D=f(V_{DS})$; $T_J=150^oC$; parameter V_{GS}.

Typical Output Characteristics for the SJEP120R100 (Normally-off) for various temperatures

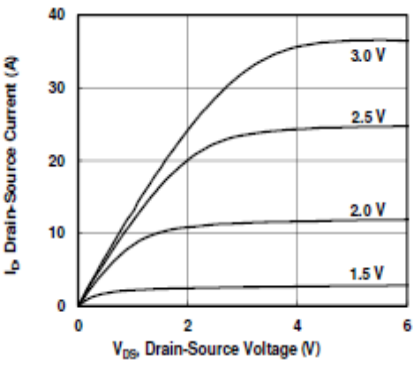


Figure 63. TJ=25°C

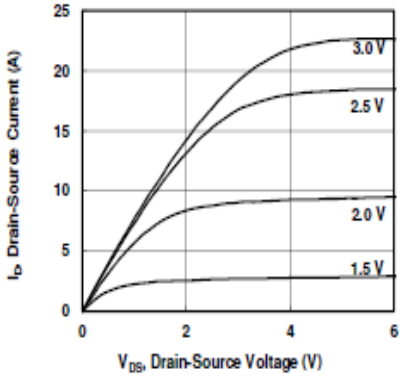


Figure 64. TJ=100°C

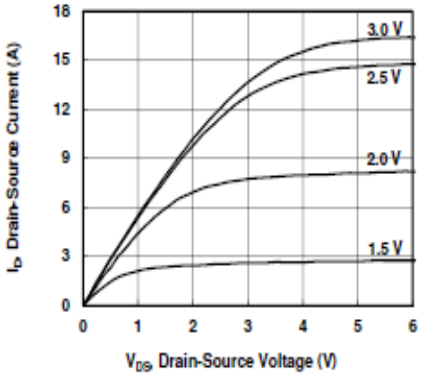


Figure 65. TJ=150°C

As can be seen the larger the applied gate-source voltage the larger is the drain current I_D. In the case of the Normally-on device an increase of 20% at most for T_J=25°C is noted if we apply 2V instead of 0V in V_{GS}. On the other hand, for the Normally-off, an increase of 0.5V in V_{GS} may offer up to 40% larger value for the I_D. Consequently, it is evident that by applying the largest possible value for the V_{GS} we can gain a significant increase in the efficiency of our system. This limit in the gate-source voltage value will be given by the typical output characteristics of the diodes D_{GS} and D_{GD} of each device so that we will not allow large currents in the gate drive circuit but in the same time we will be able to achieve improvements in our systems.

To continue the previous discussion for the increase of the gate-source voltage, the effects on the $R_{DS,on}$ are investigated on figure 14 and 15. As was expected the increase of V_{GS} (in the case of the Normally-on) or I_G (for Normally-off) results in further reduction of $R_{DS(on)}$ according to the plots from the datasheet of the devices.

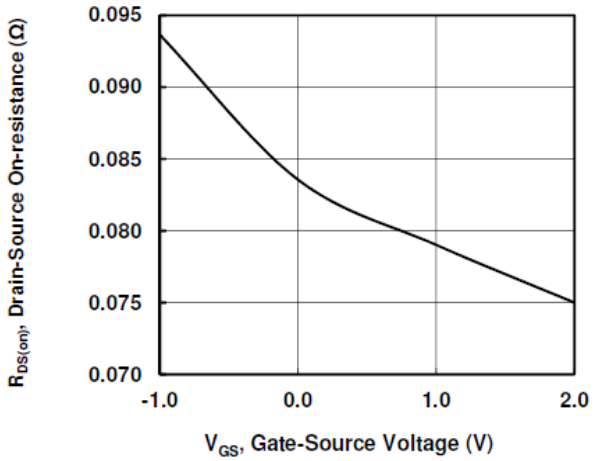


Figure 66.Drain-source resistance. $R_{DS(on)}=f(V_{GS})$; $T_J=25^oC$. SJDP120R085 (Normally-on)

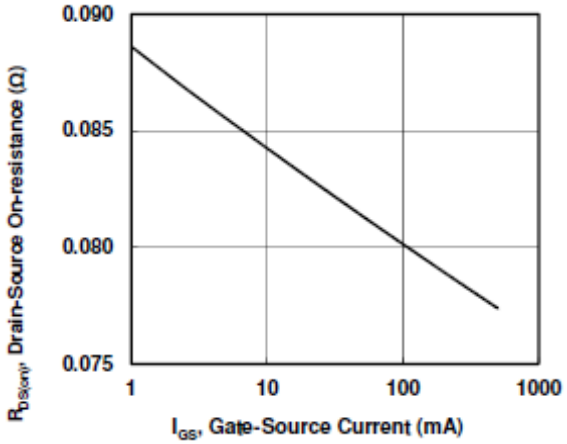


Figure 67. Drain-source resistance. $R_{DS(on)}=f(I_G)$; $T_J=25^oC$. SJEP120R100 (Normally-off)

The correlation between the drain–source on-resistance $R_{DS,on}$ and the applied gate bias to V_{GS} (in the case of the Normally-off in terms of the current, which can be related to the respective voltage using the diode characteristic in *Figure 69*) is shown in previous figures. From the datasheet plots and [3] it can be seen that $R_{DS,on}$ depends on T_J and I_D. As the temperature increases, the saturation limit of the drain current is decreased. So for both devices, as T_J is increased from T_J =25°C to T_J =150°C, I_D is limited approximately up to 30% while $R_{DS,on}$ gets 100% larger. For example, for the Normally-off device, we may achieve 36 A with $R_{DS,on}$ equal to 125 mΩ for T_J =25°C but as T_J gets high I_D is limited to 16 A with $R_{DS,on}$ 100% higher (250 mΩ).

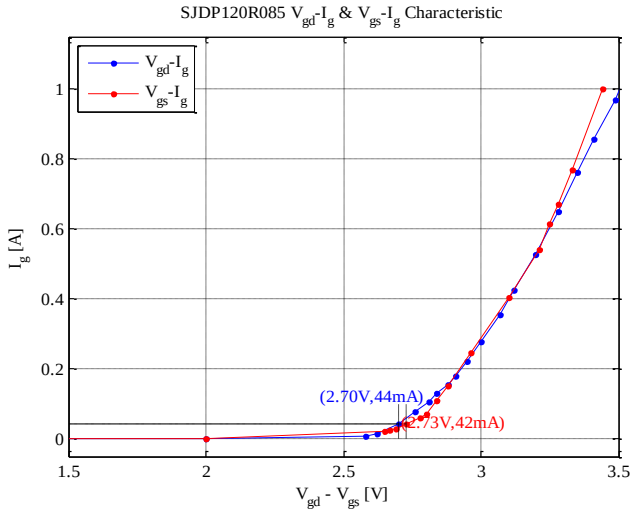


Figure 68. Output characteristics for the Dgs and Dgd. SJDP120R085 (Normally-on)

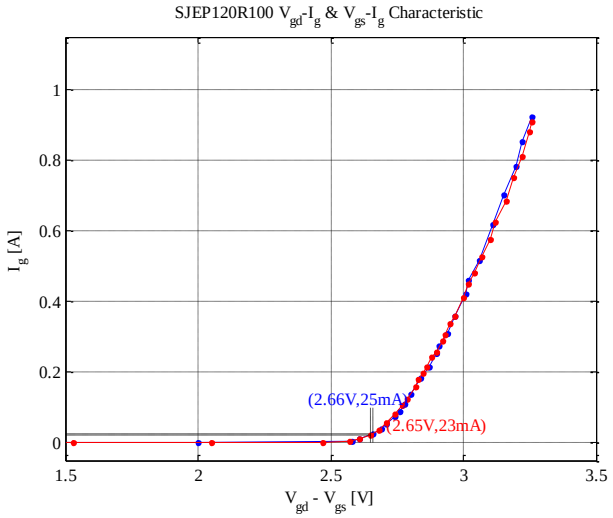


Figure 69. Output characteristics for the Dgs and Dgd. SJEP120R100 (Normally-off)

As explained earlier, the applied V_{GS} will be determined by the output characteristics of the diodes in the devices. In order not to allow large currents, which would result in augmented power consumption from the gate drive circuit or even in the destruction of the device, we should take into account the above plots. As a result, no more than 3V should be applied in the devices. A value of 2.7V is chosen in order to exploit as most as possible the forward characteristics of the *SiC VT JFETs* and simultaneously to avoid large values of I_G. Additionally, choosing these values, a design is introduced that can be easily adapted for other applications towards lower or higher gate currents for other on-resistances or the parallelization of several chips. Besides, in [1] a reduction of over 18% in conduction losses was presented through forward biasing a *DM SiC JFET*, while switching losses less than 500 μJ were achieved over one switching cycle when operating at 600 V, 20 A.

The required gate currents that have to be determined for the gate driver design cannot be identified application independent. That is, the drain current (depending on the converter specifications), the available chip area (limited by cost constraints), and the maximum on-resistance (given by efficiency requirements) have to be determined for each application. This will be an iterative optimization as these different aspects interact. It has to be noted that at the mentioned gate current levels, the required power at the gate–source terminal can be more than 1 W for a single switch. Taking the efficiency of the gate driver supply converters or restrictions with respect to self-heating of the drive components (e.g., due to high ambient temperature levels) into account, the gate current, which has to be delivered by the gate driver, and its influence on the on-resistance are also subject to the overall converter optimization.

3.2.2 Requirements During Off-State

During the cut-off state, the gate-source junction must be reverse biased in order to create a depletion layer in the channel of the JFET. However, if the applied voltage will be larger than the breakdown one, then according to the diode output characteristics plot there will be a large current flowing through the JFET gate. The breakdown voltage may change with the temperature. That's why a large resistor reducing this current should be present in the cut-off path of the gate drive circuit in the extreme case of high temperature values but in the same time would also be able to keep the device off on this period under normal conditions.

Bearing in mind that the leakage currents occur in the off-state of the device and that the device may remain in the off-state for a longer time than only a few microseconds if, for example, the overall converter is in standby, the losses in the diode D_{GS} and D_{GD} as well as the drain-source leakage current I_{DSS} (*Figure 70*, *Figure 71*) should be limited to a low level. Hence, the off-state bias is chosen to −15 V leading to a leakage current on the diodes of less than 1 mA and on the drain-source junction even less. Consequently, low gate driver power consumption and off-state losses on the channel of the JFET may be achieved.

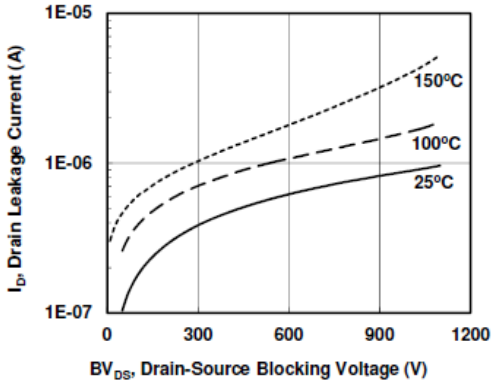


Figure 70. Drain-Source Leakage current. $I_{DSS}=f(V_{DS})$; $V_{GS}=0V$; parameter T_J.
SJEP120R100 (Normally-off)

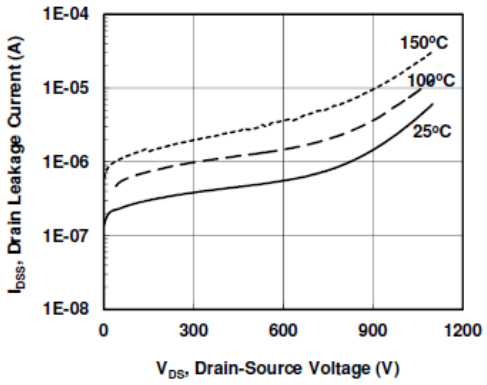


Figure 71. Drain-Source Leakage current. $I_{DSS}=f(V_{DS})$; $V_{GS}=0V$; parameter T_J.
SJDP120R085 (Normally-on)

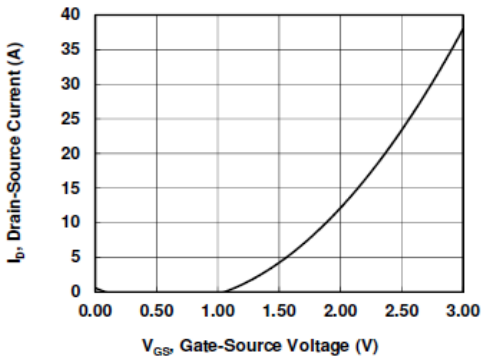


Figure 72. Typical Transfer Characteristics. $I_D=f(V_{GS})$; $V_{DS}=5V$; $T_J=25^oC$. SJEP120R100 (Normally-off)

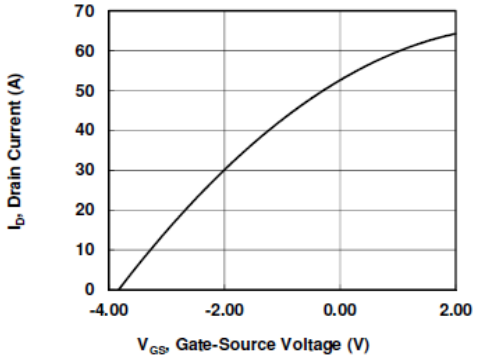


Figure 73. Typical Transfer Characteristics. $I_D=f(V_{GS})$; $V_{DS}=5V$; $T_J=25^oC$. SJDP120R085 (Normally-on)

Apart from the above requirements special attention should be given to the Miller effect of the *SiC VT JFET* devices which causes specific demands on the gate driver during the off-state. After turn-off of the *JFET's* channel, i.e., after discharging the gate–source capacitance C_{GS} from approximately 2.7V to a value below the threshold voltage, and thus turning the JFET completely off, it can happen in half-bridge configurations that the gate–drain capacitance C_{GD} of the $JFET_{HS}$ is charged to the actual blocking voltage V_{DC} significantly later than the turn-off of the switch. This time delay between the turn-off of the $JFET_{HS}$ and the voltage rise across it occurs typically in the following situation: the inductor current i_L in Figure 74 is freewheeling in $JFET_{HS}$, before the channel of $JFET_{HS}$ is turned off. The current i_L will continue to freewheel in D_{HS} after turn-off of $JFET_{HS}$, until $JFET_{LS}$ is turned on. Once $JFET_{LS}$ is turned on, the source of $JFET_{HS}$ (and thus also its gate, if the negative gate bias is negligible compared to V_{DC}) will be clamped by $JFET_{LS}$ to the negative supply voltage rail, while the drain of $JFET_{HS}$ remains at V_{DC}, resulting in quick charging of C_{GD} to approximately V_{DC}. Depending on the gate driver design, a certain portion of the capacitive current charging C_{GD} flows via C_{GS} or via the gate driver circuit to the source of the JFET.

So, since the $JFET_{HS}$ is in cut-off state, a large parasitic current I_{CGD} flows through R_{gL}, because of C_{GD} ,to the earth causing a rise in gate-source voltage,

$$V_{GS} = -V_{gg} - R_{gL}I_{CGD} \qquad (76)$$

Accordingly, the same effect takes place when the $JFET_{HS}$ turns-on and the $JFET_{LS}$ switches to cut-off state,

$$V_{GS} = -V_{gg} + R_{gH}I_{CGD} \qquad (77)$$

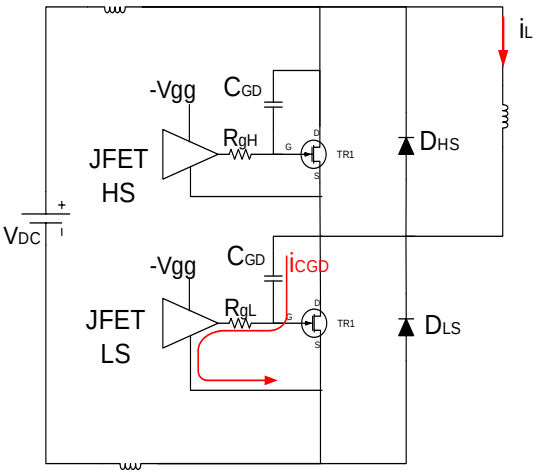


Figure 74. Half bridge configuration and Miller effect.

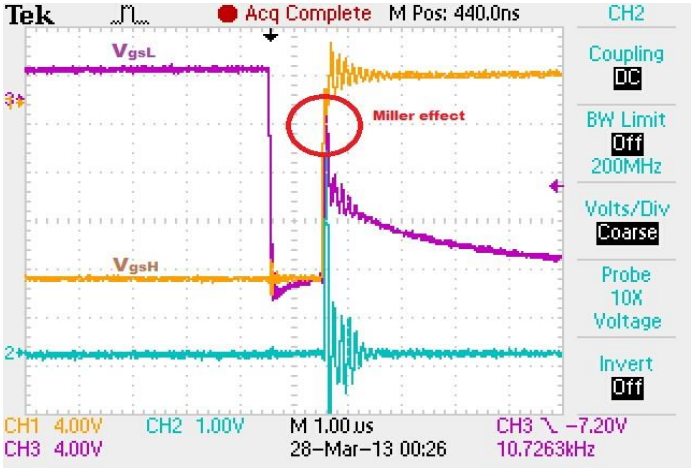


Figure 75. Miller effect.

Three factors increase the risk that this capacitive current leads to a voltage rise across C_{GS} above the threshold voltage resulting in an accidental turn-on of $JFET_{LS}$ which would short circuit the dc link voltage. The investigated *SiC VT JFET* has a vertical channel in contrast to typical Si and *SiC* MOSFETs. This purely vertical structure leads first to a comparably low gate–source capacitance C_{GS} and second to an inherently high gate–drain (Miller) capacitance C_{GD}. This fact is illustrated in [3], which compares C_{iss} and C_{rss} of the 1200V 30A *SiC* normally off JFET with the C_{iss} and C_{rss} of a typical *SiC* MOSFET with similar voltage and current rating. C_{rss} is C_{GD} in the JFET model and is significantly higher for the JFET compared to the MOSFET (by a factor of 3 to 10 depending on the drain–source voltage V_{DS}). C_{iss} as the sum of C_{GS} and C_{GD} is lower for the JFET (by a factor of approximately 1.5), i.e., the JFET's C_{GS} is much smaller than that of the MOSFET, as expected from the device cross section. Then, even though the direct comparison of C_{GS} and C_{GD} of the JFET reveals still a ratio of $C_{GS}/C_{GD} \approx 10$, the charge of C_{GD} can increase the gate–source voltage of the JFET as the voltage across the charged gate–drain capacitance is typically three orders of magnitude higher than the threshold voltage of the JFET which goes down to 0.7 V at 250 ◦C.

Hence, in order to avoid this effect the gate driver circuit has to provide a low-impedance path for the capacitive current from the gate connection to the source of the normally off JFET to turn it reliably off. As this path will have parasitic resistances and inductances, a negative gate bias with respect to the source during the off-state is, thus, also needed. That's why it is chosen to use an external capacitor C_{GS} which offers an extra low-impedance path to I_{CGD} to pass through the gate without affecting V_{GS}. This small filter capacitor C_{gs} connected across the gate-source of the transistor is intended to suppress oscillations and the problem of retriggering at the turn-off of the transistor (Miller effect).

3.2.3 Requirements During Switching

The procedure for switching on and off the new *SiC* devices is the same like the traditional Si Mosfets. The concepts that were used so far for the Mosfets may be applied also in the *SiC JFETs*. So during the switching transients, the gate driver must deliver the charge required by the parasitic input capacitance C_{iss}, (Figure 76, Figure 77) which is the sum of the gate–source capacitance C_{GS} and the gate– drain capacitance C_{GD} of the JFET model in Figure 59.

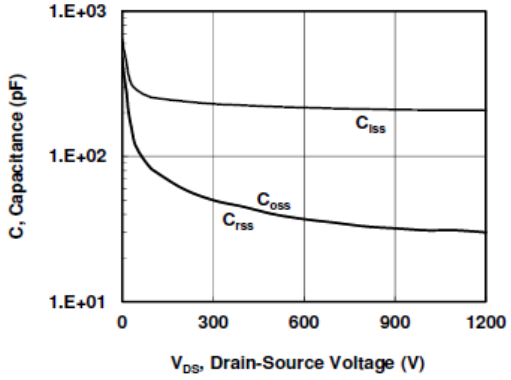


Figure 76. Typical Capacitance. C=f(VDS); VGS=-15V; f=100 kHz. SJDP120R085 (Normally-on)

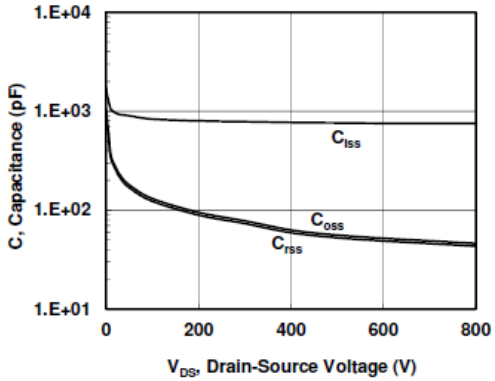


Figure 77. Typical Capacitance. C=f(VDS); VGS=-15V; f=100 kHz. SJEP120R100 (Normally-off)

To turn the devices on, C_{GS} must be fully charged by the gate driver and C_{GD} (charged to approximately V_{DS} in the off-state of the device) must be discharged by feeding current from the gate terminal to the drain. To turn the device off, the opposite action is necessary. The gate driver must sink current in order to discharge C_{GS} and charge C_{GD} to approximately V_{DS}. The charges that the parasitic capacitances are needed may be found in the datasheet of the devices. For example, the Normally-on JFET demands a total gate charge Q_g=32nC while the Normally-off Q_g =71nC. From the fundamental electric law $I = \frac{dQ}{dt}$, the required gate current for the charge of a Q may be determined.

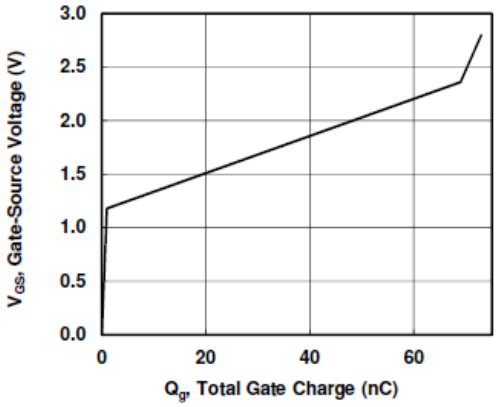


Figure 78. Gate charge. $Q_g=f(V_{GS})$; V_{DS}=800V; I_D=10A; T_J=25°C. SJEP120R100 (Normally-off)

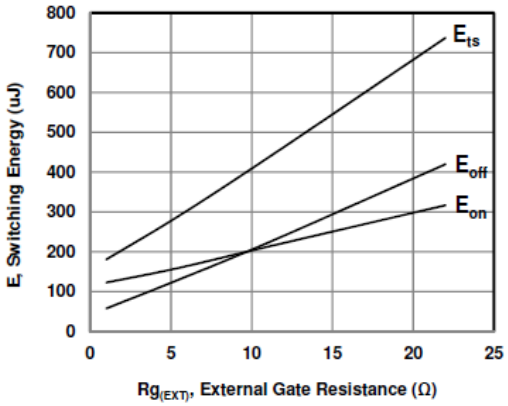


Figure 79. Switching Energy Losses, $E_s=f(R_{g(EXT)})$; V_{DS}=600V; I_D=17A; GS=±15V. SJDP120R085 (Normally-on)

Due to the RC low-pass characteristic at the gate, the achievable switching speed of the *JFET* is limited. In order to be able to reach the desired voltage levels during turn-on ($V_{GS} \geq V_{GS,th}$) and turn-off ($V_{GS} \leq V_{GS,th}$) fast, the gate driver should apply voltages significantly higher than these steady-state values for a short period of time at each switch state transition, so that C_{GS} is rapidly charged to the desired voltage level with a higher current. Semisouth allows transient gate–source voltages for turn-on of up to +15 V for a duration of less than 200 ns, and for turn-off, a voltage of −15 V equals the voltage level during the off-state in this gate driver design.

However in some applications, requirements given by electromagnetic interference, common mode or insulation issues, set limitations to the switching speed of power semiconductors. In such cases, a further gate driver requirement concerning the switching transients is the ability to switch with a preset switching speed that is below the maximum achievable speed.

Peak gate current value dictates the turn-on speed. The higher the applied gate driver voltage, the higher the gate resistance R_g is required for a given current. It is worth mentioning that the higher the R_g the higher the damping in the gate circuit, which in some applications is critical. The drawback of high R_g values is that higher losses might occur due to power dissipation in the gate resistor which limits the constant gate current needed for on-state conduction. In order to achieve a very fast turn-on, a high amplitude fast rising gate current pulse is required. This can only be possible if the gate leakage inductance L_g is low enough. Minimizing the physical distance between the gate driver and the gate of device is a reasonable solution. Due to fairly low gate threshold voltage of *SiC VJFET* any parasitic ringing in the gate circuit can result in the accidental turn-on of the device. Thus, it is important to keep the ringing in the gate minimized.

3.2.4 Gate Driver Temperature Behavior

Some of the requirements for the gate driver set by the switch characteristics investigated so far are temperature dependent, especially with respect to the gate current. Ideally, the gate driver behaves over the operating temperature range such that it caters to these changing requirements and does not induce any additional temperature variations itself. It is important to note that one of the risks in case of temperature rise is the change of the breakdown voltage as it would result in destruction of the device. But the gate drive circuit which is analysed in the following section offers protection from the temperature by limiting with a large resistor the current that would pass in the case that the breakdown would be lower than -15V.

3.2.5 Gate Driver Standard Requirements

All of the aforementioned requirements for the investigated gate driver are given by the properties of the *SiC* normally off JFET. A novel, ubiquitous gate driver has to also fulfil standard requirements that apply to any gate driver used in power electronic converters:

1. low power consumption;
2. qualification for switching frequencies of standard power electronic converters in the investigated voltage range up to around 100 kHz;
3. enable arbitrary duty cycles from 0% to 100%;
4. robustness against steep voltage changes;
5. performance invariance against spread for factory standard models (of the gate driver IC itself as well as the switch);
6. protection from high $\frac{dv}{dt}$, $\frac{di}{dt}$ ratios;
7. functionality even in high temperature conditions;
8. low (circuit) complexity and cost.

3.3 Novel topologies of gate driving VT SiC JFET

As described two main requirements must be satisfied by the gate driver; delivery/removal of dynamic gate charge and sustainability of DC gate voltage and resulting gate-source current during conduction/cut-off. The ability of the gate driver to quickly deliver/remove the necessary gate charge required the by internal gate-source and miller capacitance of the device is the main factor that affects the time it takes for the device to

transition between states. The gate drive should also be designed to efficiently maintain the steady state DC gate voltage and gate current required to maintain minimum $R_{DS(ON)}$ during conduction. Thus far three types of gate drivers have been designed to satisfy these conditions and are recommended based on user experience and application needs.

Several concepts for adapted gate drivers have been presented in the literature. Some still have certain limitations, e.g., with respect to switching frequencies and possible duty cycles, and some are very complex solutions with the need for several integrated circuits, their own dc–dc converters or additional cooling due to high gate driver losses [3]–[9]. In this paragraph, one novel ac-coupled and one dc-coupled gate driver topologies are presented that overcome the current limitations while still having a low circuit complexity using one or two gate driver IC and passive components only. First, the proposed novel gate driver concepts are presented in detail. Next, the theoretical considerations are validated in a double pulse test showing experimental waveforms of the switching transients. The conditions under the test will be performed are for V_{DC}=200V, L=115μH for a time period dt=3μs and I_D will be ~4A. Conclusions and a comparison study are drawn in the next section.

More specifically, in this section three different gate drive circuits from which all of them apply for the Depletion Mode (DM) SJDP120R085 *SiC JFET* and two of them for the Enhancement Mode (EM) SJEP120R100. Two will be based on the AC-Coupled logic where the main core of the design is an R-C-D network and are depended by the time constant $\tau=RC$. The differences between the two AC-coupled circuits are concerning the applied voltage during the conduction state. The last circuit is based on the DC-coupled logic which means that remains unchanged for all the switching frequencies.

3.3.1 R-C-D gate drive circuit

This drive circuit which is illustrated in Figure 80 is a simple R-C-D network which is widely used for driving Normally-on SiC JFETs. The basic idea of the proposed driver is to create a circuit that adapts to the different JFET gate characteristics. The output of the parallel combination is directly connected to the gate of the JFET and the source of the JFET is connected directly to the positive supply pin of the gate driver IC.

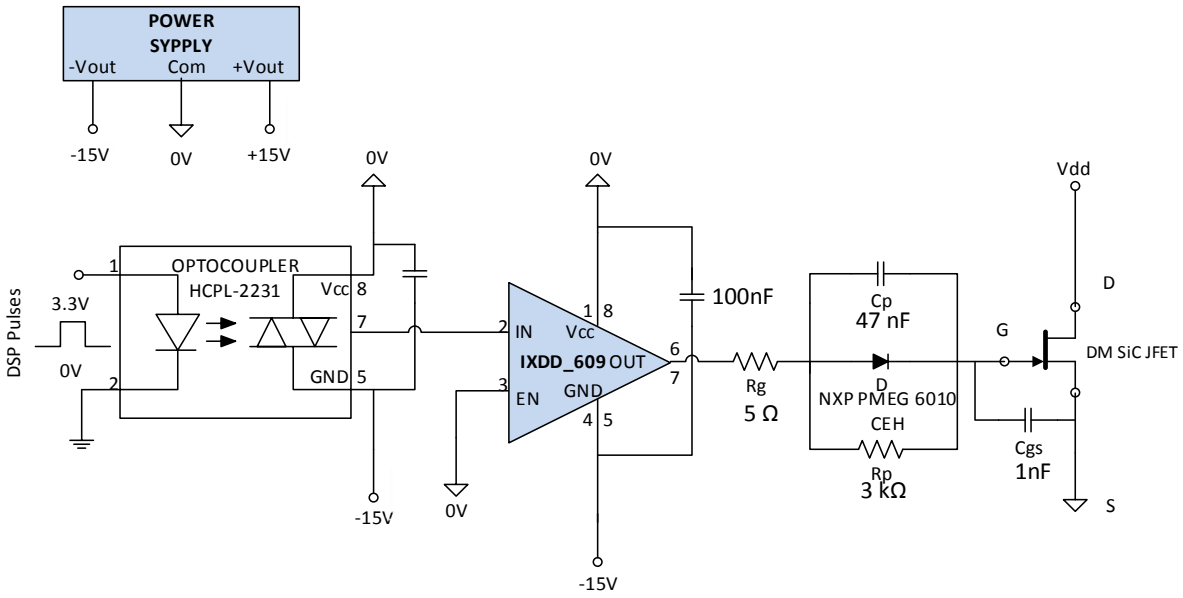


Figure 80. R-C-D gate drive circuit without forward bias for the DM SJDP120R085 SiC JFET.

Circuit Schematic; More specifically, an isolated power supply is used which is supplied externally, in order to provide voltage ± 15V to the circuit. The control signal is isolated via an optical isolator HCPL-2231, while the IXDD_609 is used as a current amplifier, with a maximum rated current of 9 A. The IXYS integrated circuit is a high speed high current driver for large MOSFETs and IGBTs with a peak current of 9 A and a wide voltage range varying from 4.5 to 35 V. The output stage of this IC is a PMOS-NMOS totem-pole arrangement with a matched turn-on and turn-off output impedance R_d of 0.5 Ω. When driving a capacitance of 47 nF, approximately the value of the *JFET* input capacitance C_{iss} ($C_{iss} = C_{gs}+C_{ds}$). The use of capacitor C_{gs} aims at the Miller effect protection and at the limitation of the V_{DS} voltage oscillations by reducing the $\frac{dv}{dt}$ and $\frac{di}{dt}$ in the maximum affordable levels of the semiconductor. The bias voltage used for the output stage of the gate-drive chip is 15 V, and is bypassed by a ceramic capacitor of 100 nF; it is sized to provide the turn-on and turn-off currents for the gate drive transients. Also, a 1 nF ceramic capacitor is used as a differential filter at the control input pin of this IC which adds a 20 ns delay to the control signal, but provides a smoother output signal. The R-C-D network on the other hand, although in the gate-source loop, is only used to compensate for the varying pinch-off and breakdown voltages of present *JFETs* and also to limit the gate terminal current in breakdown, but not to slow down the device switching. This network is needed in case the JFET gate-source p-n junction becomes forward biased or is transiently broken down into avalanche by the gate-driver, in which case it would statically absorb the voltage difference between the gate-drive output voltage and the device gate-source terminals once its capacitor voltage builds up. This voltage difference has also the advantage to provide a positive bias at turn-on increasing the JFET switching speed. The specific surface mount devices (SMD) used in this case for the R-C-D

network are a 5 kΩ resistor, a 47 nF ceramic capacitor, and one 60V/1A very low V_f Schottky barrier diodes by NXP (PMEG6010).

This simple AC-coupled gate drive circuit consists an effective way of driving a Normally-on *SiC JFET* as it is possible to control the switching speed of the element to very high levels by modifying the series resistance R_s. However, the applied duty cycle and the switching frequencies are limited by the ac-coupled nature of the circuit.

Operation; The operation mode of this particular circuit is to provide a negative voltage V_{GS} = -15 V, which is lower than the pitch-off voltage V_p, in order to lead the JFET in cut-off state, while in the conduction state, positive voltage V_{GS} = 0 V is supplied to the *JFET* gate in order to lead it to conduction. The main part of this circuit is driving the R_p-*C*-*D* network along with a series resistance R_s.

During the transition from the on-state to the cut-off state, the amplifier provides -15V negative voltage to the gate of the *JFET* for hasty discharge of parasitic capacitances of the device, while the capacitor of the R_p-*C*-*D* network charges with a constant charging time τ = R_gC. after it is fully charged, the current stops flowing through the capacitor *C* and passes through the resistor R_p. To sum up, during the transition to the conducting state of the JFET, the current amplifier provides a voltage of 0 V to the JFET gate while the capacitor of the R_p-*C*-*D* network discharged with the same constant charging time τ, offering the necessary current spikes to the gate for fast charging of the internal parasitic capacitances and C_{GS} and C_{GD} of the device.

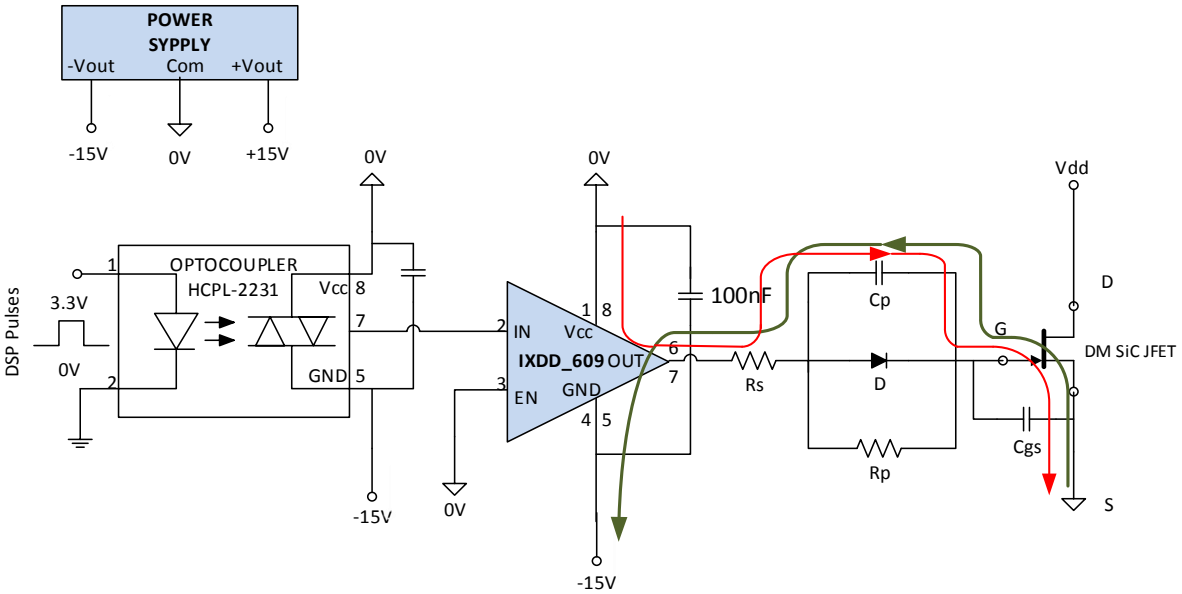


Figure 81. Green line describes the transition procedure from the on-state to cut-off; red line, transition from the cut off-state to on.

The values of the elements of the above circuit are based on the previous theoretical analysis as well as experimental measurements. First of all, the series resistance R_s should

have a small value so that the charging and discharging time of the capacitor will be low enough and on the same time the gate drive circuit may provide the appropriate current spikes. According to the datasheet of the Normally-on *SiC JFET* SJDP120R085 a typical value for the gate charge in the best case that V_{GS}=2.5V, V_{DS}=600V and I_D=10A is Q_g=32nC. In any other case the gate charge is much larger. So we may assume that the total gate charge including the parasitic one formed in the gate-drain junction will be equal to *75nC* and it is desirable for the capacitors to be charged within 50ns. Hence, the current spikes will be

$$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{75nC}{50ns} = 1.5A \qquad (78)$$

After experimental measurements, the series resistance is chosen to be R_s=5Ω which in combination with the internal gate resistance of the JFET will give current spikes of 1.5A and will limit the drain-source voltage overshoots by reducing the switching time. Finally, for the choice of the capacitor *C*, the following inequality is applicable,

$$\frac{2Q_g}{V_{DD} - V_{GS}} \leq C \leq \frac{4Q_g}{V_{DD} - V_{GS}} \qquad (79)$$

where V_{DD}=-15V is the negative gate voltage of the current amplifier while V_{GS} is the real voltage that is applied in the gate. In fact, during the transition to the cut-off state is never -15V as there is a 2.5V voltage drop so that the capacitor can be fully charged. In the computation of the gate charge, the addition of the external C_{gs} is also considered.

$$\frac{2Q_g + Q_{Cgs}}{V_{DD} - V_{GS}} \leq C \leq \frac{4Q_g + Q_{Cgs}}{V_{DD} - V_{GS}} \Leftrightarrow$$
$$\frac{75nC}{2.5V} \leq C \leq \frac{140nC}{2.5V} \Leftrightarrow$$
$$27.6nF \leq C \leq 55.2nF \quad (80)$$

As a result the capacitance is chosen *C=47nF*, R_s=5Ω and the charging time τ=235ns.

Once the capacitor is fully charged, then the current flows through the resistance R_p. Choosing a high value for the resistance R_p, the gate current is limited to a very low value and as a result the device gains protection against the effect of the gate's breakdown. Since the capacitor is fully discharged, then the conduction-state and cut-off current flows through both R_g and the diode *D* respectively. The switching cycle can now be repeated.

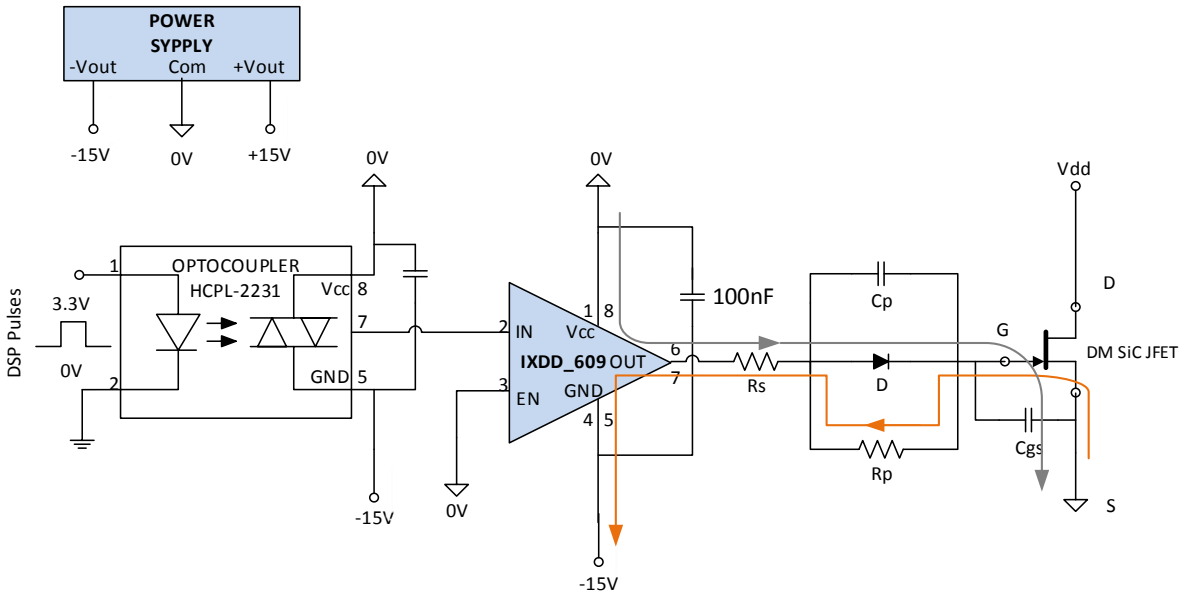


Figure 82. Grey line describes the route of the current during the conduction state and the yellow one the steady cut-off state.

Since R_p=3kΩ, the steady cut-off current is

$$I_{g_{cutoff}} = \frac{V_{DD} - V_{GS}}{R_p} = \frac{2.5V}{3k\Omega} = 0.83mA \qquad (81)$$

while the conduction current I_{gFWD} is much smaller and can be found by the diode characteristics D_{gs} shown in the previous section.

To sum up, the main part of the driver is a parallel connected network consisting of a diode D, a capacitor C_p, and high-value resistor R_p, while a gate resistor R_g is connected in series with the gate. During the on state of the *SiC JFET*, the output of the buffer, V_g, equals 0 V, and the device is conducting the current through the diode *D* and the series resistance R_s. When the JFET is turned off, the buffer voltage, V_g, is switched from 0 V to -15V. At this time, a current peak is supplied to the gate-source junction of the JFET through the gate resistor R_g, and the capacitor C_p. Hence, the parasitic capacitance of the gate-source junction, C_{gs}, is charged, and the voltage drop across the capacitor C_p equals the voltage difference between -15V and the breakdown voltage of the gate (<-15V). During the steady-state operation in the off-state, a low current is only required to keep the JFET off. This current is supplied through the resistor R_p. It is worth mentioning that the value of R_p should be chosen carefully to avoid breakdown of the gate-source junction. Regardless of the choice of R_p, it is possible to adjust the switching performance to any desired speed by selecting an adequate value of the gate resistor R_g. Despite the overwhelming advantages of the normally on *SiC JFET*, the main problem with this device is that a possibly destructive shoot through is obtained in case

the power supply for the gate driver is lost. It is, therefore, more than essential to design smart gate drivers to overcome such problems.

Element	DM SJDP120R085
Decoupling Capacitors	100nF
Diodes D_1, D_2	PMEG6010
C_{gs}	1nF
R_s	5 Ω
C_p	$\frac{2Q_g + Q_{Cgs}}{V_{DD} - V_{GS}} \leq C \leq \frac{4Q_g + Q_{Cgs}}{V_{DD} - V_{GS}}$ $27.6nF \leq C \leq 55.2nF$ $C = 47\ nF$
R_p (for low cut-off current and temperature protection)	3 kΩ
Required Peak current for Δt=50 ns, I_{peak}	$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{75nC}{50ns} = 1.5\ A$
Forward gate current, I_{FWD}	0.05 mA
Cut-off gate current, I_{cutoff}	0.83 mA
Charging constant, $\tau = R_s C_p$	235 ns
Total considered gate charge, Q_g	75 nC
On-state Voltage	0 V
Off-state Voltage	-15 V

Table 4. Calculation of the various parameters for the AC-coupled gate drive without forward bias.

3.3.2 AC Coupled Drive Circuit With Forward Bias

This innovative driver circuit is an improvement of the previous one, due to the forward bias applied to the *SiC JFET* [1]. In general, the AC coupled with forward bias drive circuit operates in a similar way as the drive circuit investigated above. The only essential difference in comparison to a typical *R-C-D* driver is that, during the on-state, a positive voltage +5V, using a voltage regulator, is applied to the gate in order to forward bias the gate. Moreover, for safety reasons explained below, a resistance R_c was added in series with the diode D_1 in order to limit the conduction current. This circuit applied both in Depletion Mode (DM)

SJDP120R085 *SiC JFET* and Enhancement Mode (EM) SJEP120R100 by modifying only the values of the R-C-D network. The exact value of the elements and the resulting gate currents for each device are given in *Table 5*.

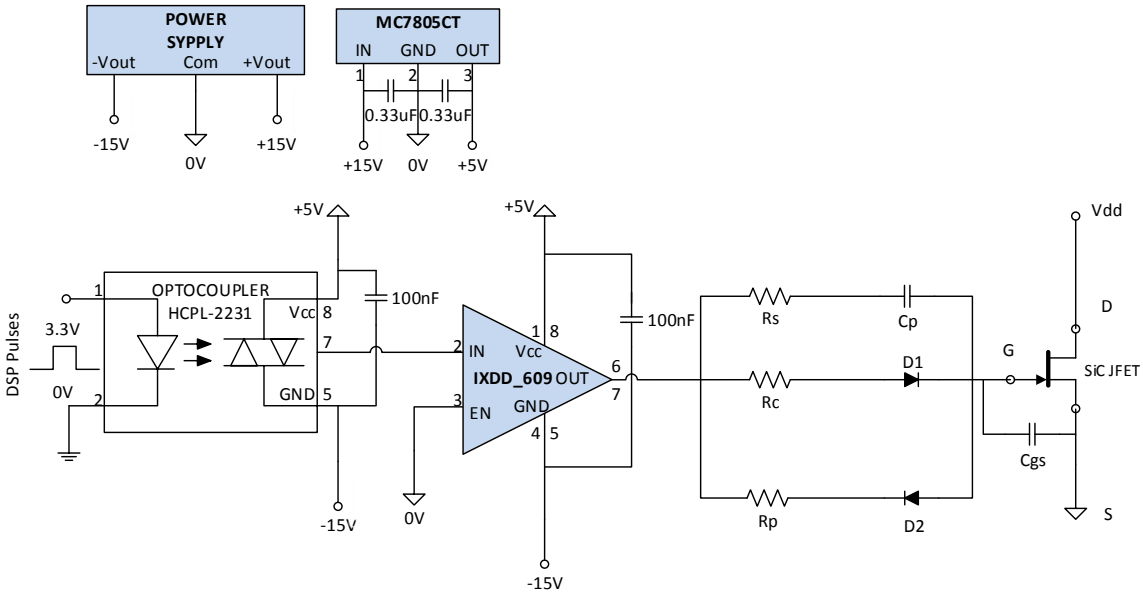


Figure 83.AC-coupled gate drive circuit with forward bias

Circuit Schematic; The proposed circuit is shown in Figure 83. Comparing to the previous simple circuit, it is also composed by an isolated power supply with rated voltage ± 15V, an optical isolator HCPL-2231 for the isolation of the control signal, an IXDD_609 for amplifying the current as well as a capacitor C_{gs} to avoid the Miller effect and voltage overshoots and decoupling capacitors in the voltage pins of the IC. On the contrary, a modified *R-C-D* network was used in order to exploit the reduction of the channel resistance in case of forward bias. The voltage +5V was supplied by the voltage regulator MC7805CT.

Operation; A standard gate driver IC IXYS is supplied with a differential voltage V_{CC} *(+5V)*– V_{EE}*(-15V)* with the midpoint (0 V) connected to the source of the JFET, V_{CC} being close to the desired gate– source voltage $V_{GS} \approx 3$ V and V_{EE} in the range of −15 V.

During the on-state of the switch, +5V is applied to the gate through the output resistance R_c and a 60V/1A very low V_f Schottky barrier diodes by NXP (PMEG6010) D_1 in order to provide the required dc gate current to the *JFET* during the on-state. As the gate current differs for the two *SiC JFETs* (DM and EM) the desired on-resistance is chosen according to their D_{GS} characteristics. It is worth to point out that the gate-source junction behave like a conventional diode and for this reason the forward bias will not exceed 3 V. Therefore, as happening in a common diode, while increasing bias voltage, the current is increased to a greater degree, so during the conduction mode the gate current must be limited in order to protect the semiconductor. Therefore during the on-state, diode D_2 prevents the flow of the gate current through this branch and the current is limited by the resistance R_c.

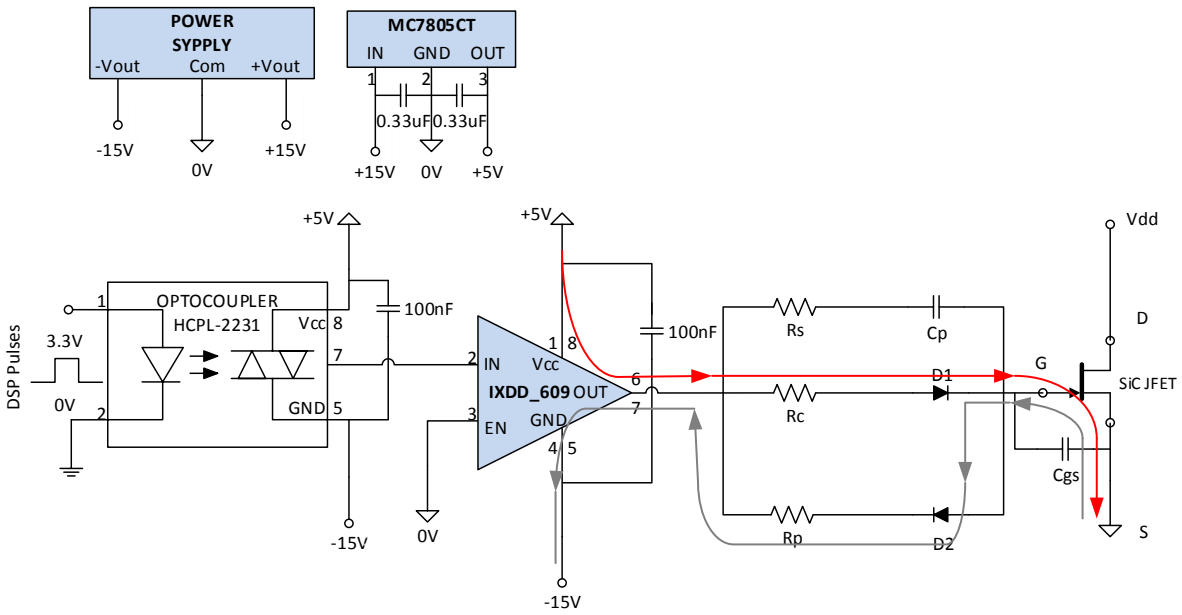


Figure 84. Red line describes the route of the current during the conduction state and the grey one the steady cut-off state.

During the off-state of the device, the output voltage of the gate driver IC is at -15V which fulfils the requirement of negative bias at the gate during the off-state and D_2 makes sure that no current flows through other branch during the off-state. To make sure that the Miller effect does not take influence and, thus, a large portion of the current charging C_{GD} during the off-state of the device can flow to the source of the JFET without flowing through the internal C_{GS} of the JFET, the proposed gate driver has the external capacitance C_{GS}.

During turn-on of the JFET, the voltage +5V is applied to the gate terminal for fast charging of the JFET's input capacitance while discharging C_p. To dampen oscillations or to slow down the switching speed, a resistor R_s can be connected in series to C_p.

During turn-off, the required negative bias can be applied to the gate while the R_s and C_p provide a low-impedance path for fast turn-off of the channel. The state of charge of C_p imposes duty cycle and frequency limitations because if the on/off-time of the *JFET* is low, C_p is not fully charged/discharged which would cause an additional voltage drop or a delay for the on/off state. The problem on this issue is given on the next section by the DC-coupled gate drive circuit.

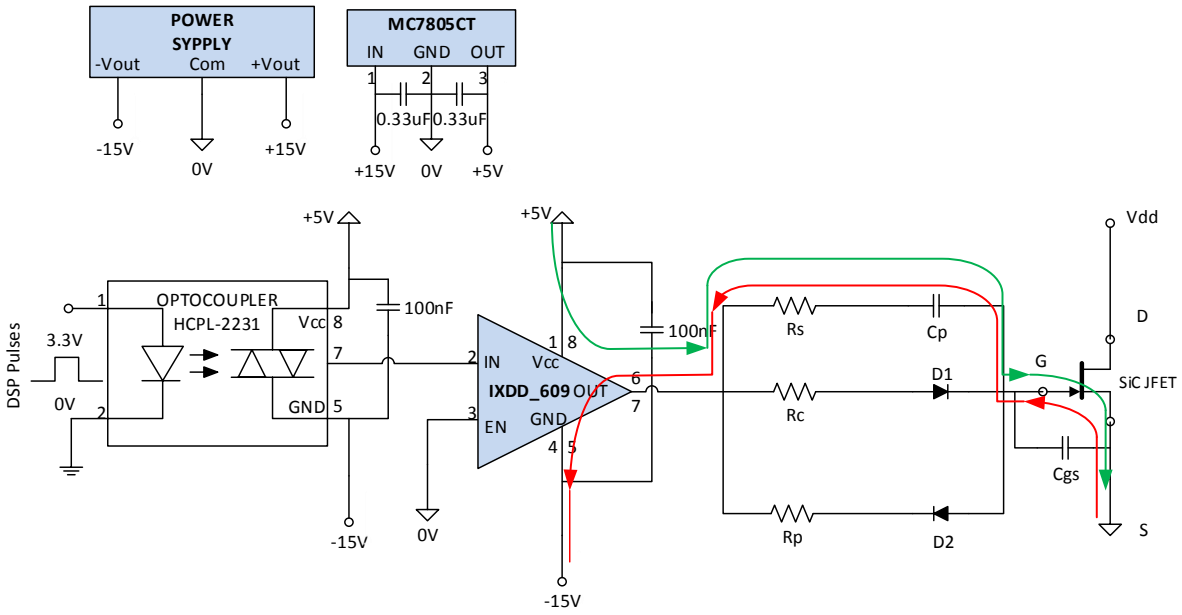


Figure 85. Green line describes the turn-on procedure; red line the turn-off.

To sum up, the proposed gate drive is composed by three branches. The first one with the R_s and C_p is for the fast turn-on and off offering low impedance route for the current until the capacitor is fully charged or discharged. The capacitor should be approximately equal to the internal capacitance C_{iss} while R_s is useful for the reduction of the voltage oscillations. The second branch is for the steady conduction state and is possible to control the value of the gate forward current by modifying the R_c so that there will be no large currents which could destroy the gate. Finally, the R_p branch offers a high impedance route to limit the gate terminal current in case it is transiently broken down into avalanche by the gate-driver. On the following table, the various parameters for both devices for the specific gate drive are computed and presented.

Element	DM SJDP120R085	EM SJEP120R100
Decoupling Capacitors	100nF	100nF
Diodes D_1, D_2	PMEG6010	PMEG6010
C_{gs}	1nF	1nF
R_s	5Ω	2Ω
C_p	$\frac{2Q_g + Q_{Cgs}}{V_{DD} - V_{GS}} \leq C \leq \frac{4Q_g + Q_{Cgs}}{V_{DD} - V_{GS}}$ $27.6nF \leq C \leq 55.2nF$ $C=47nF$	$\frac{2Q_g + Q_{Cgs}}{V_{DD} - V_{GS}} \leq C \leq \frac{4Q_g + Q_{Cgs}}{V_{DD} - V_{GS}}$ $70\ nF \leq C \leq 130\ nF$ $C=94nF$

R_c(for low forward current)	100 Ω	20 Ω
R_p (for low cut-off current and temperature protection)	3 kΩ	3 kΩ
Required Peak current for Δt=50 ns, I_{peak}	$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{75nC}{50ns} = 1.5A$	$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{110nC}{50ns} = 2.2A$
Forward gate current, I_{FWD}	$I_{gFWD} = \frac{V_o - V_{gs} - V_{D1}}{R_c} = \frac{5 - 2.5 - 0.5}{100} = 20mA$	$I_{gFWD} = \frac{V_o - V_{gs} - V_{D1}}{R_c} = \frac{5 - 2.5 - 0.5}{20} = 100mA$
Cut-off gate current, I_{cutoff}	0.75 mA	100 mA
Charging constant, $\tau = R_s C_p$	235 ns	188 ns
Total considered gate charge, Q_g	75 nC	110 nC
On-state Voltage	2.7 V	2.7 V
Off-state Voltage	-15 V	-15 V

Table 5. Calculation of the various parameters for the AC-coupled gate drive with forward bias.

3.3.3 DC Coupled drive circuit With Forward Bias

The driver circuits based on AC coupled logic are widely used for driving *SiC JFETs* because of the simplicity of construction and operation and low cost, but as mentioned before, they are not the optimal choice for all levels of pulse width and switching frequencies. In high frequency applications, it is required an optimized driver circuit which is independent of the charging and discharging time constant $\tau = RC$, for better performance. The solution to this problem is a DC coupled circuit drive with two levels optimized for high-speed and hard-switching operations. A two-stage, DC-coupled driver design has been developed specifically for the *SiC JFET*. The purpose of this driver is to first apply a high peak current pulse for supplying the required dynamic charge as quickly as possible for a fast turn-on. Then secondly maintain the steady state DC gate voltage/current to sustain conduction.

Circuit Schematic; The proposed drive circuit is shown in Figure 86 and the PCB in Figure 99. Accordingly to the previous drive circuit, it, also, uses an isolated power supply which is supplied externally, in order to provide voltage ± 15V to the circuit, as well as, a +5 V voltage

regulator in order to achieve the forward bias of the *SiC* device. The control signal is isolated via an optical isolator HCPL-2231 enabling fast switching speeds and allowing layout spacing to meet safety isolation requirements, while in contrast to previous circuits; the DC coupled drive circuit uses two current amplifiers IXDD_609. The presence of the second current amplifier is justified by the operation mode of the circuit, which is separated into two levels as will be mentioned below. Finally, four logic gates were used in order to synchronize the output signals of the two ICs.

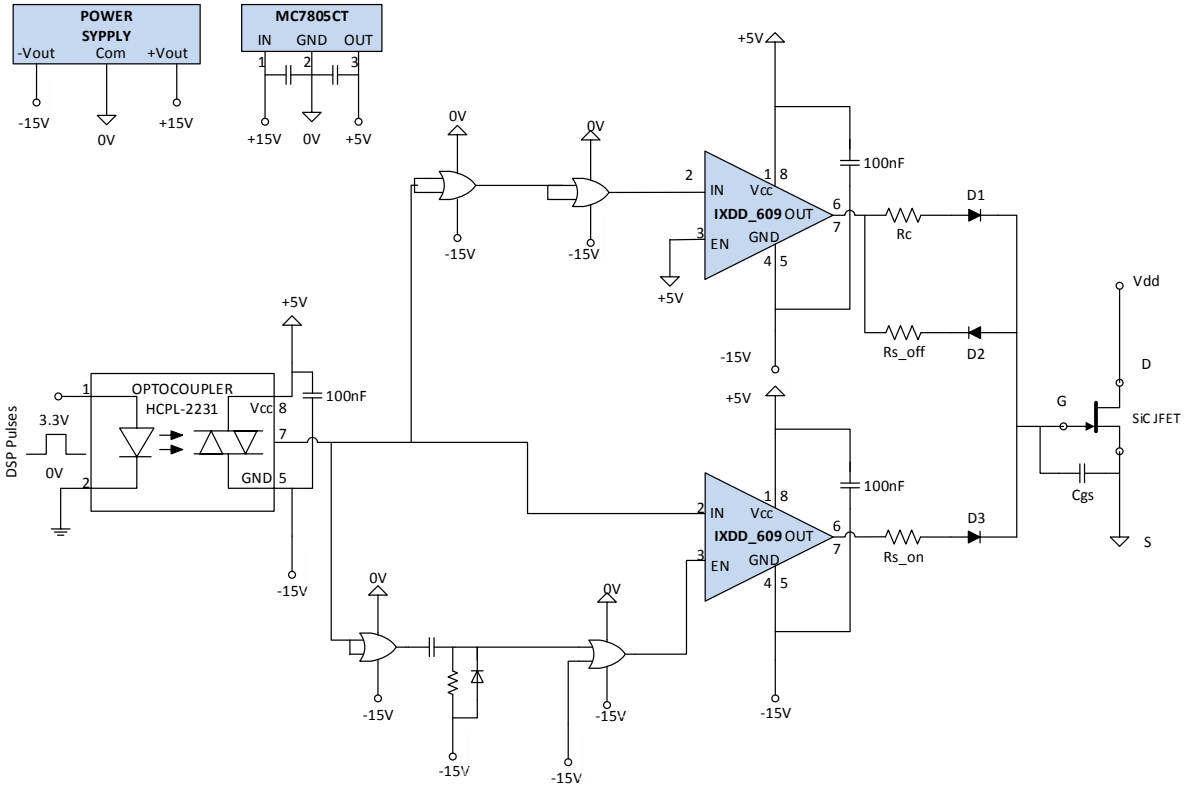


Figure 86.Dc-coupled gate drive circuit with forward bias

Operation; During the turn-on and off, the operation of this circuit is based on creating a short-duration pulse, by a logic circuit composed by logic gates and a filter RC, synchronized with the initial pulse. The pulse duration generated by the logic circuit will be approximately 150ns and will be driven to the ENABLE input of the current amplifier. Thus, for 150ns the ENABLE pin remains to logical HIGH and as a result the amplifier provides large current spikes for fast charging of the *SiC* parasitic capacitances. In the rest time interval the ENABLE equals to logical LOW, and the output of the amplifier is high Z, which is equivalent to open circuit. Thus, the generated pulse drives a first turn-on stage which controls delivery of dynamic gate charge. The upper IXDD connects a high peak current source for quickly charging the device's gate and miller capacitance at turn-on.

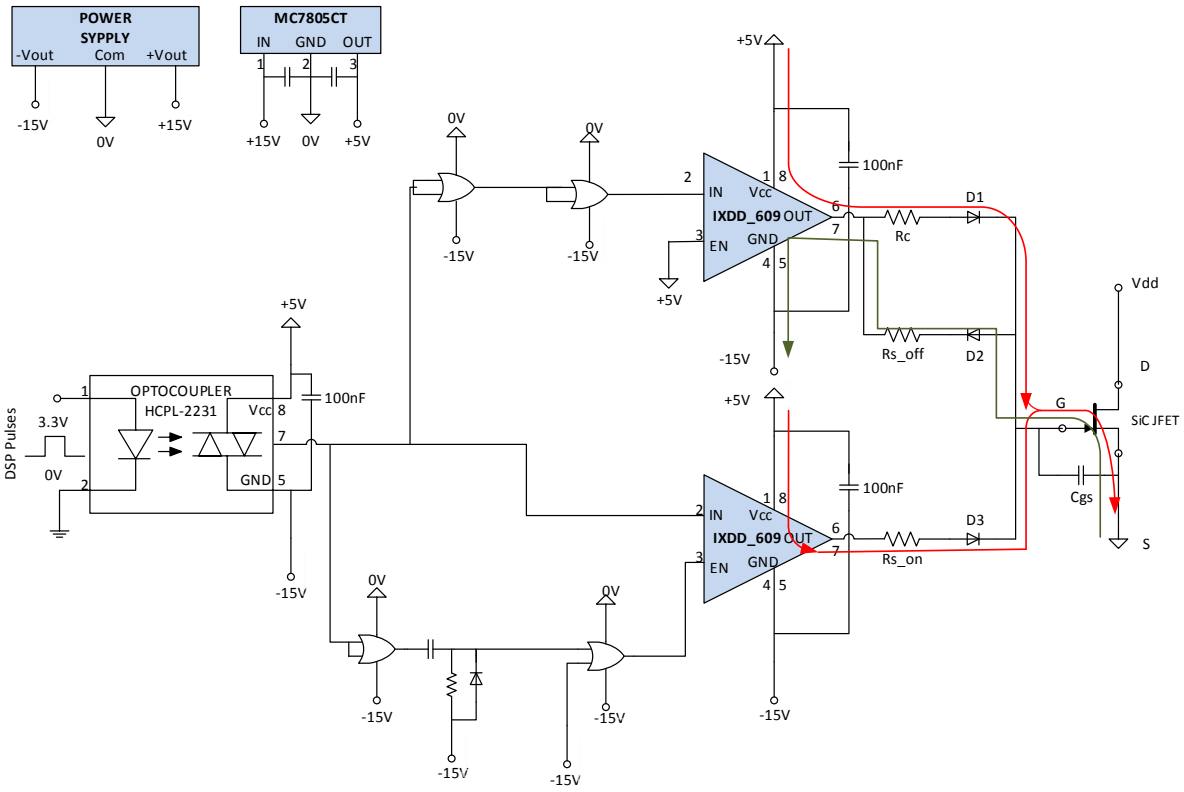


Figure 87. The red line denotes the turn-on state and the green one the turn-off.

The input to the other amplifier is given by the initial pulse from the optocoupler and passes through a couple of logic gates without modifying the signal but creating an artificial delay so that the two amplifiers are synchronized. This amplifier will provide 5V at conduction state and -15V at cutoff state. However, in contrast to an *R-C-D* drive circuit, this particular drive circuit consists of two branches which conduct at different switching states. The original control pulse is applied to the second turn-on stage, where the second IC supplies the necessary steady state DC gate current required to maintain conduction. Current limiting resistors R_c and R_{s_off} are properly sized to set the forward gate current I_{GFWD}. Both resistors are sized with the same approach used for the current limiting resistor in the AC-coupled RC drive circuit.

During the transition to the cutoff state the current amplifier provides -15V negative voltage to the gate in order to quickly discharge the parasitic capacitances, while in the cut-off state, the gate current will continue to flow through this branch. The value of the resistance R_{s_off} should be low so that it provides a low ohm path and the transaction to the cut-off state will be fast. Nevertheless, the small value of R_{s_off} results in the lack of security in the case of the breakdown of the gate – source junction. Choosing a larger value provides protection from collapse, but the transactions would be slow which is not desirable. The

diodes D_1 and D_3 aim at preventing current flow through these branches at the cutoff state of the device.

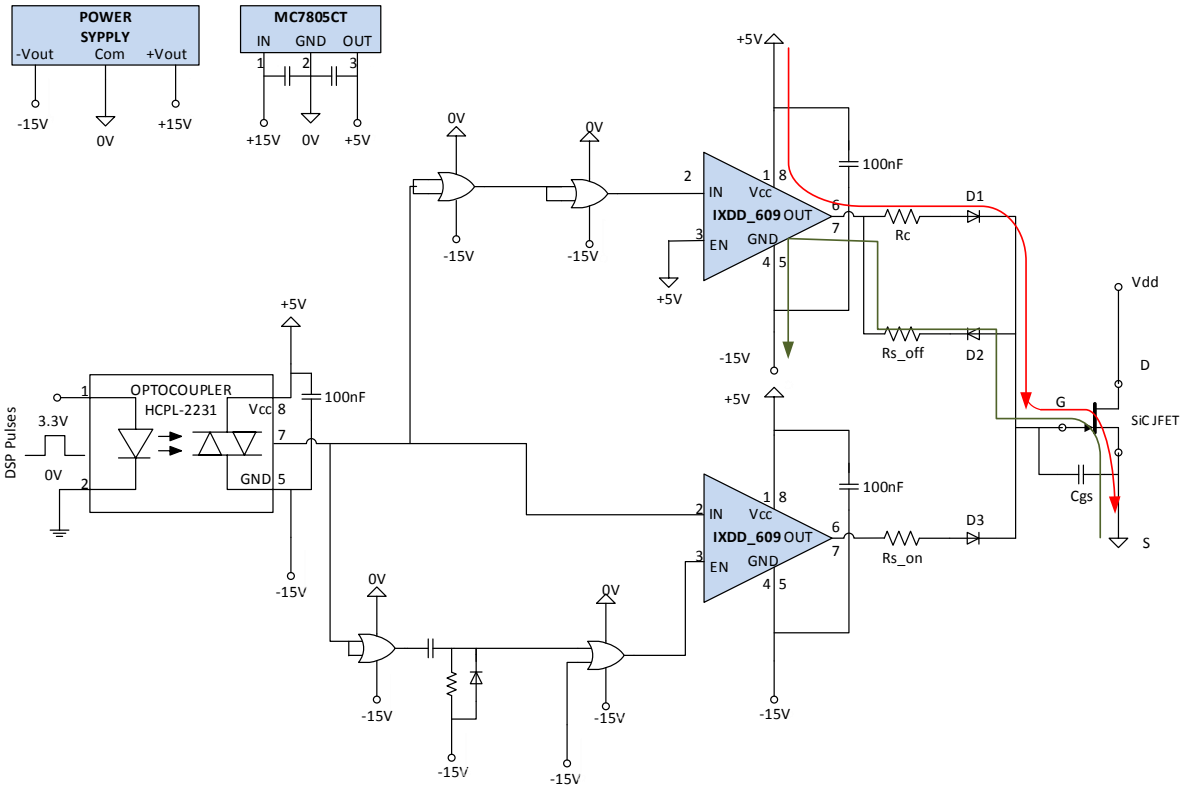


Figure 88. The red line denotes the conduction state and the green one the cut-off.

At the transition to the conduction state, as mentioned above, for an interval of approximately 150ns both current amplifiers provide 5 V at the *SiC JFET* gate. The value of resistance R_{s_on} should be small so that, in period of 150ns where the two branches become parallel, the parallel combination of $R_{s\_on} \| R_c$ to be low in order to provide the necessary current spikes to the gate for fast charging of the internal parasitic capacities. The diode D_2 aims at preventing current flow through this branch at this state.

In steady conduction state, when the output of the amplifier is high Z, the other amplifier provides positive voltage +5 V via the resistor R_c to the gate in order to forward bias the device. The resistor R_c should limit the gate current at this state as in the previous cases.

To sum up, to meet the different requirements for transient turn-on and turn-off, on the one hand, and the steady on-state, on the other hand, a two-stage gate driver has been proposed on this section. One stage supplies a short pulse with a high voltage (around 5 V) for turn-on and a second stage delivers the dc gate current for the on-state (at a gate–source voltage $V_{GS} \approx 3$ V) from the same supply voltage rail via a resistor (causing high losses in that resistor due to high voltage drop across it and high gate current flowing through the resistor). The second stage is either realized by a second output of a dual gate driver IC

connected to the supply voltage of the gate driver. The control of the second stage is realized by an additional logic IC.

Element	DM SJDP120R085	EM SJEP120R100
Decoupling Capacitors	100nF	100nF
Diodes D_1, D_2 , D_3	PMEG6010	PMEG6010
R_c(for low forward current)	100 Ω	20 Ω
R_{s_off}	5 Ω	2 Ω
R_{s_on}	5 Ω	2 Ω
Required Peak current for Δt=50 ns, I_{peak}	$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{75nC}{50ns} = 1.5A$	$I_{peak} = \frac{\Delta q}{\Delta t} = \frac{110nC}{50ns} = 2.2A$
Forward gate current, I_{FWD}	$I_{gFWD} = \frac{V_o - V_{gs} - V_{D1}}{R_c} = \frac{5 - 2.5 - 0.5}{100} = 20mA$	$I_{gFWD} = \frac{V_o - V_{gs} - V_{D1}}{R_c} = \frac{5 - 2.5 - 0.5}{20} = 100mA$
Total considered gate charge, Q_g	75 nC	110 nC
On-state Voltage	2.7 V	2.7 V
Off-state Voltage	-15 V	-15 V

3.4 Experimental Evaluation

On this section, separate results for each device are presented while in the next paragraph a comparison study is done. A thorough experimental evaluation was carried out with the various gate-drive circuits and double-pulse tester built for the *SiC JFET*, in an effort to evaluate the performance of both the device and the circuit physical layout. The switching and conducting performance of the proposed gate drives were investigated in the experimental setup illustrated in Figure 89. It is a common double pulse tester consisting of a 200 V_{dc} source, a bulk 235 μF capacitor, a one film ceramic 4.7 μF capacitor, a 115 μH inductor and two freewheeling diodes. The double pulse square wave was formed via a digital controller from Texas Instruments. In order to face voltage overshoots and ringing effects, particular emphasis was placed on minimizing parasitic elements. For this the complete driving and protection circuit was constructed with surface mounted devices

(SMD) in order to minimize stray inductances. Moreover, the physical distance between the driver IC, the capacitor C_g and the power device was minimized.

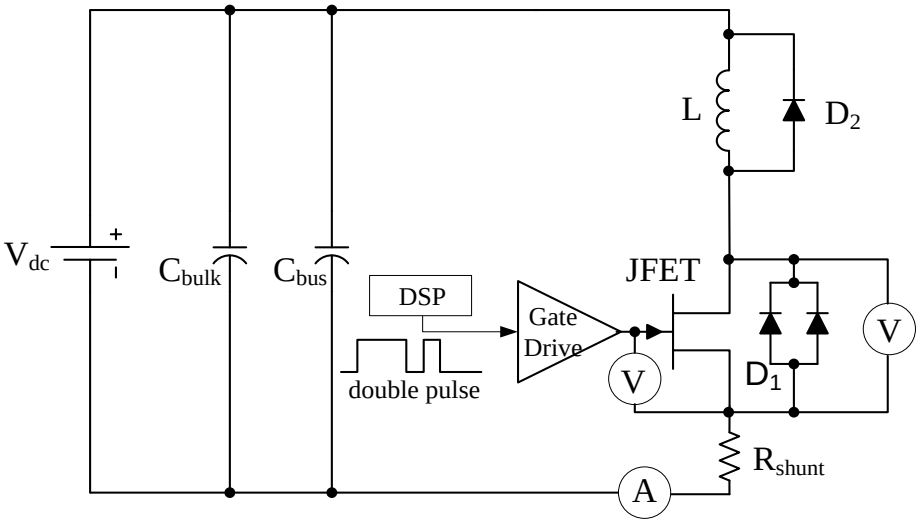


Figure 89. Double pulse tester circuit

Double-pulse clamped inductive load transistor test as shown above is an efficient method to investigate the switching times, energies, turn-on and turn-off power loss and conduction loss of power electronic devices under testing at different current and voltage levels. Integrated with the oscilloscope power measurement software was used to acquire switch power dissipation and switching energies.

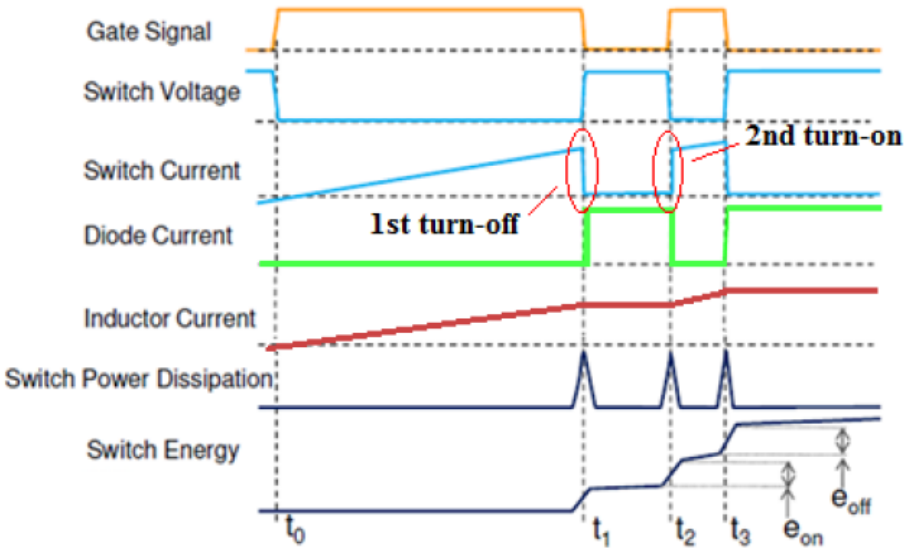


Figure 90. Principles waveforms during double-pulse test.

The gate drive circuit is connected to transistors gate, and a double-pulse is applied. The two pulses are composed by one long pulse followed by a fairly short pulse. This allows stressing the transistor by turning on and turning off at rated current. The typical current and voltage waveforms can be observed in *Figure 90*, the power dissipation and energy loss of transistor can be calculated using equations (70)-(75) as well as (82)-(84). Energy loss is the integral of power dissipation.

The power can be calculated by using the following equations,

$$P = V(t) \times I(t) \qquad (82)$$

where $P \longrightarrow$ switching power dissipation, $V(t) \longrightarrow$ instantaneous transistor voltage, $I(t) \longrightarrow$ instantaneous transistor current.

The turn-on/off energy is the energy dissipated inside the transistor during the turn-on/off of a single drain current pulse which can be calculated by using equation

$$E_{on} = \int_{t_{on}} V(t)I(t)dt \qquad (83)$$

$$E_{off} = \int_{t_{off}} V(t)I(t)dt \qquad (84)$$

where E_{on} , E_{off} the turn-on and turn-off energies.

Finally, the experimental results for all the three gate drive circuits are presented for both the *SiC JFETs*. The double pulse test operated for V_{ds}=200V and $I_d \approx$ 4A

3.4.1 R-C-D gate drive circuit without forward bias

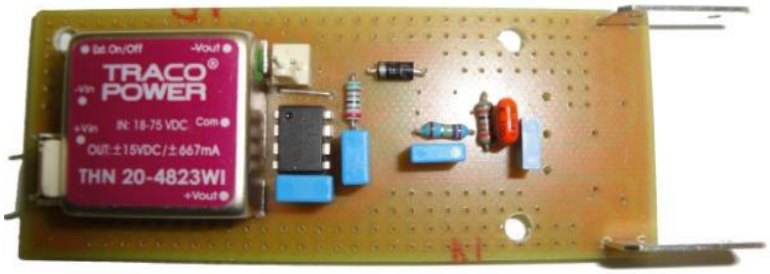


Figure 91. Physical layout of AC Coupled without forward bias gate drive PCB circuit.

Depletion Mode SiC JFET SJDP120R085

Figure 92 depicts the turn on characteristics of the proposed driving circuit and Figure 93 shows the turn off transients when operating at double pulse tester at 200 V_{dc} and 4 A load current for the DM *SiC JFET*.

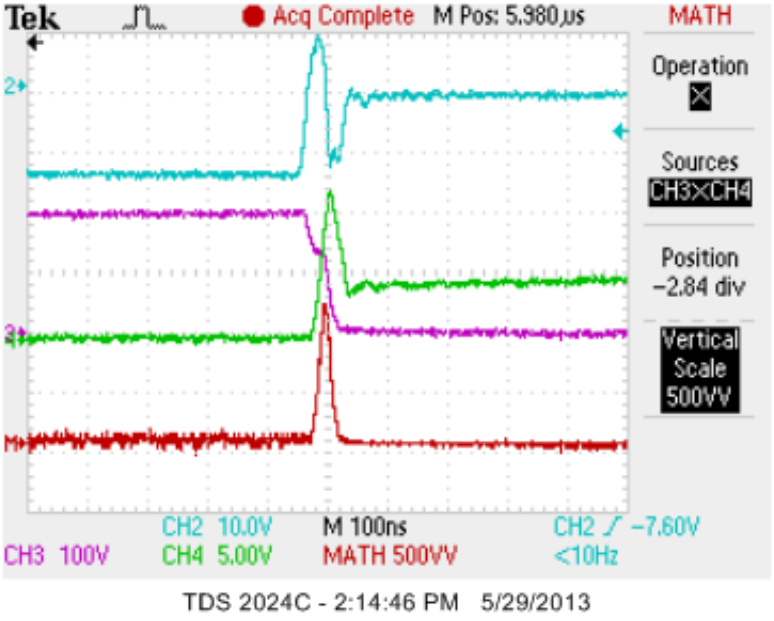


Figure 92. Turn on transients. Gate-source voltage (CH2– 10V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5 A/DIV) and switching energy (MATH - 500W/DIV).

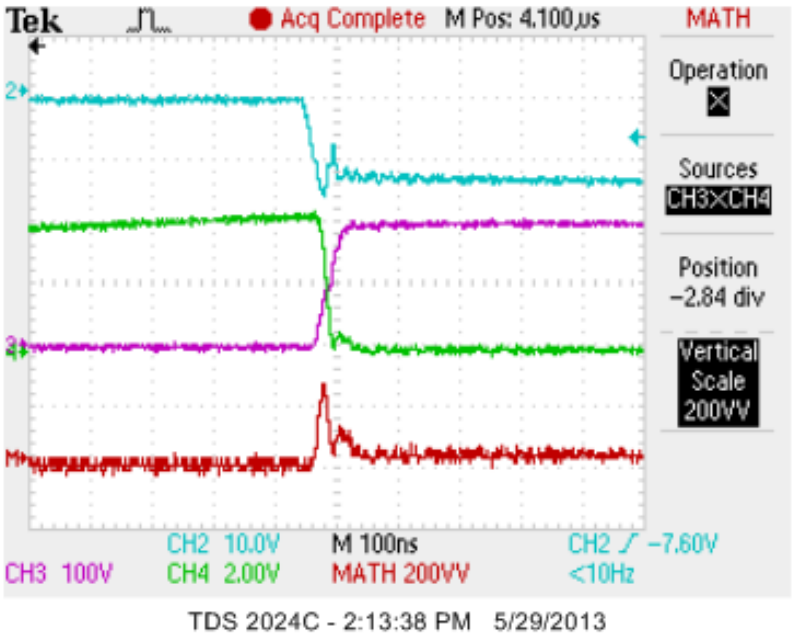


Figure 93. Turn off transients. Gate-source voltage (CH2– 10V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 2A/DIV) and switching energy (MATH - 500W/DIV).

3.4.2 AC-coupled gate drive circuit with forward bias

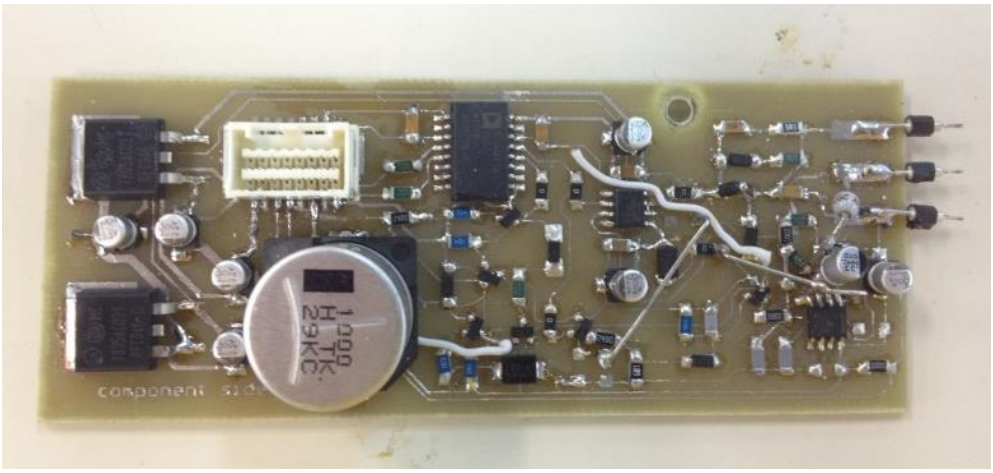


Figure 94. Physical layout of AC Coupled with forward bias gate drive PCB circuit.

Figure 95, Figure 96 depict the switching characteristics of the proposed driving circuit at the same circumstances for the Normally-on and Figure 97, Figure 98 for the Normally-off.

Depletion Mode SiC JFET SJDP120R085

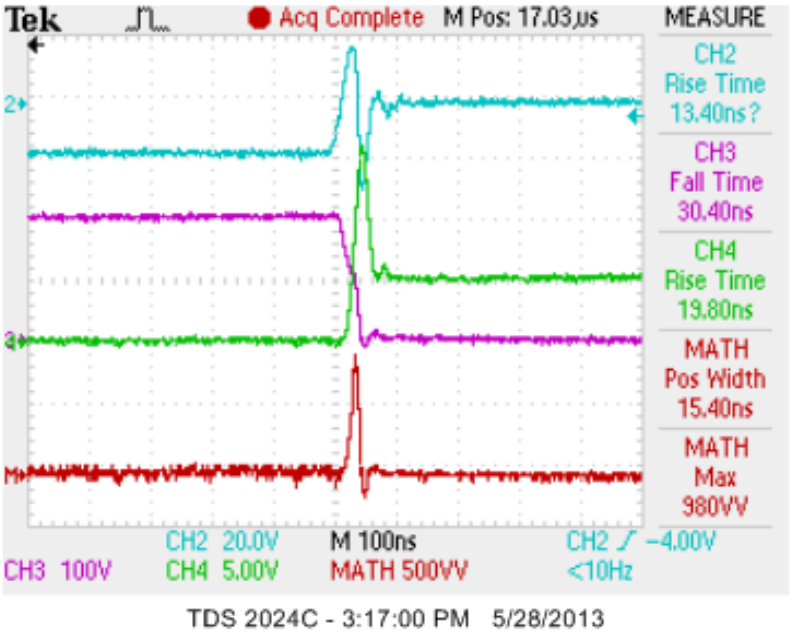


Figure 95. Turn on transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5A/DIV) and switching energy (MATH - 200W/DIV).

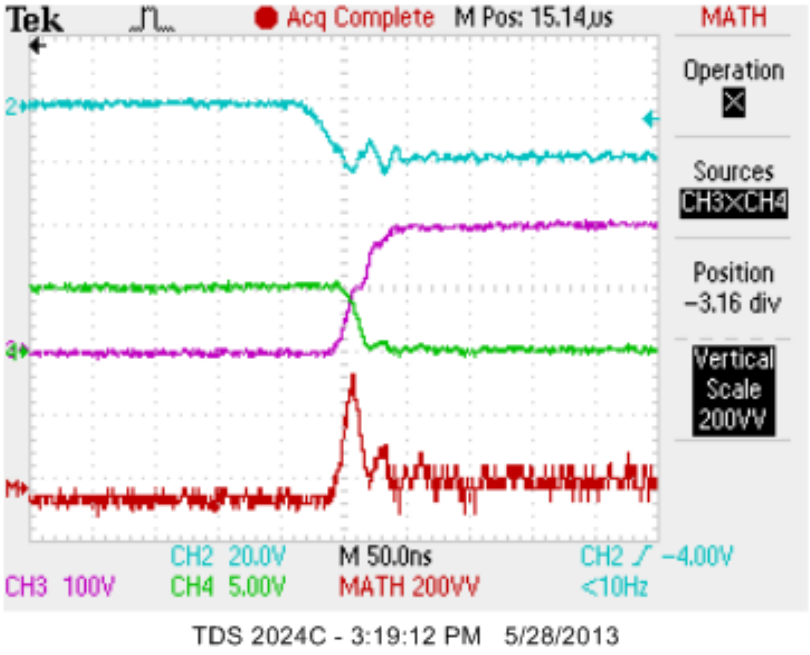


Figure 96. Turn off transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5A/DIV) and switching energy (MATH - 200W/DIV).

Enhancement Mode SiC JFET SJEP120R100

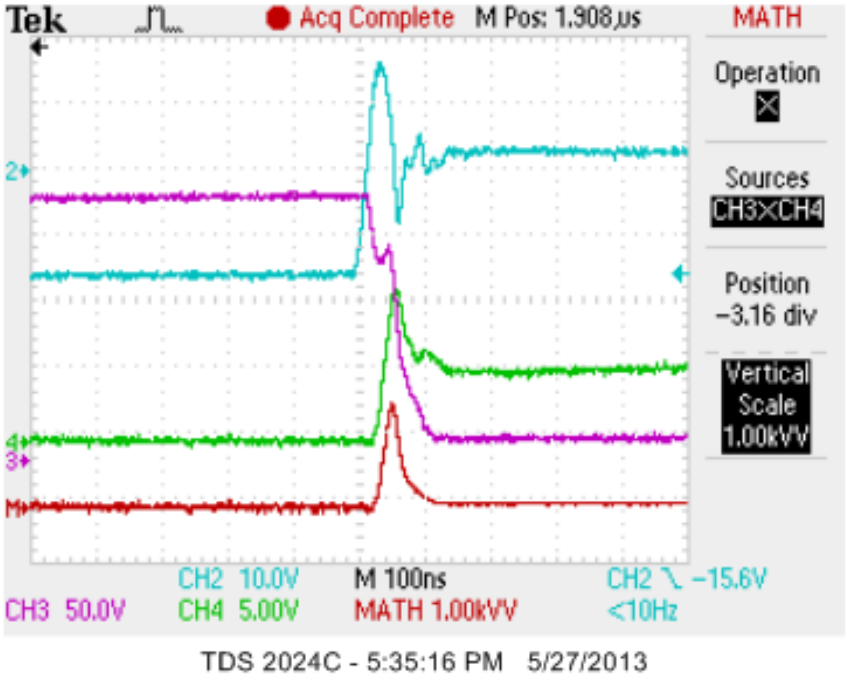


Figure 97. Turn on transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5A/DIV) and switching energy (MATH – 1kW/DIV).

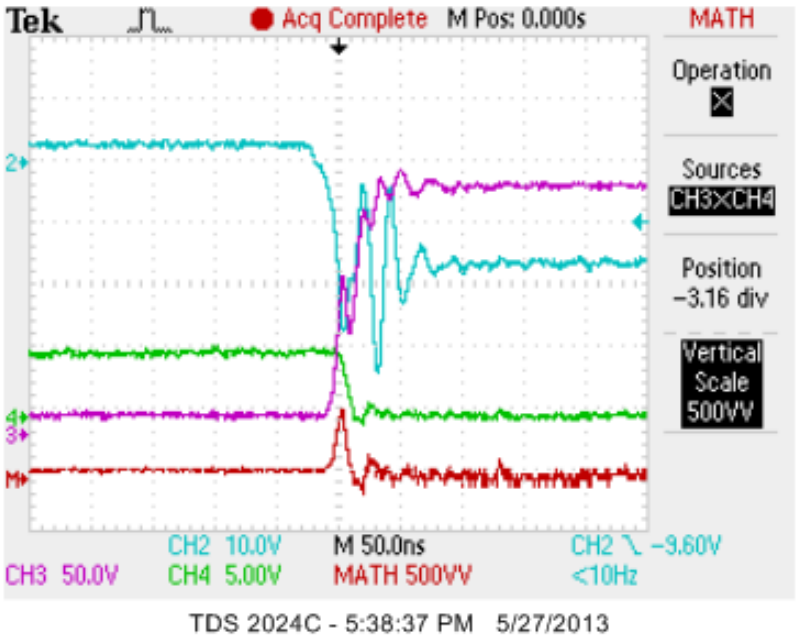


Figure 98. Turn off transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5A/DIV) and switching energy (MATH - 500W/DIV).

3.4.3 DC-coupled gate drive circuit with forward bias

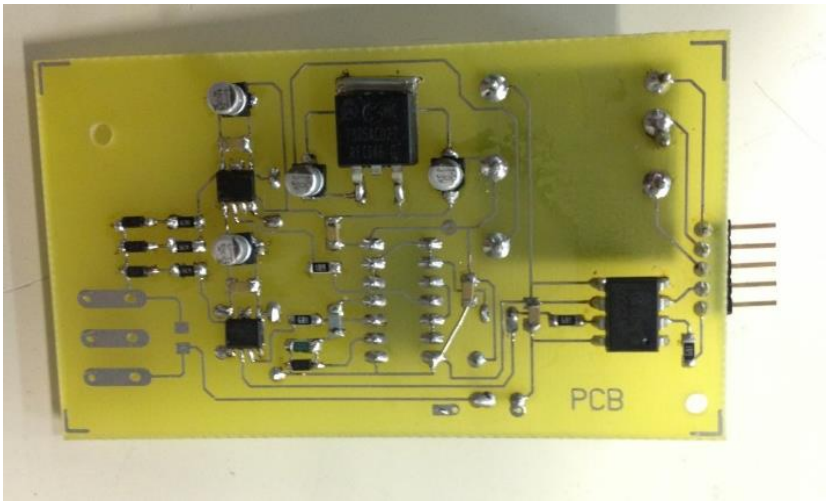


Figure 99. Physical layout of DC Coupled with forward bias gate drive PCB circuit.

Figure 100, Figure 101 depict the switching characteristics of the proposed driving circuit at the same circumstances for the Normally-on device while in Figure 102, Figure 103 the equivalent plots for the Normally-off.

Depletion Mode SiC JFET SJDP120R085

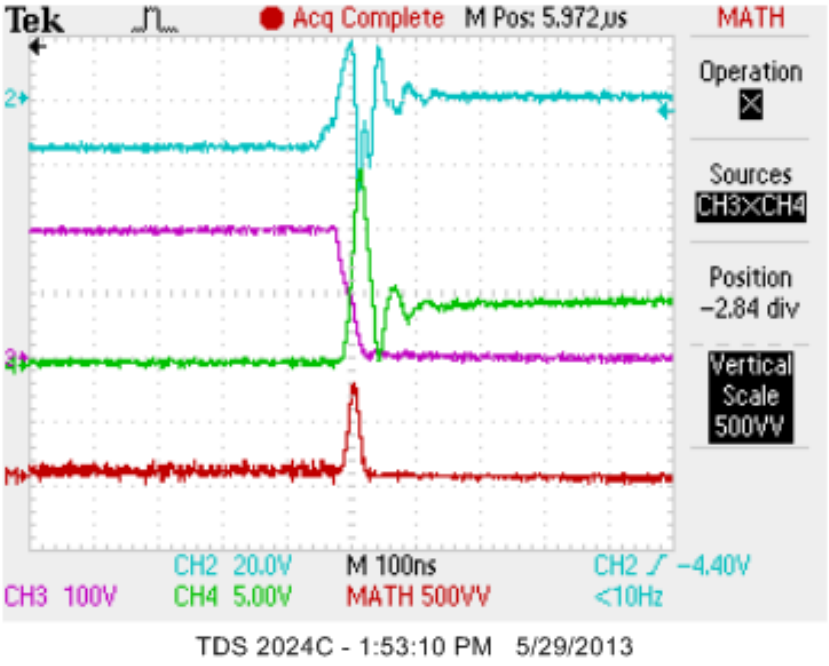


Figure 100. Turn on transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 5A/DIV) and switching energy (MATH - 500W/DIV).

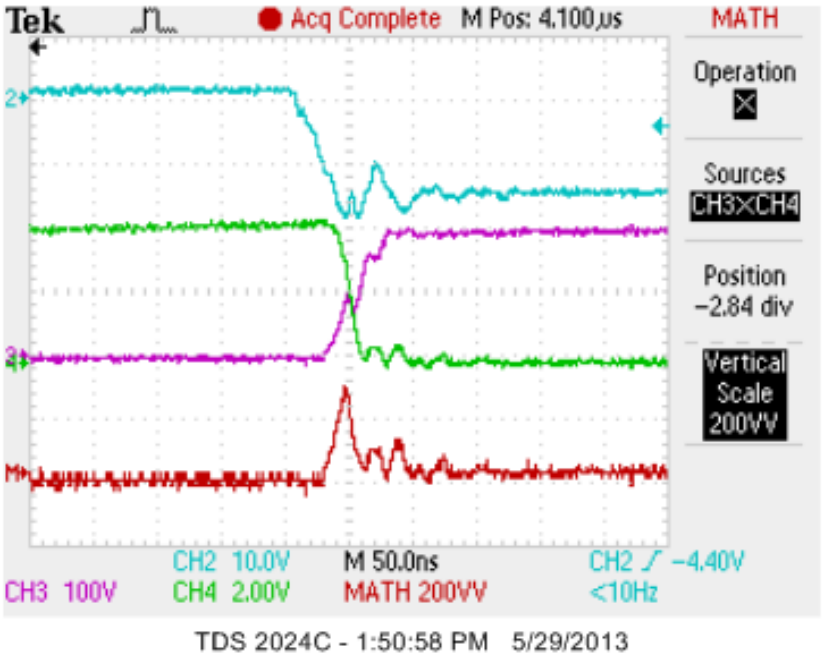


Figure 101. Turn off transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 2A/DIV) and switching energy (MATH - 200W/DIV).

Enhancement Mode SiC JFET SJEP120R100

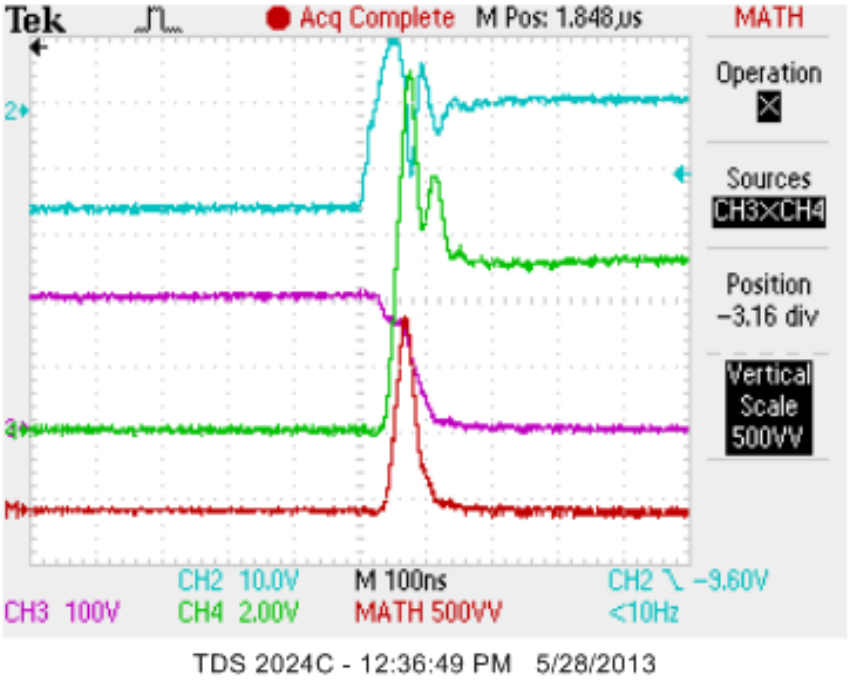


Figure 102. Turn on transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 2A/DIV) and switching energy (MATH - 500W/DIV).

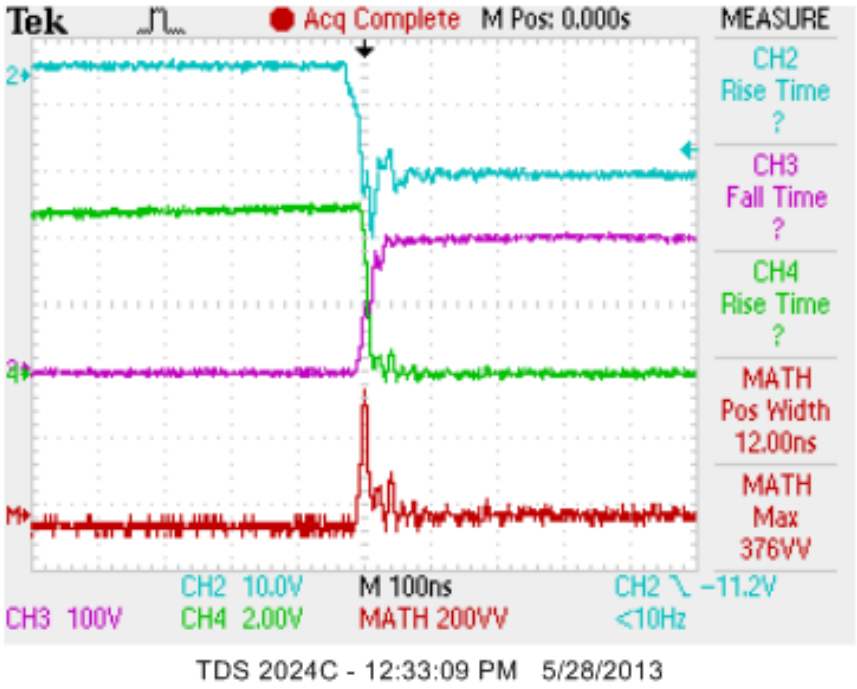


Figure 103. Turn off transients. Gate-source voltage (CH2– 20V/DIV), drain voltage (CH3 – 100V/DIV), drain current (CH4 – 2A/DIV) and switching energy (MATH - 200W/DIV).

3.5 Comparison study

Comparison of SiC JFETs

An evaluation of the switching losses and the switching times that were measured above is done on this paragraph. The results are shown in the following table. To begin with, it is demonstrated that the results for the AC-coupled gate drive circuit are much better than the DC coupled one exhibiting up to 10% better switching times and less than 15% energy losses. Consequently, the gate drive of our choice for future converter systems would be the AC coupled with forward bias.

VT SiC JFET	Switching Characteristics			
	t_{on} (ns)	E_{on} (uJ)	t_{off} (ns)	E_{off} (uJ)
AC Coupled with forward bias				
DM JDP120R085 SiC JFET	60	27	70	7.4
EM SJEP120R100 SiC JFET	100	60	60	8
DC Coupled with forward bias				
DM SJDP120R085 SiC JFET	80	20	75	7
EM SJEP120R100 SiC JFET	100	75	70	9.5

Table 6. Switching characteristics comparison.

In addition, we have to point out the superior performance of the normally-on *SiC JFET*. It has approximately 40% faster turn-on and off times while the normally-off device exhibits 70% more energy losses. With such impressive results it is undeniable that the DM *SiC JFET* may play a significant role in future power converters.

Then, a comparison between the gate drive circuits only for the DM *SiC JFET* is done in order to choose the most appropriate design for the inverter implementation.

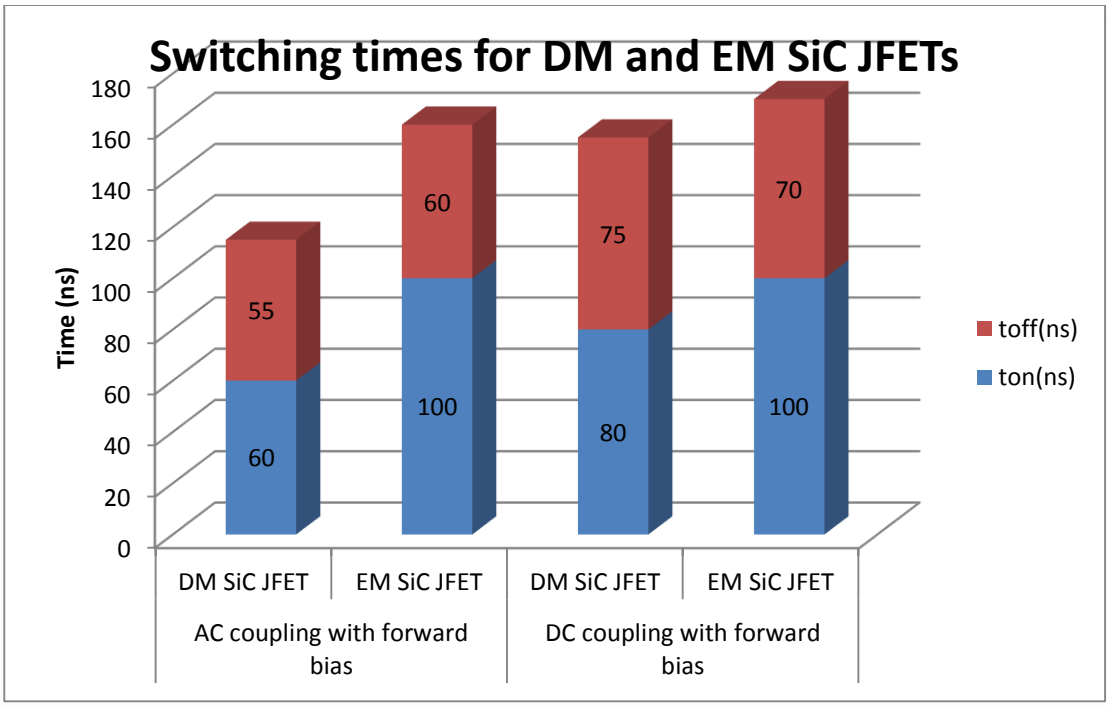


Figure 104. Switching times in ns for DM and EM SiC JFET for the two gate drive circuits with forward bias.

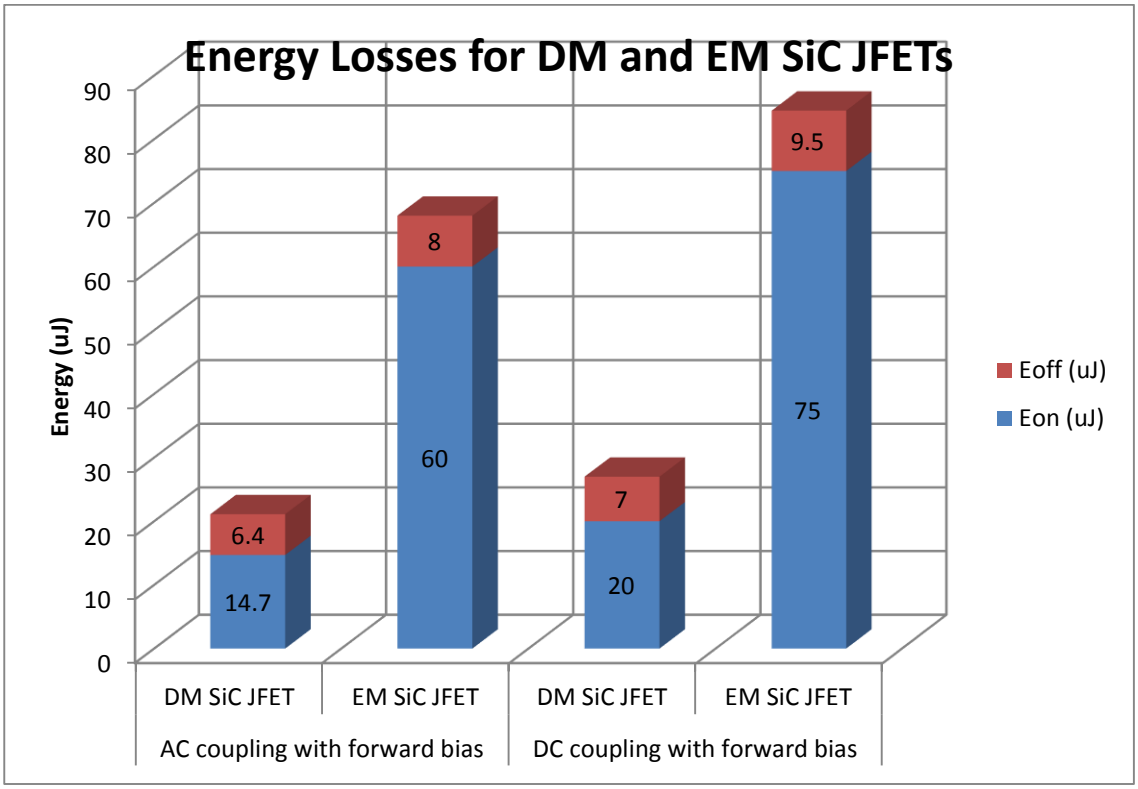


Figure 105. Switching Energy losses in uJ for DM and EM SiC JFET for the two gate drive circuits with forward bias.

Comparison of gate drive circuits

In the previous section we have analysed the structure and the operation of three different gate driving schemes while in this paragraph we compare the above results. It is shown on the Table 7 that the ac coupled without forward bias exhibits the worst behavior of the proposed gate drives although it is one of the most known and used in the literature. This is due to the fact that it doesn't exploit the favorable characteristics of the SiC JFET during the forward conduction by biasing the gate.

On the other hand by using the ac coupled with forward bias a reduction in energy losses of 38.66% is achieved in comparison to a zero bias scheme and 20% in relation to the dc coupling logic. In addition it is also demonstrated that by applying a positive bias a reduction of more than 30% is performed in the switching times.

As far as the comparison between the AC Coupled with forward bias and DC Coupled with forward bias gate drive circuits is concerned, it can be noticed that there are no remarkable differences in their performance, with the first one to exhibit a slightly better performance, about 6uJ less total energy loss. However, the decision is under the jurisdiction of the designer if he needs a more stable behavior over all levels of pulse widths and switching frequencies (dc coupling) or a lower construction cost, simplicity design and protection from large gate currents in breakdown (ac coupling). The entire above mentioned are presented graphically in Figure 106 for better understanding.

Drive Circuit	Switching Characteristics			
	t_{on} (ns)	E_{on} (uJ)	t_{off} (ns)	E_{off} (uJ)
Normally – On SJDP120R085 SiC JFET				
AC Coupled without forward bias	60	27	70	7,4
AC Coupled with forward bias	60	14,7	55	6,4
DC Coupled with forward bias	80	20	75	7

Table 7. Summarized experimental drive circuits switching results for Vdc=200V and 4A load current

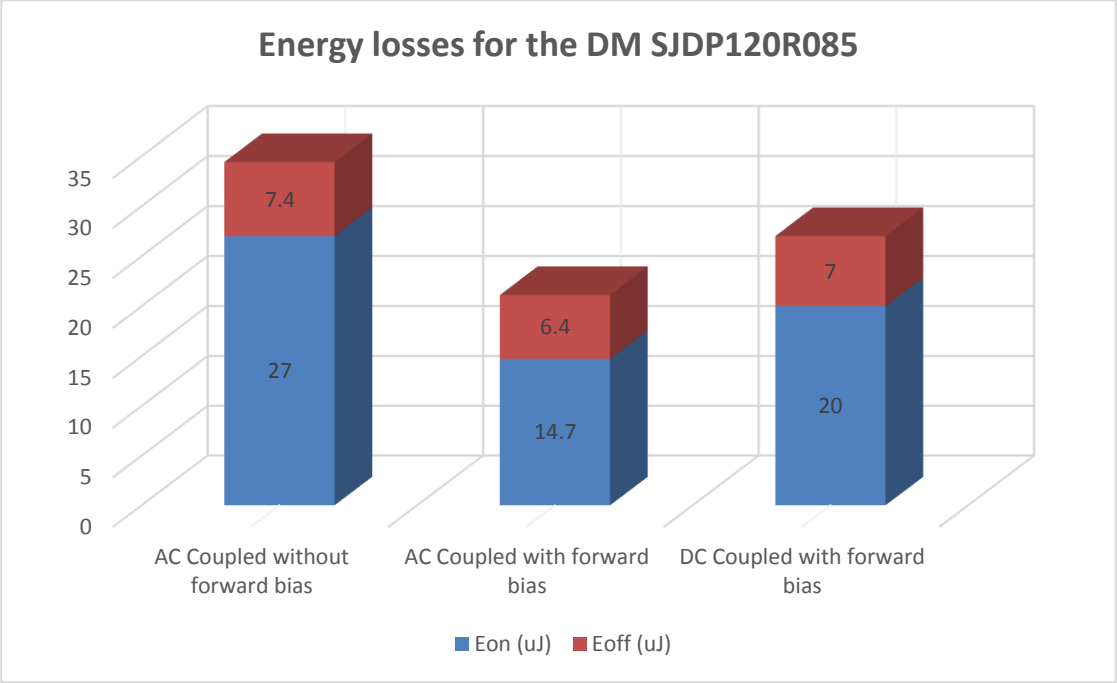


Figure 106. Energy losses for the Normally-on SiC JFET for the proposed gate drive circuits for 200 V_{dc} and 4 A load current.

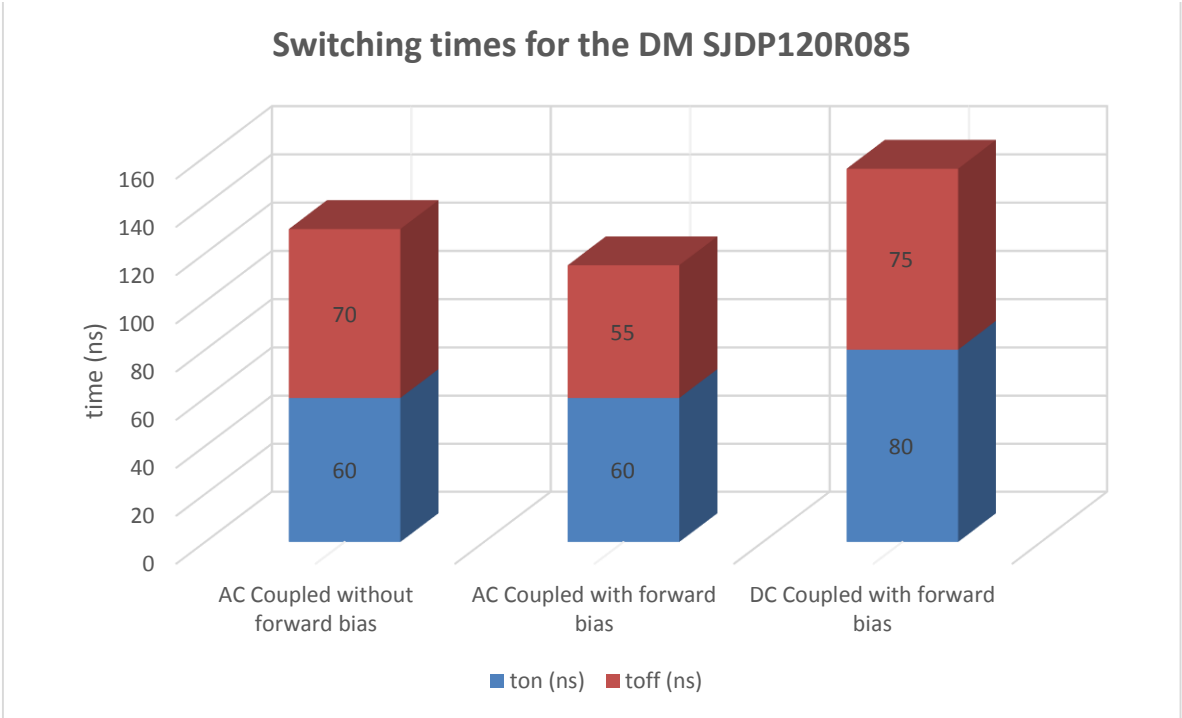


Figure 107. Swithcing times for the Normally-on SiC JFET for the proposed gate drive circuits for 200 Vdc and 4 A load current.

In this chapter, two universal gate drive circuits for both *SiC JFETs* and one only for the Depletion Mode were constructed in order to evaluate their switching characteristics. The better performance that the normally-on device exhibited, leads us to the conclusion that we can reduce the losses in converter applications using these new devices. The future for the new devices and especially for the normally-on *SiC JFET* seems promising. There is no doubt that when the technological and financial issues will be overcome, a new Silicon Carbide era will be established.

3.6 Future trends

The normally ON nature counts as the main factor which keeps this device far from being considered as an alternative to the silicon insulated-gate bipolar transistor. The proposed circuits are able supply the necessary negative gate-source voltage during the steady-state operation. In the opinion of the author, the normally ON JFET is, therefore, preferable if the normally ON problem can be accepted. This is a problem that has to be handled on the system level in such a way that a sufficient reliability can be ensured. This may involve several safety systems, of which some would be used also for normally OFF transistors. A vital unit in such a safety system is an automatic power-up gate driver without the need for external power sources. Such a gate driver should be able to handle the short circuit caused by the normally ON JFETs at start-up and bring them to a stable OFF state. Additionally, it should be capable of driving the JFET during normal operating conditions taking the power from the main circuit.

Consequently, the future gate drive circuits apart from the characteristics that were presented on this chapter should also focus on handling both the start-up and gate-driver power failures of normally ON *SiC JFETs* and be self-powered without external voltage sources. This concept would be extremely important to converters used in space applications or even to isolated regions where there is no network supply.

References

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Chapter 4

MINIMIZING OSCILLATIONS IN POWER CONVERTER APPLICATIONS

Power semiconductors are the heart of power electronics equipment. Switches have been playing a major role in efficient power conversion since 1840 with mechanical switches, through to today's variety of power semiconductor devices. Although the switching device technology has changed dramatically over time, the need to use techniques to reduce switch stress and losses has remained.

The design of switching converters with high performance semiconductors such as the SiC JFets require special attention to detail to maximize the effectiveness of the devices and optimize the overall performance of the switching function. Consideration of the challenges of working with ultra-fast power devices early in the design process will ensure the highest performing, most reliable product. As the performance of SiC power devices is improved, the SiC Jfet has the ability to switch voltages at rates greater than today's usual dV/dt . However, the fast switching faces a common challenge of dealing with switching noise. This noise with the parasitic elements and inductances will result in voltage overshoot and ringing at the switch node.

The scope of this chapter is to introduce and analyse some basic techniques for reducing the oscillations mainly for power converters which exploit the particular characteristics of SiC devices. Through this presentation several advices are given but we focus to a detailed analysis of the snubber formations often used to semiconductors until today. The most suitable snubber circuit for the new Silicon-Carbide JFet technology is proposed. The theoretical results of this chapter have been simulated and ascertained by Pspice in a phase-leg topology and are used in the 1-phase full bridge inverter built in the next chapter.

4.1 Background

To begin with, we have to understand the problem of the ringing phenomenon and the high frequency oscillations. We take for example the formation of a phase-leg inverter [Figure 108] while in Figure 109 a typical output waveform of a half bridge inverter is shown when we don't use any method of damping oscillations.

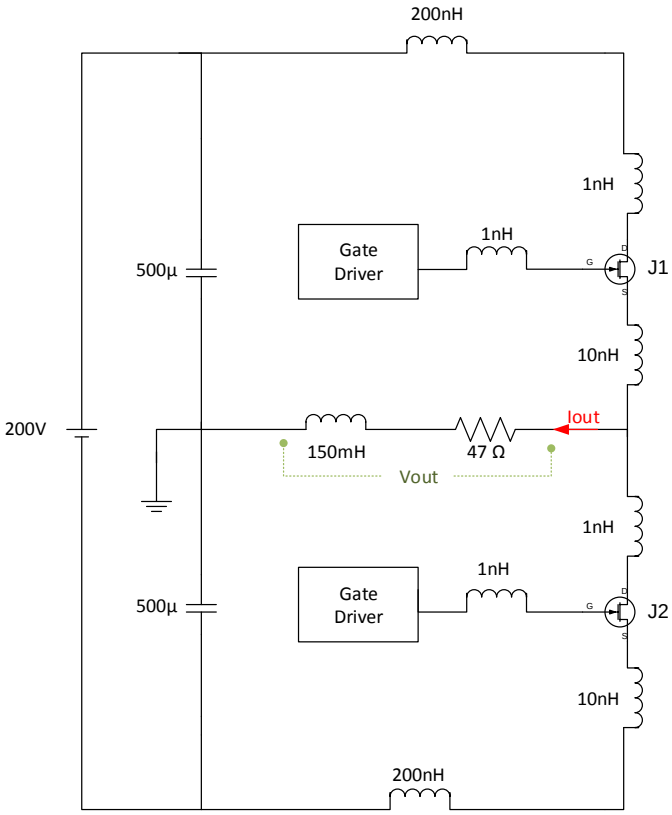

Figure 108. Phase-leg inverter used in Pspice simulations.

The oscillations initiated during the turn-off of J1 can be explained by an analysis of the current through the parasitic inductances and the voltage across J1 during the turn-off transient. When J1 starts to turn off, the voltage across J1 will increase while there is a current flowing through the stray inductance L. The associated stored magnetic energy in the stray inductance needs to be discharged. Since there are both inductive and capacitive elements in the circuit, a release of the stored magnetic energy will automatically initiate an oscillation. During this oscillation, the energy will be dissipated in the resistive elements in the circuit.

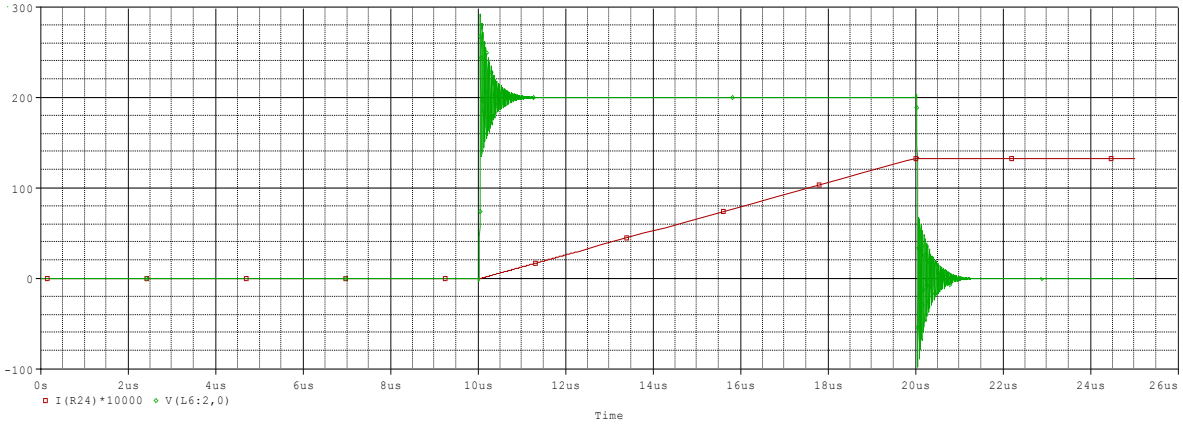

Figure 109. Typical voltage and current output waveform of a half-bridge inverter.

In the previous waveforms it is evident the problem of oscillations. We will try to improve them through our analysis in order to satisfy the peak voltage/current standards and dv/dt, di/dt we will set.

4.2 Adding boot resistance and gate-source clamp capacitor

As discussed the fundamental problem of parasitic ringing is caused by high speed switching of the devices which injects excess energy into the parasitics during the switching transient. The two primary sources of this excess energy are fast current transients (di/dt), and fast voltage transients (dv/dt). Slowing down the turn-on of the SiC JFET will help reduce both of these, but at the cost of more switching power loss.

Adding a small gate resistance between the driver and the gate of the FET is the simplest way to slow down the switching edges [Figure 1103]. A gate resistor will accomplish this, but will also slow down the turn-off transition resulting in unnecessary power loss. This can be circumvented by placing a resistor in the bootstrap path to slow down only the turn-on. By slowing down the turn-on and turn-off we damp the output voltage and current oscillations.

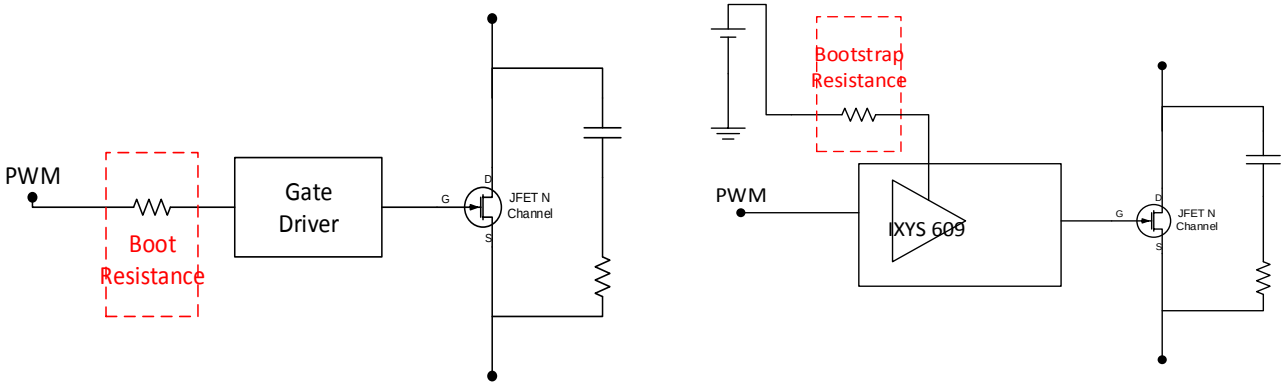

Figure 110. Boot and bootstrap resistor to improve switching transient. The latter case slows down only the turn-on speed.

Figure 1114 shows the effect of the boot resistance on the peak of the output voltage. Increasing the boot resistance decreases the peak of the ringing. However it is noted that there is a limit to the benefit that can be gained using this method.

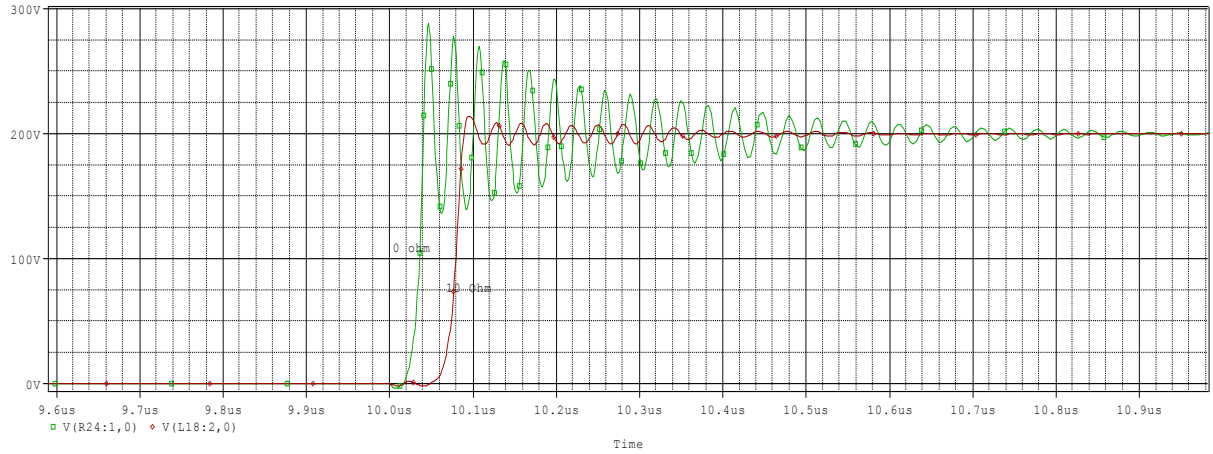

Figure 111. Effect of adding a boot resistor in output voltage. The green plot has 0 ohm gate resistor and the red one 10 ohm.

But this method also increases the switching losses and raises the temperature of the JFets. Thus the power loss was also measured. The trend [Figure 112] follows the expected trajectory of higher power loss for higher bootstrap resistance.

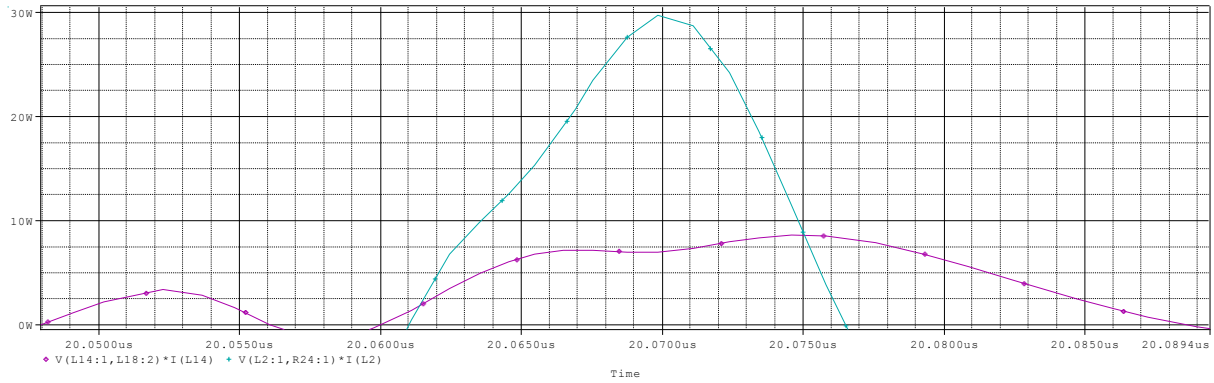

Figure 112. Peak power loss, the blue plot is with 10 ohm boot resistance and the purple with 0.

Consequently, for a given application, a balance must be found between peak ringing and the increased power loss.

Furthermore, a small capacitive clamp connected tightly across the gate-source terminals of each switch in a phase leg can help offset undesirable false trigging of the opposed switch due to the “Miller effect” when a bridge configuration is used.

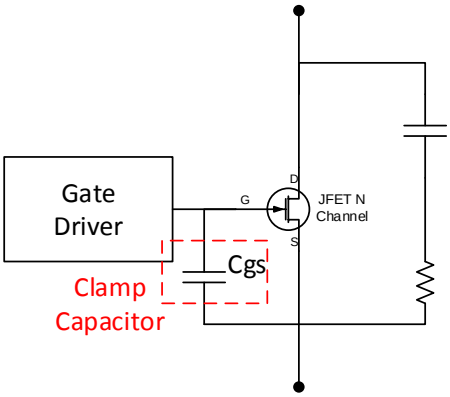

Figure 113. Gate-source capacitor

Finally, in Figure 114 the results from the use of such a capacitor are presented. The peak voltage is smaller but still the problem of the ringing is visible.

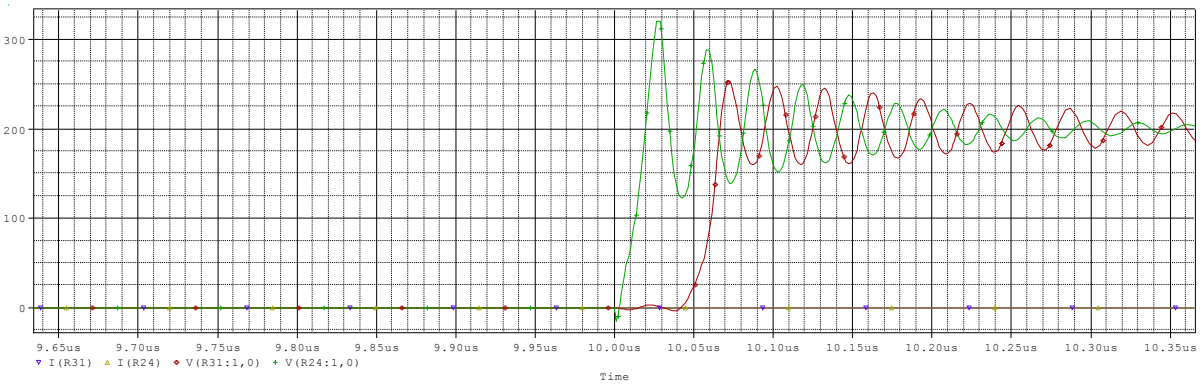

Figure 114. Output voltage after the use of a G-S capacitor.

4.3 Optimized placement of Power stage components

This method attempts to optimize the location of the components and improve the PCB designs to minimize the layout parasitic inductance. Special care must be then taken with the PCB layout design and placement of the Power Stage components in order to account for the high rate of change in voltage. Optimized PCB board layout is the preferred method for ringing reduction as it does not involve power loss and can actually improve efficiency since one is minimizing the parasitic loop inductance which is one of the root causes of the ringing.

Layouts should be designed to properly separate power grounds from signal ground with a common connection between the two made at a single point. Also the proper use of ground planes can help shield the gate from the drain as well as other high frequency circuit connections. Ferrite beads connected as close as possible to the gate terminal of the SiC JFET

may also be used to reduce voltage spikes at the gate. Lastly, gate drivers and gate turn-off components should always be connected as close as possible to the gate terminal of the device to reduce all of the aforementioned contributors of gate noise.

The externally applied PWM input must be sufficiently isolated from the output of the optocoupler and the isolated power supplies of the gate driver. Excessive ringing on the gate voltage waveform is either caused by parasitic inductance in the main power circuit and/or the gate circuit. The loop area of the power circuit and the physical distance between the gate driver output and the gate terminal should be minimized as much as possible.

Decoupling caps should be place as close as possible to the gate driver circuit as high peak currents are involved.

While this is undeniably the most effective method to decrease the ringing without negative effects on the system performance, in many cases such an optimum design is not easily achievable because of cost, and manufacturability constraints. Subsequent changes and optimizations of the layout may also be prohibitively expensive.

4.4 Separating Heat sinks

SiC power devices have presented many superior qualities that Si power devices are not able to handle, such as faster switching, higher blocking voltage and higher operating temperature. Because of the perfect match of their voltage blocking and current rating levels, no significant change is required to the power converters when replacing one type of device with the other but only the requirements on modifying the driving circuit. The enhanced SiC temperature operating ability and switching performance, allowing for the released thermal managements and increased power density through a size reduction of magnetic components and cooling substrates [12-13]. However, these advances are obtained at the cost of the increased high frequency (HF) EMI contents. Moreover, the influence of previously negligible circuit parasitics starts to play an increased role in EMI production.

The document [16] proposes to use separate heat sinks combined with dampening snubbers to improve the EMC performance for a SiC JFET based inverter for motor drives and these results are summarized again here.

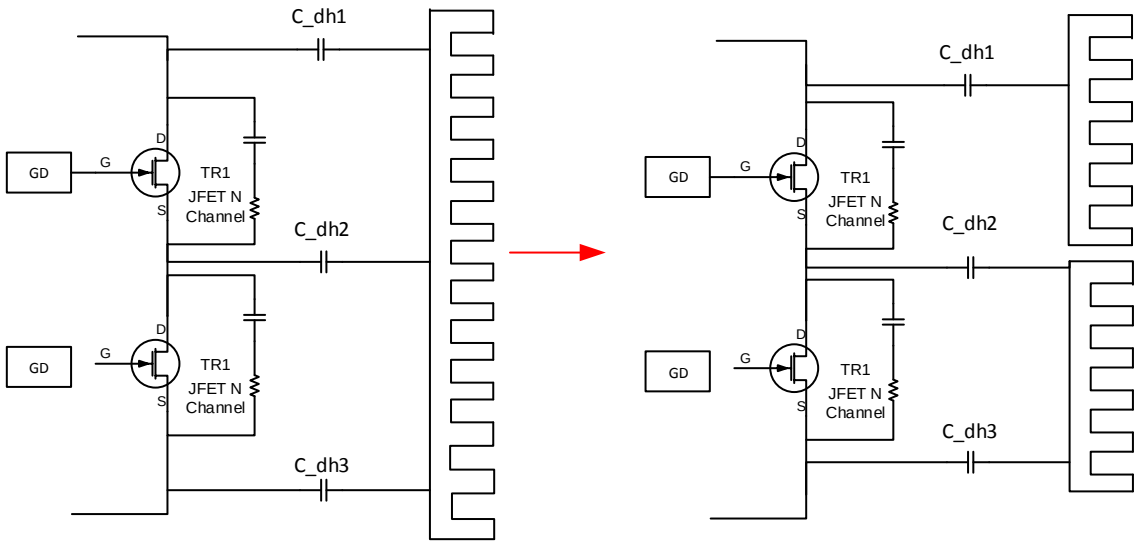

Figure 115. Heat sinks separation.

The use of one common heat sink creates the parasitic coupling capacitors (*Cdh1, Cdh2,* and *Cdh3*) which cause significant parasitic overshoots and oscillations and in return deteriorates the conducted EMC performance. To overcome this influence, the method of using separate heat sinks was proposed. The graphic interpretations are illustrated in Figure 115. Heat sinks separation.. It can be seen that the use of separating heat sinks has the decoupling effect by breaking the neutral point of the three capacitors in *Y* connection, which effectively decreases the equivalent capacitance in parallel to the switches. However, it must be mentioned that these capacitive couplings also have the effect of slowing down the switching transient and consequently decreasing the values of switching *dv/dts*. This could be a benefit from the EMC point of view.

Two inverter prototypes that implement discrete SiC JFETs with external SiC diodes on top of one common heat sink and separate heat sinks were built and investigated. It was shown that the use of separate heat sinks significantly reduce the EMI magnitudes and the oscillations.

4.5 Blanking times

In the document [14] and [0] instead of using a positive blanking time, a negative blanking time was used. This means that J1 [Figure 108] will be turned-on a short time before J2 is turned off. The reason for this negative blanking time is to increase the current through L and J1 and to decrease the negative current through J1 by a short circuit. This means that J1 will have a hard turn-on but the turn-off for J2 will be soft

According to the results in [14,0], a blanking time between turn-off of J1 and turn-on of J2 of -150ns would give low oscillations. The difference is that J2 is turned on before J1 has been completely turned off. This means that the upper JFET will change working point during the transition in the saturation region during the turn-off, delaying the current turn-off. This means that the current through the stray inductance is nearly zero when the voltage across

J2 reaches the dc-link voltage, E. The consequences of using this method is that the oscillations are reduced and that the switching losses increase significantly.

The choice of the blanking times are dependent on the circuit parameters. However, it can be concluded that a short blanking time at turn-off and a short negative blanking time at turn-on is a good choice in a majority of different cases although the power losses are increasing a lot.

4.6 Snubbers

The need to use auxiliary circuits or techniques to reduce switch stress and losses has been shown in the beginning. On this section we will use a circuit which is often called snubber and can handle and improve the repetitive switching behaviour of a semiconductor.

4.6.1 Why use snubbers?

Snubbers are frequently used in electrical systems with an inductive load where the sudden interruption of current flow leads to a sharp rise in voltage across the current switching device, in accordance with Faraday's law. So, if the voltage generated across the device is beyond what the device is intended to tolerate, it may damage or destroy it. Additionally, we outline some of the reasons that switching devices and circuit components may fail

- *Overheating – usually due to excessive switching losses*
- *Overcurrent*
- *Overvoltage*
- *Excessive di/dt, dv/dt*

To solve these problems we place heat sinks and fuses at suitable locations. But in order to confront the excessive slopes in the voltage and the current we have to use snubbers across the semiconductors.

For electrical circuit snubbers, one definition might be: “A snubber is a network that alters the voltage and/or current waveforms of a switch during turn-on and turn-off.” In fact, snubbers are a means to switch a device more "softly".

SiC power devices have presented many superior qualities that Si power devices are not able to handle. However, these advances are obtained at the cost of the increased high frequency oscillations and ringing problems. With the faster SiC switching dv/dts and di/dts, the parasitic oscillations and overshoots become much more extensive and evident, which significantly depredates the system reliability and in return deteriorates the conducted/radiated EMC performance. Furthermore, the HF parasitic oscillations combined with the faster *dv/dts* cause great potential of the shoot-through problems and fault operations for power systems.

Inductive elements are often unintentional, but arise from the current loops implied by physical circuitry. The board parasitics must be taken into account during the analysis of oscillations. The power JFETs themselves contain multiple parasitic. The intrinsic and parasitic elements (inductance and capacitance) of the JFET contribute to high frequency ringing during the switching transients. Figure 116 shows a simplified model of the Vertical Trench SiC Jfet by Semisouth and its parasitic components. Inductors L_G, L_S, L_D represent the parasitic inductances of the device.

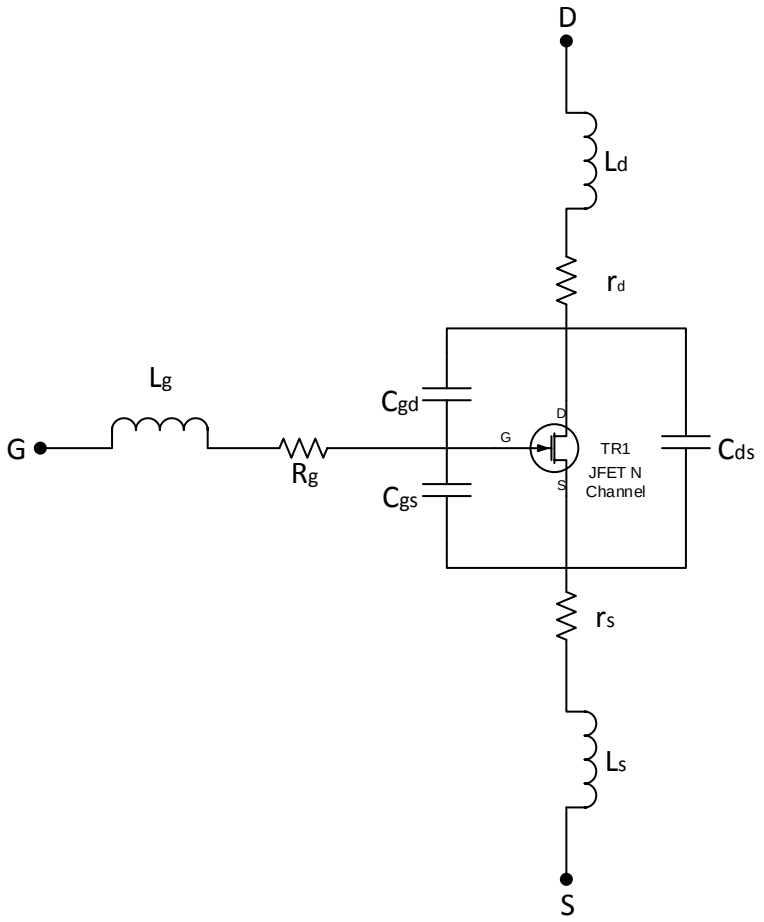

Figure 116. Model of the SiC VT Jfet by Semisouth where we can see all the parasitic inductances and capacitances.

So the goal of the snubber is to provide a short-term alternative current path around the current switching device so that the inductive element may be discharged more safely and quietly. When the switch turns off, the switch current is commutated to the capacitor but the voltage across the capacitor is very small because the switch has discharged it and only rises slowly as the integral of the current. The result is to allow the switch contacts to open with a very low voltage across them, minimizing the primary arc.

No matter how useful or interesting snubber circuits may be their advantages are not coming for free but they still require design compromises between:

- *cost*
- *complexity*
- *reliability*
- *loss*
- *circuit performance*

Finally, we present a list of typical applications of the snubbers.

- *peak voltage limiting*
- *peak current limiting*

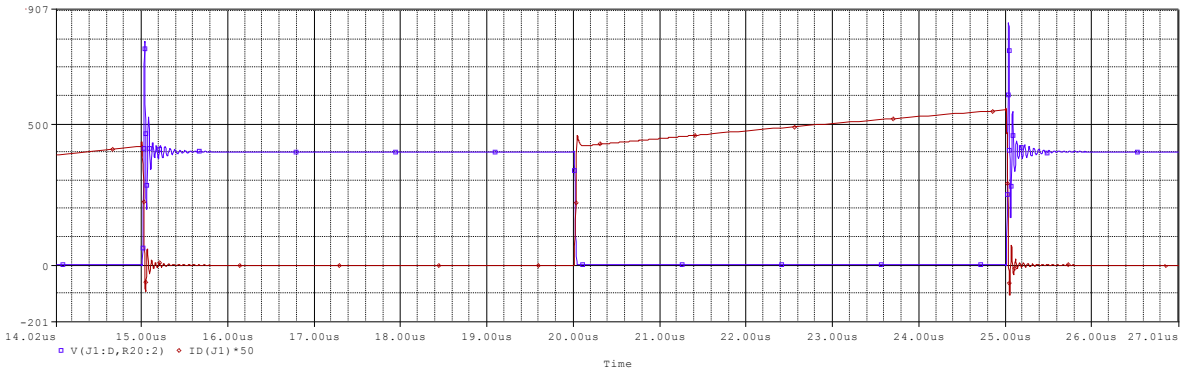

Figure 117. The problem of the peak voltage (during turn on), peak current (during turn-off)

- $\frac{dV}{dt}$ *limiting*
- $\frac{dI}{dt}$ *limiting*

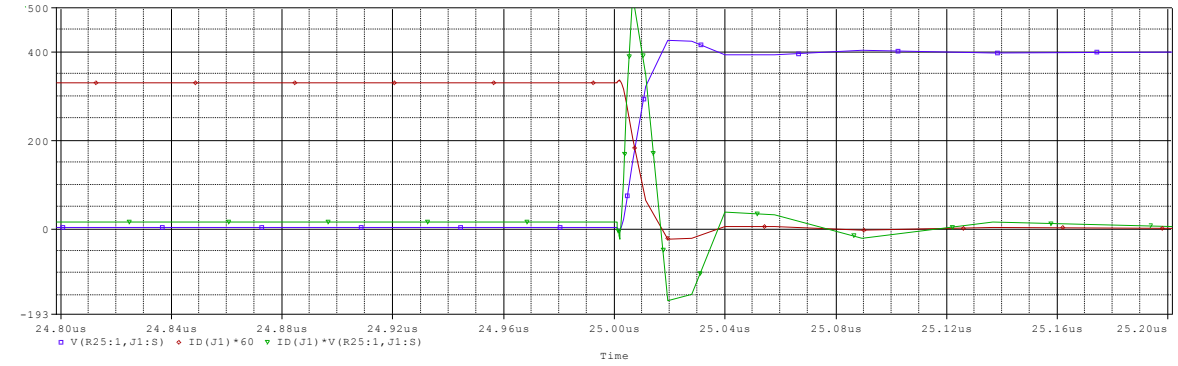

Figure 118. The problem of high dv/dt , di/dt and the high switching loss(green)

- *load-line shaping to stay within the safe operating are (SOA) boundaries*

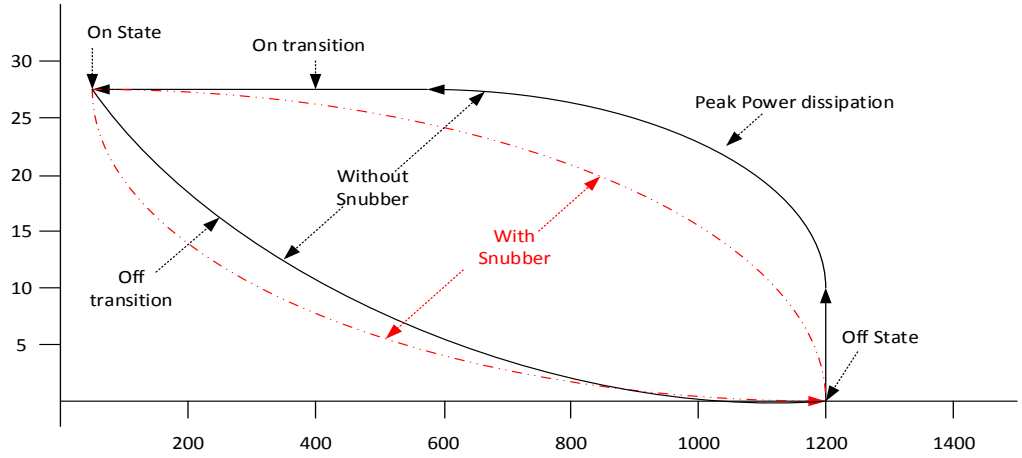

Figure 119.With snubber the power losses are less

- *improve circuit reliability through reduced electrical and/or thermal stress.*
- *switching loss reduction*
- *transfer of switching loss from the switch to a resistor or a useful load*
- *EMI reduction*
- *voltage sharing in series devices*
- *current sharing in parallel devices*
- *increasing the power obtainable from a given device or devices in a given application*
- *extension of switch service life*

4.6.2 Types of Snubbers

We classify the snubbers and so we introduce some categories of them:

- *Passive*

Snubbers made up of linear network elements, i.e. resistors, capacitors and/or inductors.

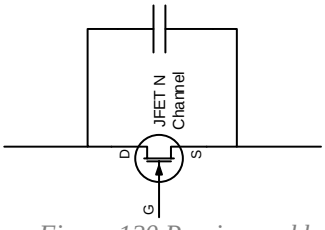

Figure 120.Passive snubber

- *Active-lossy*

  These are networks which use non-linear or active devices such as diodes or switches in addition to resistors, inductors and/or capacitors. This class of network dissipates a majority of the switching loss but usually in a resistor rather than in the switching device.

- *Active-low loss*

  In this type of snubber circuit the energy which would normally be lost in the snubber resistor(s) is delivered either to the input source or to some useful load.

- *Non-polarized*

  These are networks which have no preferred polarization, i.e. they can be installed in the circuit without regard to polarity. An example would be a simple series R-C damping network.

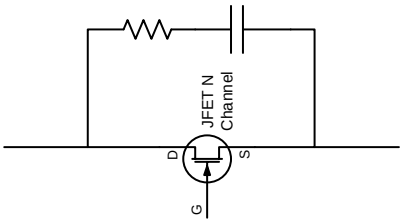

Figure 121. Non Polarized

- *Polarized*

  Most snubber networks using active devices can be installed in the circuit with only a given polarity. At least in principle, almost any polarized snubber network can be made non-polarized by imbedding it in a diode bridge. But in general most active snubbers have a defined polarity.

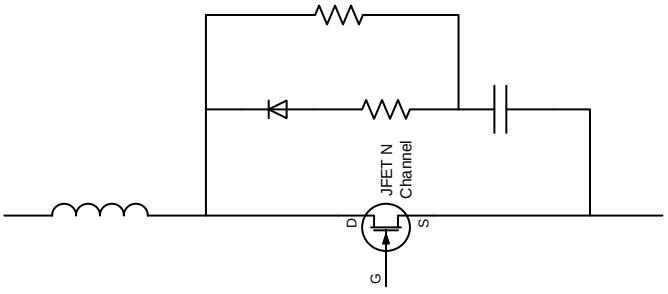

Figure 122.Polarized

- *Soft switching*

Conceptually, "Soft switching" is enabling the switch to turn on and/or off with either very low voltage across the switch or very low current through the switch. This can result in very low switching loss and stress. Many snubber circuits do provide varying degrees of soft switching but this term is usually reserved for circuits which use either resonant topologies or some form of resonant transition switching to control switch stress.

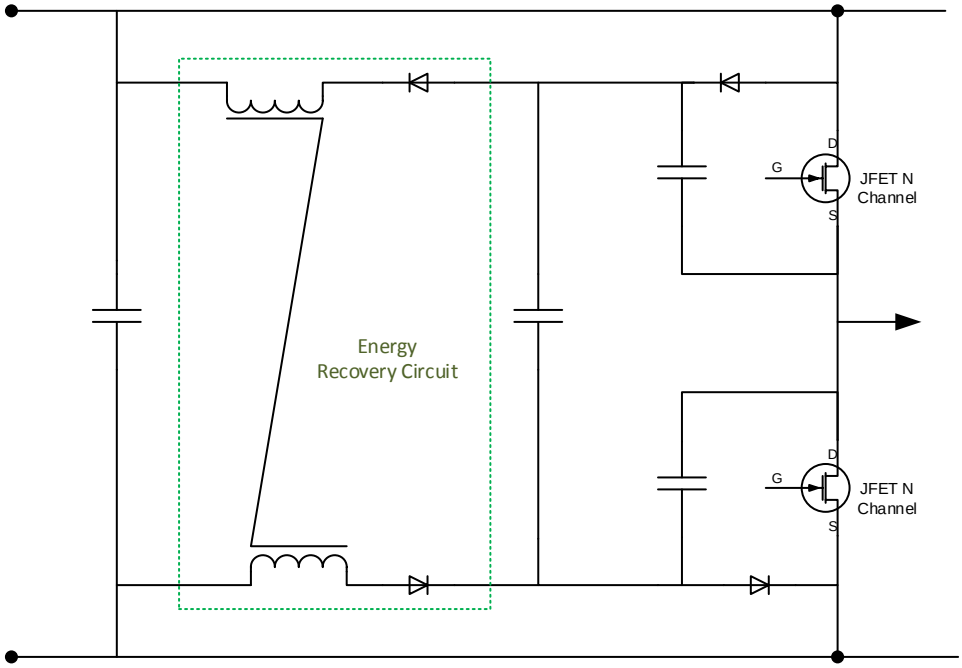

Figure 123.Soft-Switching snubber

4.6.3 Design of Snubber circuit

Firstly we have to understand the waveforms which we try to improve by using snubber circuits. There are many different types of circuits in power converters, motor drives and other devices but all of them have a common network and waveforms associated with the switches. Most power electronics circuits have within them the same switch-diode-inductor network (shown in the dotted lines).

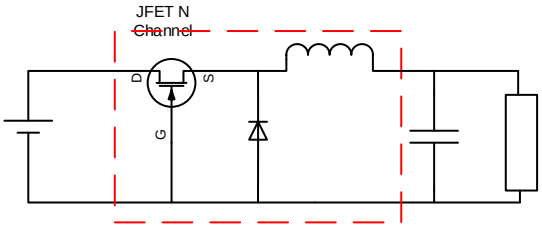

Figure 124. Buck dc-dc converter

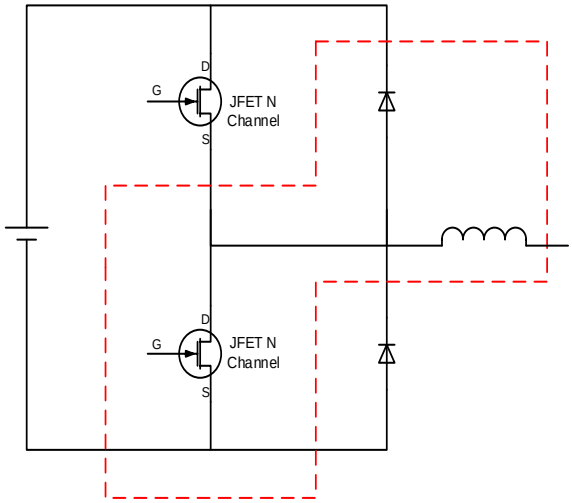

Figure 125.Inverter leg

The behavior of this network is the same in all the circuits which means that we only have to solve the snubber design problem for one circuit and apply it to all the others. This simplifies the problem and allows generalized snubber design techniques.

In the next paragraphs the various snubbers will be tested in inverter leg topology but as we have mentioned the same results may be applied in other power electronics converters. First the theoretical results for the values of resistors and capacitors in the snubbers are presented and then they are evaluated in the Pspice.

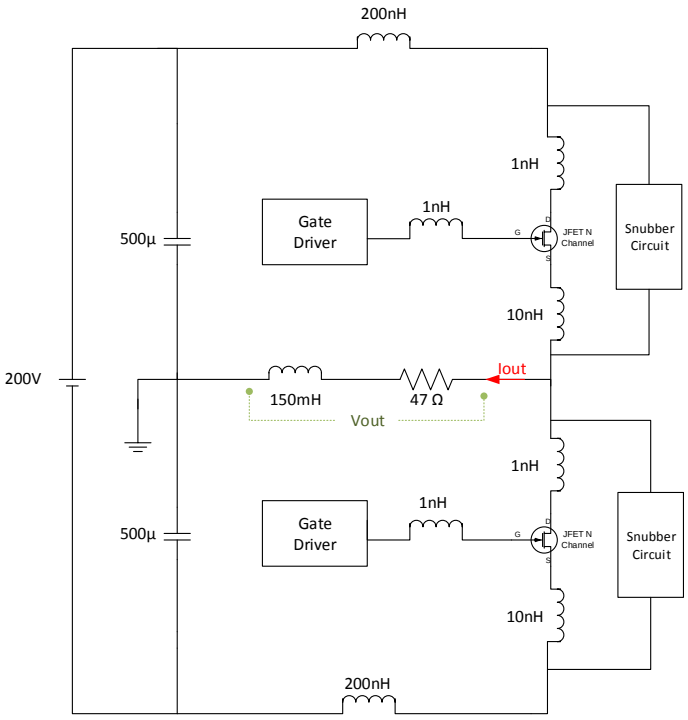

Figure 126.Inverter leg

4.6.4 R-C snubber (Passive Snubber)

The R-C snubber is by far the most commonly used snubber. Although it seems to be a simple circuit, the analytical selection of the values for the resistor and the capacitor turns out to be complex enough. So we have to make some compromises between the peak voltages, what currents are acceptable and the switching losses.

Our approach in this paragraph is adopted by the classic paper by McMurray [3] whose figures are used to extract some useful results for our R-C snubber. After we have made our choices, they will be evaluated by the Pspice simulation program in order to confirm them.

For the theoretical analysis we consider the circuit in *Figure 127*. A voltage *E*, which can be assumed steady throughout the transient, is applied to a series *RCL* circuit. The voltage *e* across the snubber resistance and capacitance series appears as recovery voltage on the semiconductor device. Time zero of the transient is the instant when the device blocks. The initial value of *e* is *IR* and the rate *di/dt* is equal to *E/L*.

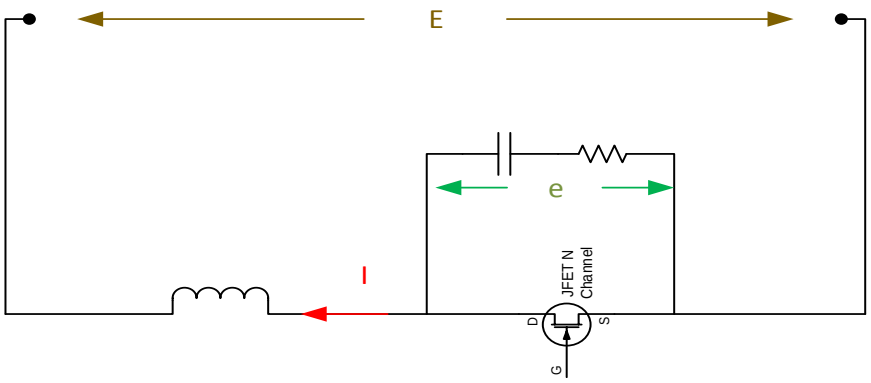

Figure 127. Passive snubber analysis.

The general Laplace transforms for the current *i* and the voltage *e* are

$$i(s) = \frac{\frac{E}{L} + sI}{s^2 + \frac{R}{L}s + \frac{1}{LC}} \quad (1)$$

$$e(s) = -\frac{s(E - RI) - \frac{I}{C}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} + \frac{E}{s} \quad (2)$$

The following parameters are introduced

$$Undamped\ natural\ frequency\ \left(\frac{rad}{s}\right): \omega_0 = \frac{1}{\sqrt{LC}} \quad (3)$$

$$Decrement\ factor: \quad a = \frac{R}{2L} \quad (4)$$

$$Damping\ factor: \zeta = \frac{R}{2\sqrt{\frac{L}{C}}} = \frac{a}{\omega_0} \quad (5)$$

The inverse transform of (2) yields

$$e = E - (E - RI)\left(cos\omega t - \frac{a}{\omega}sin\omega t\right)e^{-at} + \frac{I}{C\omega}sin\omega t e^{-at} \quad (6)$$

And by differentiating (6)

$$\frac{de}{dt} = (E - RI)\left(2a\, cos\omega t + \frac{\omega^2 - a^2}{\omega} sin\omega t\right)e^{-at} + \frac{I}{C}\left(cos\omega t - \frac{a}{\omega} sin\omega t\right)e^{-at} \quad (7)$$

The initial voltage and slope are obtained by setting t=0 in (6) and (7)

$$\left(\frac{e}{E}\right)_o = \frac{RI}{E} = 2\zeta\chi \qquad (8)$$

$$\left(\frac{de}{dt}\right)_o = (E - RI)2a + \frac{I}{C} = E\omega_0(2\zeta - 4\zeta^2\chi + \chi) \quad (9)$$

On this point we may distinguish three different cases:

I. Underdamped Condition ζ <1
II. Overdamped Condition ζ >1
III. Critically Damped Condition ζ =1

For each case we get a solution of the following form:

- $t_1 = f(\zeta,\chi)$ (10), where t_1 is the time where the voltage rises at a peak
- $\frac{E_1}{E} = p(\zeta,\chi)$ (11), where E_1 is the peak voltage

So the voltage ratio $\left(\frac{E_1}{E}\right)$ as a function of χ and ζ are depicted in the plot of the figure 14. Thus if $\left(\frac{E_1}{E}\right)_0$ is the allowable voltage ratio, the optimum snubber design may be obtained from the figure 14 and the following equations.

$$\chi = function\ of\left(\frac{E_1}{E}\right)_0 \quad (12)$$

$$\zeta = function\ of\left(\frac{E_1}{E}\right)_0 \quad (13)$$

$$C = L\left(\frac{I}{E\chi_0}\right)^2, where\ 2 \times C_{oss} < C < 10 \times C_{oss} \quad (14)$$

(C_{oss} the device capacitance from the manufacturers data sheet shown in 1,2)

$$R = 2\zeta_0\sqrt{\frac{L}{C}} = \frac{2\zeta_0 E\chi_0}{I} \quad (15)$$

In most applications (like ours), the peak recovery voltage and *dv/dt* are both important and a damping factor selected to compromise between minimum voltage spike and minimum *dv/dt* is recommended. The set of parameters for that amount of damping which will minimize the product of E_1 and *dv/dt* for a given capacitance (the inductance L equals to 200nH - 400nH and the current I=200/47=4.2A) are presented in **Error! Reference source not found.**3. We define as χ_0 and ζ_0 the optimum values of χ and ζ for minimum voltage spike and *dv/dt.* The design procedure is as follows.

- Select a tolerable peak voltage $E_1 = 280V$ and calculate $\left(\frac{E_1}{E}\right)_0 = 1{,}4$

- From figure 14, read the corresponding values of $\chi_0 = 0{,}6$, ζ_0= 0,3

- Calculate the capacitance and the resistance

$$0.5\text{nF} < C < 10nF \quad (16)$$
$$30\Omega < R < 80\Omega \quad (17)$$

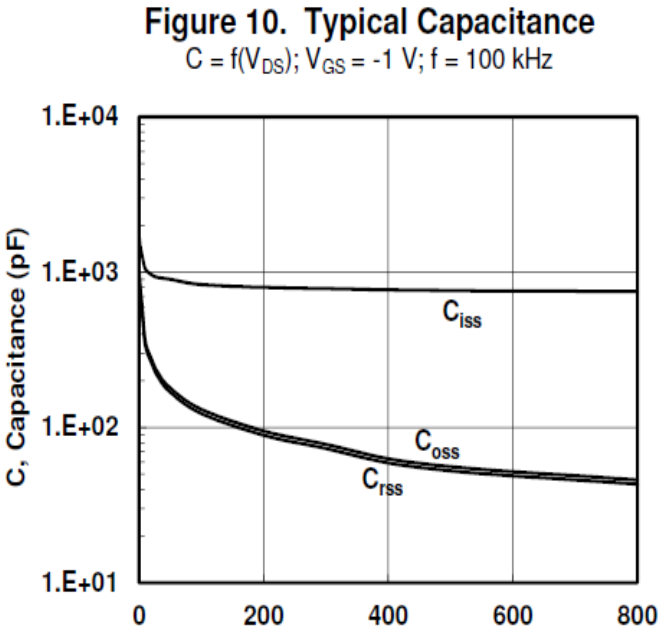

Figure 128 Typical Capacitance for SJEP120R100

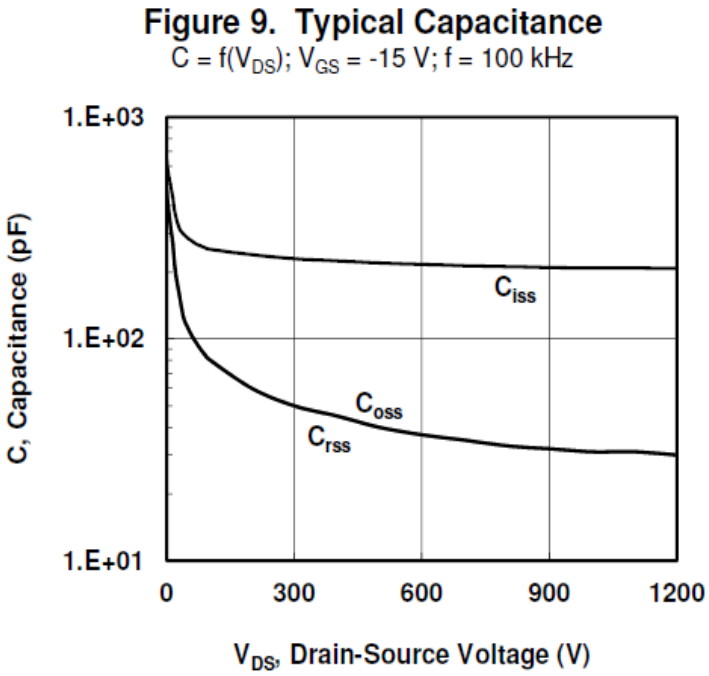

Figure 129. Typical capacitance for SJDP120R085

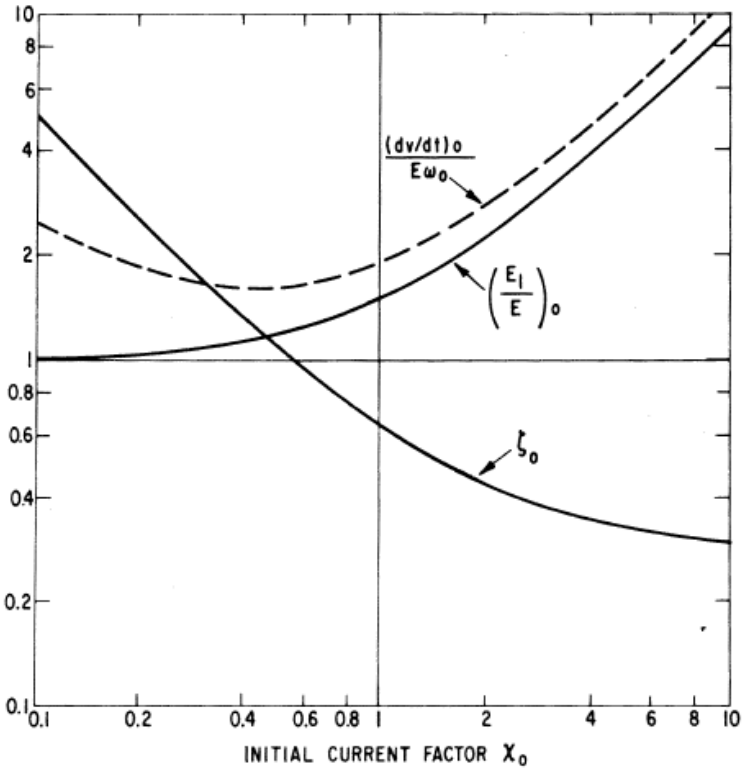

Figure 130. Optimum snubber parameters for compromise design

It is seen that for a given rate $\left(\frac{E_1}{E}\right)$ there is a particular choice of damping ζ_0 and current factor χ_0 which minimize the $\frac{(dv/dt)_0}{E\omega_0}$ and consequently the dv/dt fulfilling both our standards (voltage spike and slope).

Another effect of adding a snubber is that it introduces loss. It may be that some other losses will be reduced but this loss is still a matter of concern. The larger we make C_s the greater will be the beneficial effect of the snubber but also the greater will be the loss introduced by the snubber.

Typically we try to choose a value for C_s which is the minimum that gets the job done, although sometimes it is desirable to reduce the switch loss at the price of increased loss in R_s. The lower the value for R_s, the higher the peak pulse current will be. Because varying the value of R_s away from the optimum value, changes V_p only slowly, it is a normal practice to make R_s somewhat larger than optimum to limit the peak current.

Cs is discharged through Rs at switch turn-on. When C_s is recharged, energy will again be dissipated in R_s. As a result, the energy loss per switching cycle will be:

$$U_1 = C_s V^2/2 \xrightarrow{Cs=1nF} U_1 = 20\ \mu J \quad (18)$$

The power dissipation in R_s will depend on the switching frequency (f_s):

$$P_{Rs} = C_s V^2 f_s \xrightarrow{Cs=1nF, f=5kHz} P_{Rs} = 0.2\ W \quad (19)$$

After the last comments we conclude to the following values for the RC snubber

$$0.5\text{nF} < C < 10nF \rightarrow \boldsymbol{C = 1nF} \quad (20$$
$$30\Omega < R < 80\Omega \rightarrow \boldsymbol{R = 70\Omega} \quad (21)$$

Thereafter we use the Pspice for a further confirmation of our results. We analyze for different values of capacitors and resistors. After we have chosen a capacitor we proceed with the resistor simulations. We only present the voltage plots because the current for our application is small and it doesn't face significant ringing problems.

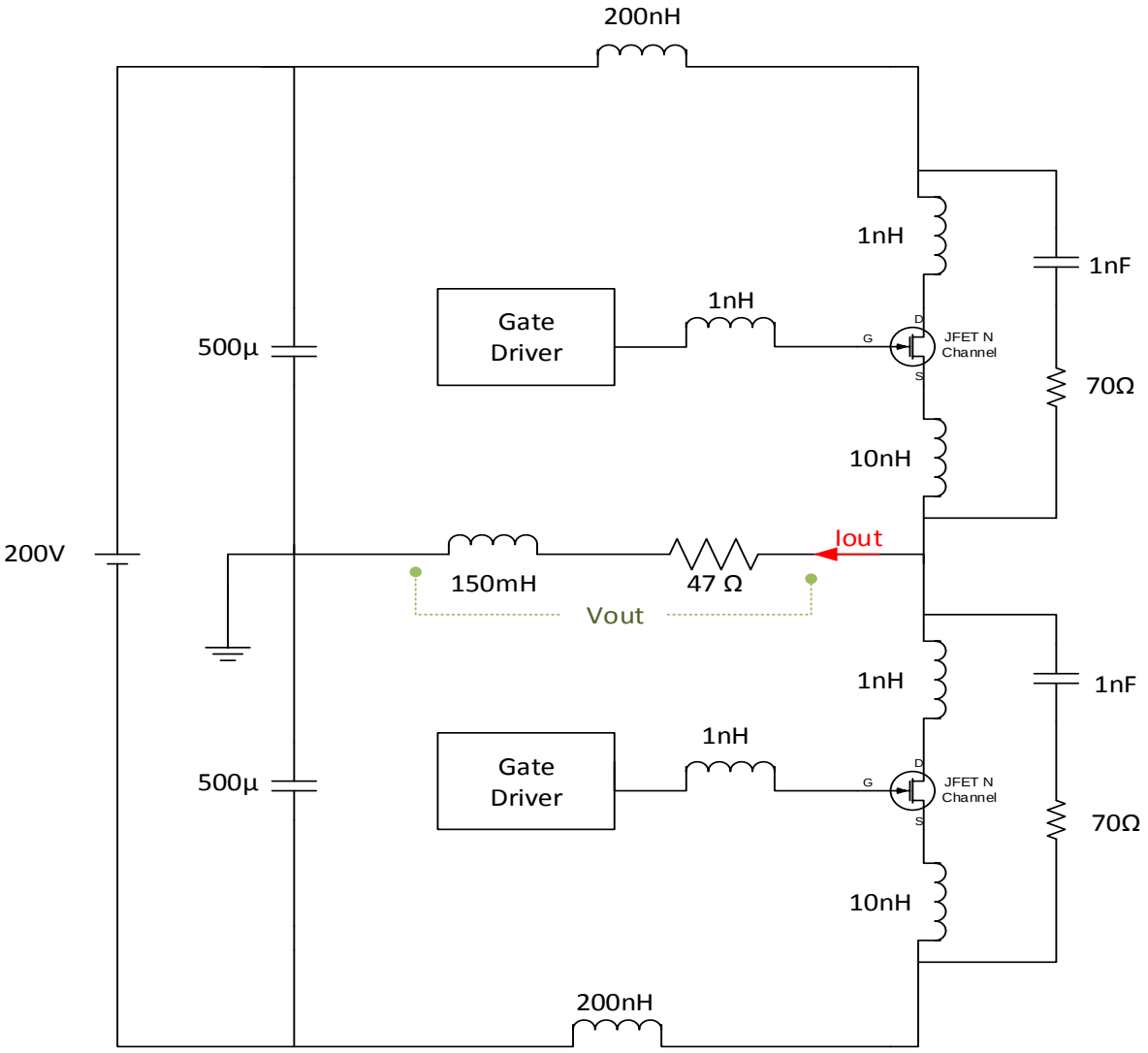

Figure 131. Inverter leg with RC snubber

We begin with the selection of the capacitor. We simulate for Cs=0.5nF, 1nF, 5nF, 10nF, 30nF. As we can see (*Figure 132*, *Figure 133*) for values larger than 5nF the differences between them are very small whereas the larger the capacitor is, it follows that the power dissipation and the current peak are larger. So a compromise between them is Cs=1nF as it was predicted through the theory before. In general we choose a value for C_s which is the minimum that gets the job done.

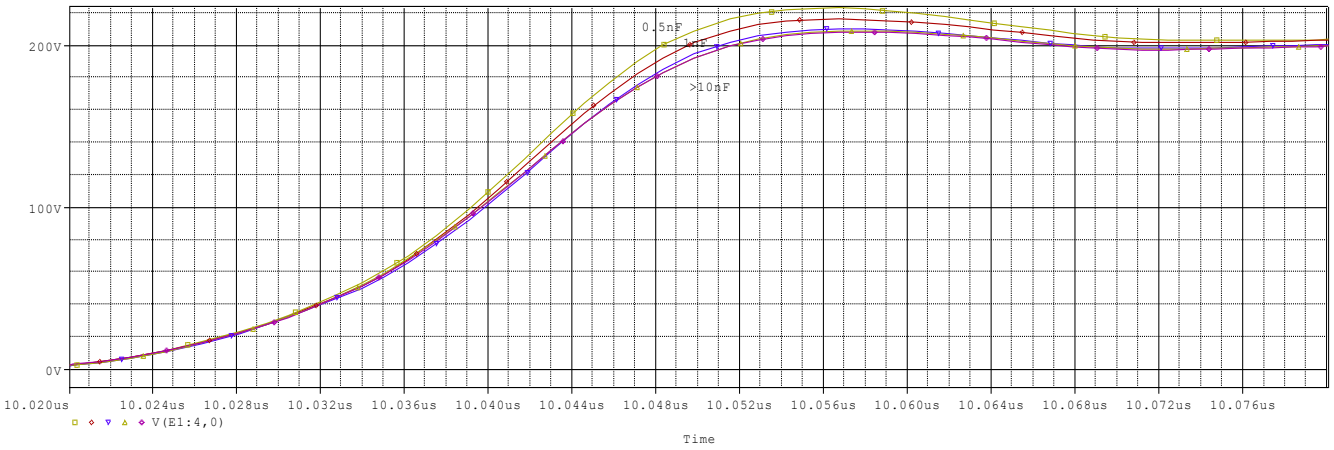

Figure 132.Spice simulation for different values of Cs(yellow=0.5nF,red=1nF and the rest are >5nF). Voltage plot during turn-on

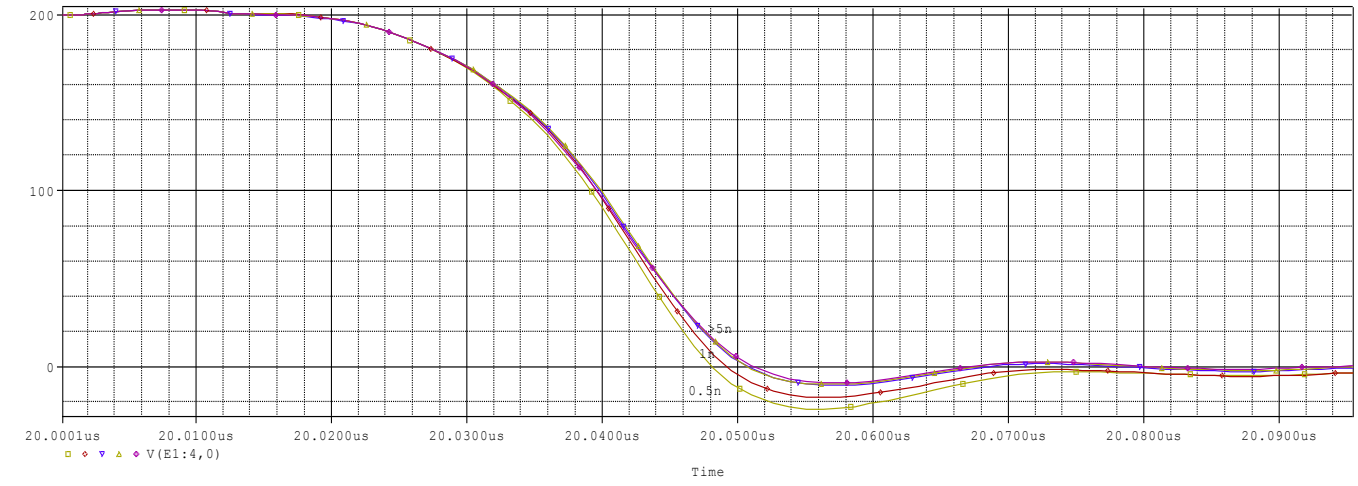

Figure 133.Spice simulation for different values of Cs(yellow=0.5nF,red=1nF and the rest are >5nF). Voltage plot during turn-off

As far as the resistor is concerned, it must be carefully chosen as it effects the peak voltage and the voltage oscillation time. We decide to select a relatively large value (R_S=70) in order to limit the peak current and the duration of the oscillations. The trade-off for this choice is the larger power dissipation we are going to have on the resistor.

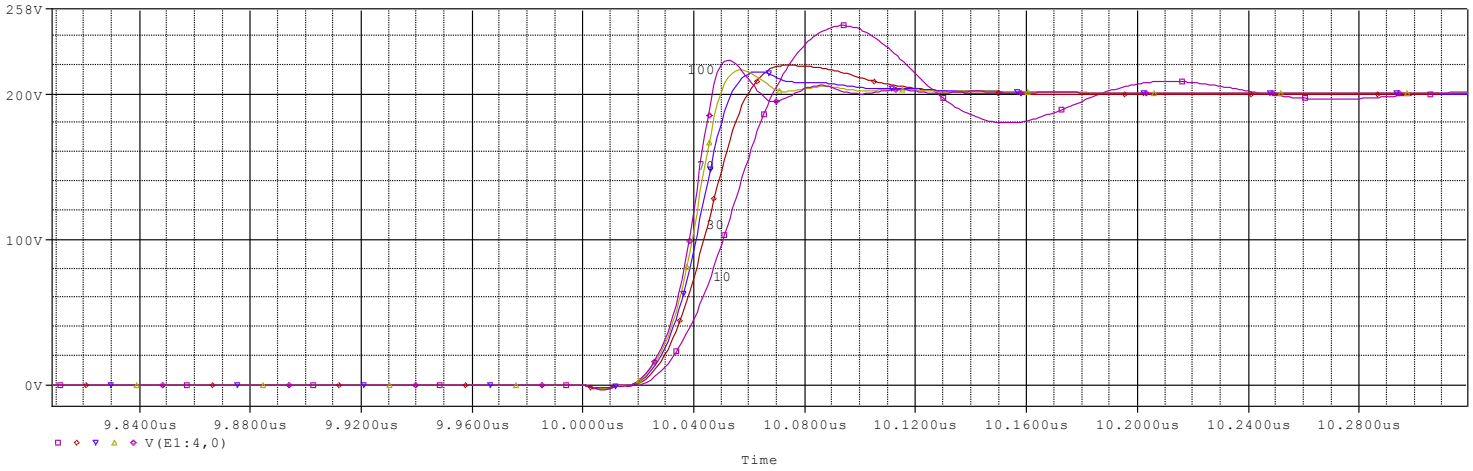

Figure 134.Spice simulation for different values of Rs (purple=10Ω,red=30,blue=50,yellow=70,light purple=100).Voltage plot during turn-on

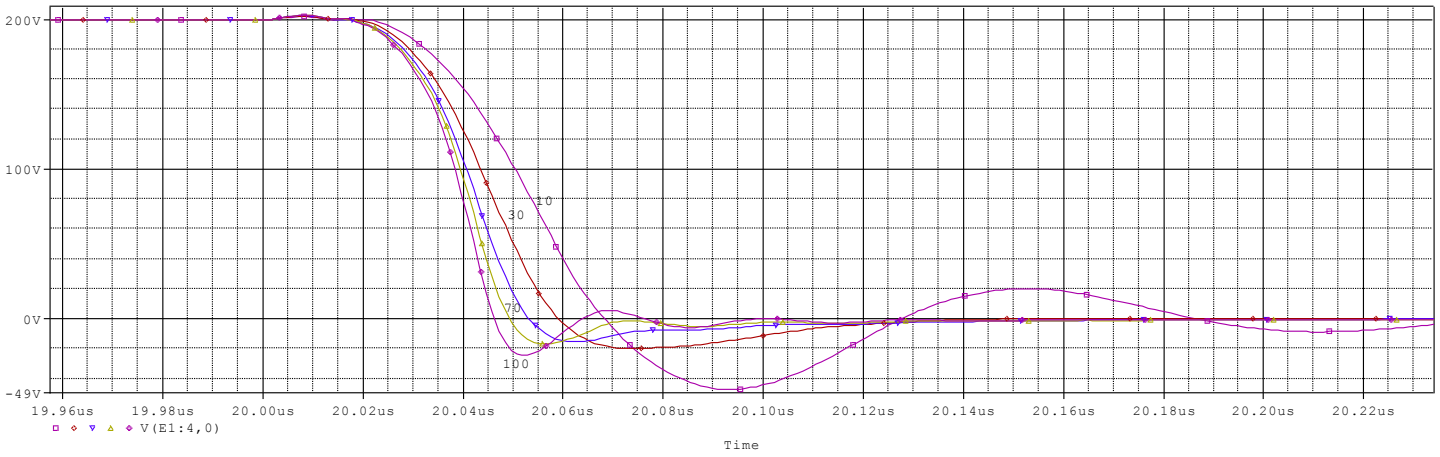

Figure 135.Spice simulation for different values of Rs (purple=10Ω,red=30,yellow=70,blue=50,light purple=100).Voltage plot during turn-off

The damping factor is important for the oscillation time during turn-on and off. When we don't use snubber the switching times are smaller but the losses due to the peak voltage and the high dv/dt are huge.

Cs=1nF	Turn-on	Turn-off	Damping factor	Peak Voltage	Oscillation time turn-on
Rs=10Ω	110nsec	90nsec	1.25	250V	300nsec
Rs=30Ω	90nsec	88nsec	1.1	220V	130nsec
Rs=50Ω	85nsec	80nsec	1.07	214V	85nsec
Rs=70Ω	**75nsec**	**70nsec**	**1.075**	**215V**	**87nsec**
Rs=100Ω	60nsec	55nsec	1.11	222V	100nsec
No Snubber	40nsec	38nsec	1.5	300V	1μsec

4.6.5 Turn-off Snubber (Active Snubber)

Passive RC-snubbers can be very effective in reducing peak voltages and damping ringing waveforms. Sometimes however, more is needed. For example, we may wish to reduce the peak stresses and to stay within SOA boundaries.

After the RC-snubber, RLC-diode family of snubbers are the most commonly used. The turn-off snubber offers a smoother turn-off for the semiconductor so that the peak power dissipation will be smaller.

This snubber operates on the same principles as the RC snubber, but only during turn-off switching. As the semiconductor turns off, energy trapped in the loop inductance is transferred to the capacitor. The diode blocks oscillations and the excess charge on the capacitor is dissipated through the external resistor.

below we present the circuit we simulate and the output voltage waveform.

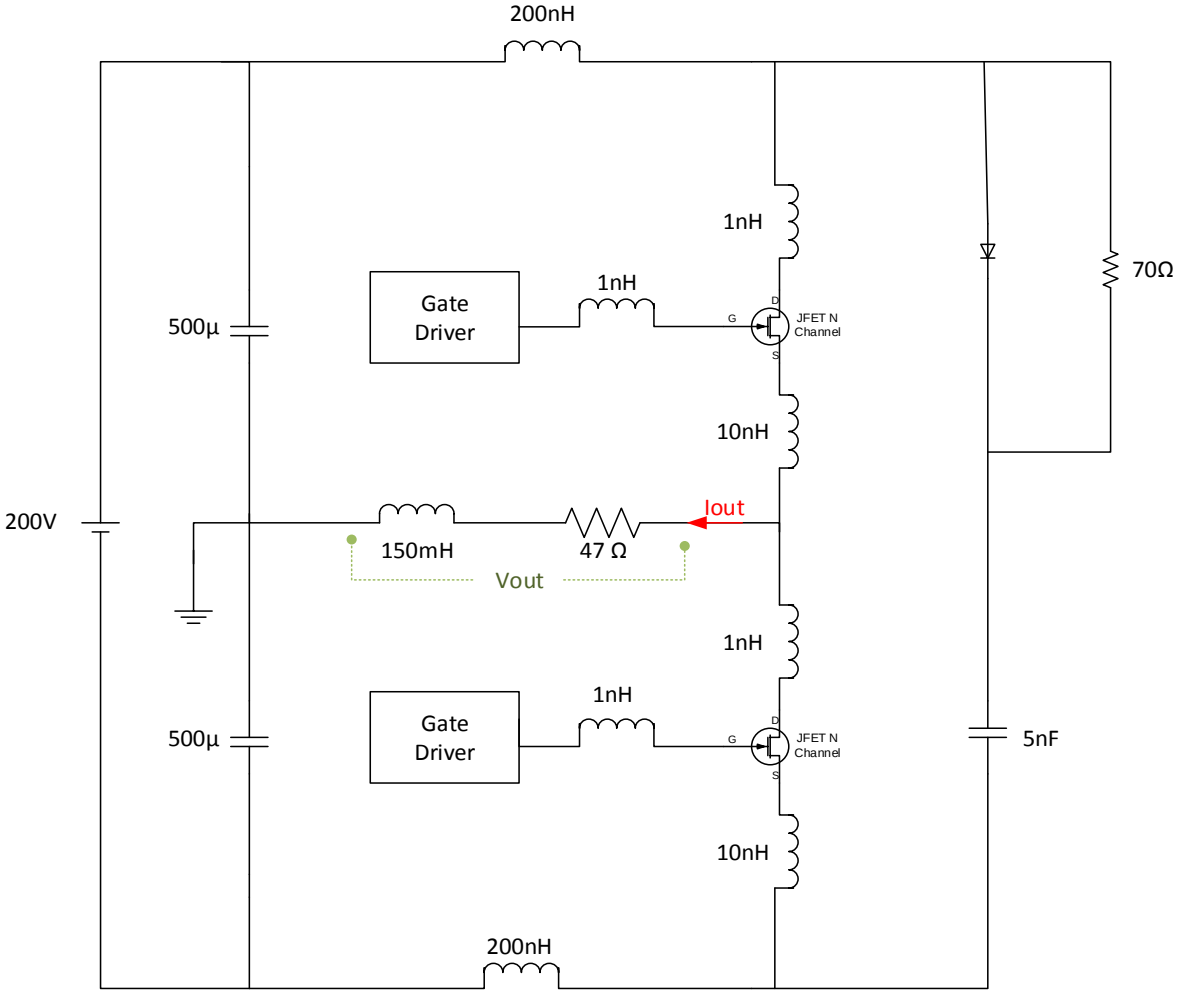

Figure 136.Turn-off snubber

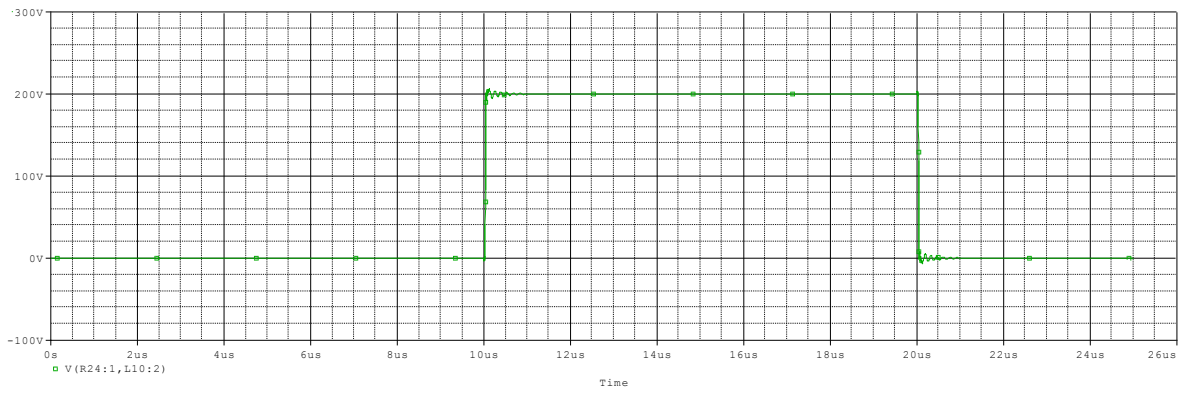

Figure 137.Voltage plot for the turn-off snubber

From the following table it is seen that the results are better comparing to the no-snubber case. But still the duration of the oscillations is a serious issue as it contributes to the deterioration of the quality of the power converter.

	Turn-on	Turn-off	Damping factor	Peak Voltage	Oscillation time turn-on
Active snubber, Cs=5nF, Rs=70Ω	80nsec	70nsec	1.05	210V	500nsec
Passive snubber, Cs=1nF, Rs=70Ω	**75nsec**	**70nsec**	**1.075**	**215V**	**87nsec**
No Snubber	40nsec	38nsec	1.5	300V	1μsec

RCD snubbers are typically used in medium to high current applications. A RLC turn-off snubber as shown in *Figure 136* can be used to prevent voltage spikes and voltage oscillations across a SiC JFET during device turn-off. But the large peak current handling capability of the SiC Jfet (comparing to our application needs~5A) and the fact that its switching speed can be easily controlled by the gate voltage eliminates the need for a turn-off snubber in this case.

4.6.6 Soft-switching snubbers

The snubber from Figure 132 has been proposed by [2]. The Passive Soft-Switching Snubber (PSSS) provides a viable alternative to the existing soft-switching inverters. The PSSS is especially suited for SiC device inverters. It is employing only passive components, reducing dv/dt, di/dt , eliminating dc bus plane layout. But the use of the transformers usually introduce leakage inductance which can be substantial. Moreover when the cost is important, we have to take into account that they are significantly more expensive than the classic RC or RCD snubber. The use of magnetic components may result in saturation problems when we go for high frequencies in the Sinusoidal PWM which is our case.

4.7 Conclusions

The comparison which has been made between some of the basic snubbers has concluded the use of a classic RC snubber for the 1-phase SiC Jfet inverter. All simulations has been made for the VT Normally-on SiC Jfet SJDP120R085 but the same results could apply in the normally-off Jfet with the appropriate change on the capacitor (Cs) value.

Apart from the use of snubbers, we have also reviewed some fundamental approaches to reduce the ringing phenomenon in the switching loop. In Figure 138, a comparison is done in which the passive snubber exhibits again very good behavior.

In the final chapter we tried to adopt all the above techniques. So we use the classic RC snubber with the resulted values, a gate-source capacitor for the Miller effect, optimized PCB boards for the gate drivers and the inverter and separated heat sinks. The blanking times are chosen positive as it was considered a better option in order to avoid short-circuit and shoot-through conditions.

	Turn-on	Turn-off	Damping factor	Peak Voltage	Oscillation time turn-on
Active snubber, Cs=5nF, Rs=70Ω	80nsec	70nsec	1.05	210V	500nsec
Passive snubber, Cs=1nF, Rs=70Ω	**75nsec**	**70nsec**	**1.075**	**215V**	**87nsec**
No Snubber	40nsec	38nsec	1.5	300V	1μsec
Boot resistor	100nsec	90nsec	1.4	280V	600nsec
Boot resistor+ Gate-source capacitor	110nsec	95nsec	1.175	235V	400nsec

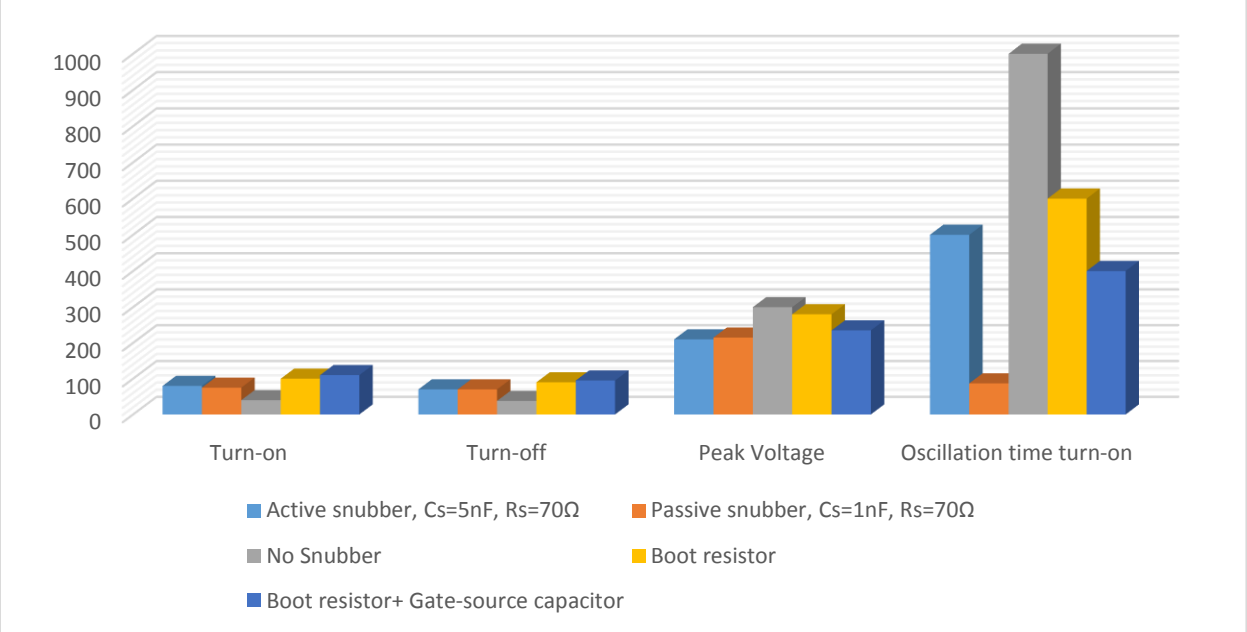

Figure 138. Comparison between the basic methods of minimizing oscillations

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Chapter 5

CONSTRUCTION AND EVALUATION OF A DIODE-LESS SiC SINGLE-PHASE INVERTER

On this final chapter we proceed with the construction of an inverter exploiting only SiC semiconductors (*DM-mode VT SiC JFET* SJDP120R085). Our scope is the investigation and the comparison of efficiency of a SiC inverter circuit with and without antiparallel diodes in order to evaluate the possibility of eliminating them and thus reduce the cost, the size and the weight of the overall system. Also a comparison with up-to-date Silicon inverters is done.

As mentioned in chapter 2, the normally-on devices exhibit better reverse and forward characteristics than the normally-off SiC Jfet while they have lower power losses. In addition, the ac-coupled gate driver discussed in chapter 3 is the most suitable one for our application in order to get the most out of the special properties of the new devices. This novel gate driver provides low gate current during conduction, low gate power losses, has the ability to protect the device from breaking down into avalanche and gives the opportunity to operate in higher temperatures. Finally classic *R-C* snubber circuits with optimum values, boot resistors and gate-source clamp capacitors are used while great effort has been made to optimize the PCB designs for both the gate driver and the inverter circuit. Separated heat sinks and positive blanking times have been chosen to minimize the oscillations and overcome ringing problems.

Firstly, the basic background for the inverter is introduced. An example of an ideal inverter system is given in the beginning. Next the total losses and efficiency of a silicon carbide based single phase inverter are studied with analytical methods while the temperature dependence of them is shown. Secondly, various types of modulation are presented like Sinusoidal PWM and Space Vector Modulation. SPWM algorithm is chosen as a more reliable solution and output signals are produced and loaded to DSP in order to provide them to the gate drivers. Furthermore, the cooling demands for the new devices are discussed and applied to our circuit. Simulations in Pspice, based on the new SiC Jfet models (both Depletion and Enhancement mode), are shown and a comparison is made between them and the traditional Silicon inverters which show the superior performance of the new semiconductors. Finally, the construction method of the inverter is explained and the experimental results are displayed while the total system is evaluated.

5.1 Background

In this section we discuss inverters with single phase *ac* outputs. The input to switch-mode inverter is assumed to be a dc voltage source. Such inverters are referred to as voltage source inverters (VSI). The other types of inverters are the current source inverters (CSI) used only for high power ac motor drives where the dc input to the inverter is a dc current source. The VSIs can be further divided into the following three general categories:

1. *Pulse-width-modulated inverters*. In these inverters, the input dc voltage is essentially constant in magnitude where a diode rectifier is used to rectify the line voltage. Therefore, the inverter must control the magnitude and the frequency of the ac output voltages. This is achieved by PWM of the inverter switches and hence such inverters are called PWM inverters. There are various schemes to pulse-width modulate the inverter switches in order to shape the output ac voltages to be as close to a sine wave as possible. Out of these various schemes, a scheme called sinusoidal PWM will be discussed in detail and some other PWM techniques will be described in a separate section.

2. *Square-wave inverters*. In these inverters, the input dc voltage is controlled in order to control the magnitude of the output ac voltage and therefore the inverter has to control only the frequency of the output voltage. The output ac voltage has a waveform similar to a square wave and hence these inverters are called square-wave inverters.

3. *Single-phase inverters with voltage cancellation.* In case of inverters with single phase output, it is possible to control the magnitude and the frequency of the inverter output voltage, even though the input to the inverter is a constant dc voltage and the inverter switches are not pulse-width modulated (and hence the output voltage is like a square wave). Therefore, these inverters combine the characteristics of the previous two inverters. It should be noted that the voltage cancellation technique works only with single-phase inverters and not with three-phase inverters.

For simplicity, we consider a single phase-inverter with anti-parallel diodes, shown in Figure 139, where the output voltage of the inverter is filtered so that v_o can be assumed to be sinusoidal. Since the inverter supplies an inductive load such as an ac motor, i_o will lag v_o as in Figure 140.

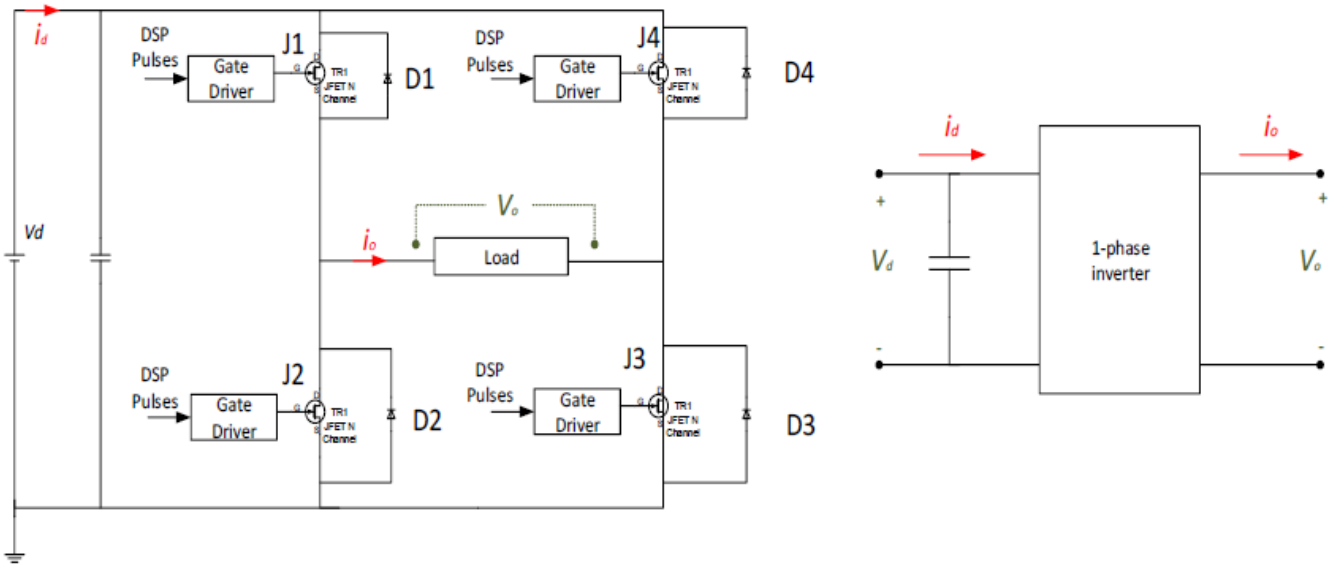


Figure 139. Single phase switch-mode inverter.

The output waveforms show that during interval 1, v_o and i_o are both positive and the current flow through [J1, J3] whereas during interval 3, v_o and i_o are both negative and [J2, J4] conduct. Therefore, during intervals 1 and 3, the instantaneous power flow $p_o = v_o \times i_o$ is from dc side to the ac side, corresponding to an inverter mode of operation.

In contrast, v_o and i_o are of opposite signs during interval 2 and 4, and therefore p_o flows from the ac side to the dc side of the inverter corresponding to a rectifier mode of operation. Interval 2 corresponds to positive voltage and negative current which means that the load is inductive and the current flow through [D1, D3]. Interval 4 is for capacitive load which means negative values of voltage and positive current and [D2, D4] conduct.

When the output voltage is zero and in the same time the output current has negative or positive value (p_o is zero), then one of the couple of semiconductor [J4, D1], [J2, D3], [J4, D1], [J2, D3] conducts and the output current flow is achieved. This current is called circulating current.

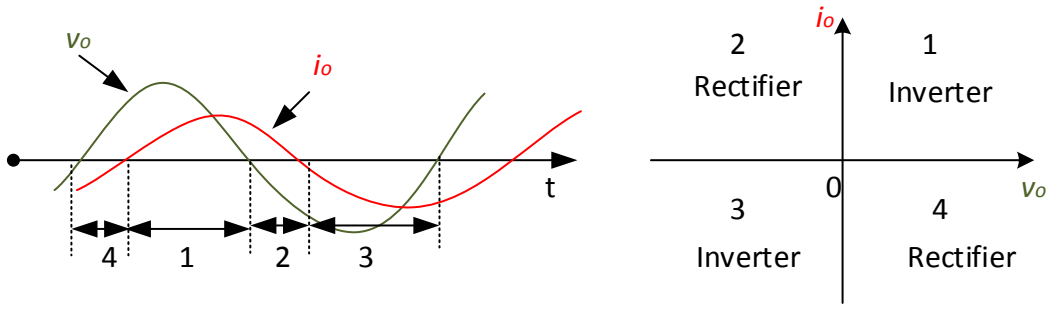


Figure 140. Inverter output waveforms and operation stages.

Hence the switch-mode inverter must be capable of operating in all four quadrants of the v_o-i_o plane. As was shown in chapter 2 due to the favorable reverse and forward characteristics of the *SiC VT JFET*, it is considered an ideal semiconductor for inverter circuit as it can operate in all four quadrants with satisfactory outputs.

In this thesis a Sinusoidal PWM inverter is constructed while the various types of modulations are explained in section (5.2). A sinusoidal waveform is tried to be extracted through the control of the magnitude and the frequency of the *ac*-outputs. First we present the ideal outputs of an imaginary inverter system equipped with ideal filters both in the dc input and ac output.

5.1.1 Ideal Full-bridge single phase Inverter system

A full-bridge inverter consists of two one-leg inverters (Figure 141) and is preferred in higher power ratings. With the same dc input voltage, the maximum output voltage is twice of the half-bridge inverter. This implies for the same power, the output current and the switch currents are one half of those for a half-bridge inverter. At high power levels, this is a distinct advantage, since it requires less paralleling of devices.

Next an ideal single phase inverter system is considered and a rough analysis of the outputs is studied. Fictitious *L*-*C* high frequency filter are used at the dc side as well as at the ac side, as shown in Figure 141. The switching frequency is assumed to be very high, approaching infinity. Therefore, to filter out the high-switching-frequency components in v_o and i_d, the filter components *L* and *C* required in both *ac*- and *dc*- side filters approach zero. This implies that the energy stored in the filters is negligible. Since the converter itself has no energy storage elements, the instantaneous power input must equal the instantaneous power output.

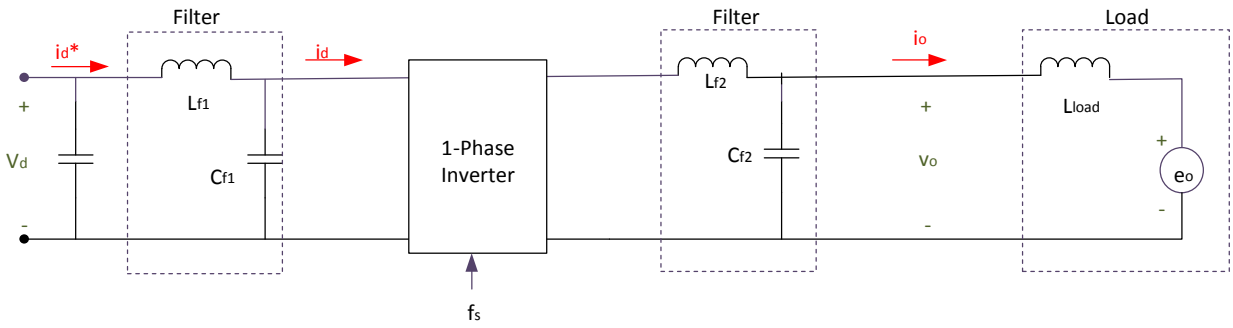


Figure 141. An ideal inverter system, while $fs \to \infty$, $Lf1$, $Cf1$, $Lf2$, $Cf2 \to 0$

Having made these assumptions, v_o is a pure sine wave at the fundamental output frequency ω_1,

$$v_{o1} = v_o = \sqrt{2} V_o \sin \omega_1 t \qquad (1)$$

If the load is as shown in Figure 141, where e_o is a sine wave at frequency ω_1, then the output current would also be sinusoidal and would lag v_o for an inductive load such as an ac motor.

$$i_o = \sqrt{2} I_o \, s(\omega_1 t - \varphi) \qquad (2)$$

where φ is the angle by which i_o lags v_o.

On the dc side, the *L-C* filter will filter the high switching frequency components in i_d and i_d^* would only consist of the low-frequency and dc components.

Assuming that no energy is stored in the filters,

$$V_d i_d^*(t) = v_o(t) i_o(t) = \sqrt{2} V_o \sin \omega_1 t \sqrt{2} I_o \sin(\omega_1 t - \varphi) \qquad (3)$$

Therefore,

$$i_d^*(t) = \frac{V_o I_o}{V_d} \cos \varphi - \frac{V_o I_o}{V_d} \cos(2\,\omega_1 t - \varphi) = I_d + i_{d2} = I_d - \sqrt{2} I_{d2} \cos(2\omega_1 t - \varphi) \qquad (4)$$

where

$$I_d = \frac{V_o I_o}{V_d} \cos \varphi \qquad (5)$$

and

$$I_{d2} = \frac{1}{\sqrt{2}} \frac{V_o I_o}{V_d} \qquad (6)$$

Equation (4) for i_d^* shows that it consists of a dc component I_d, which is responsible for the power transfer from V_d on the *dc* side of the inverter to the *ac* side. Also, i_d^* contains a sinusoidal component at twice of the fundamental frequency. The inverter input current i_d consists of i_d^* and the high-frequency components due to inverter switchings.

In practical systems, the previous assumption of a constant dc voltage as the input to the inverter is not entirely valid. Normally, this dc voltage is obtained by rectifying the ac utility line voltage. A large capacitor is used across the rectifier output terminals to filter the dc voltage. The ripple in the capacitor voltage, which also the dc input voltage to the inverter, is due to two reasons: (1) The rectification of the line voltage to produce dc does not result in a pure dc. (2) As shown from equation (4), the current drawn by a single-phase inverter from the dc side is not a constant dc but has a second harmonic component (of the fundamental frequency at the inverter output) in addition to the high-switching-frequency components. The second harmonic current component results in a ripple in the capacitor voltage, although the voltage ripple due to the high switching frequencies is essentially negligible.

Also, the assumption of ideal filters is not valid and practical impossible. This means that in order to build an inverter system relieved of high frequency harmonic components an analytical study must be done for the design of the filter for the specific application. However, this is not the scope of this thesis and more information can be found in bibliography.

5.1.2 Efficiency and power losses of a real single phase inverter

Methods for the calculation and simulation of semiconductor losses in the most common voltage source and current source PWM converters are well known. Conduction losses as well as switching losses are included in the calculation using a simplified model, based on power semiconductor data sheet information. Here an analytical calculation based on the theory is presented while the results of the study are used in the simulation and experimental section. Dependency of the semiconductor power losses on the type of the pulse width modulation is pointed out, showing the general behavior of power losses for inverter types.

Basis for the design of the cooling system of power electronic equipment, which is studied in the next section, is the determination of the expected power dissipation in the power semiconductors. There are mainly two kinds of power semiconductor losses to be considered, the conduction losses and the switching losses [3], [4]. The blocking as well as the driving losses usually can be neglected because as we will see in the simulation section the gate driver power requirements are very low in relation to the other losses [3].

For the prediction of losses in power semiconductor circuits different methods are known. One way is the complete numerical simulation of the circuit by special simulation programs with integrated or parallel running loss calculation [3]-[7]. The other possibility is to calculate the electrical behavior of the circuit analytically, i.e. current and voltage of the power semiconductors, to determine the semiconductor power losses [3], [4], [8], [9]. As this attempt yields extensive and complex mathematical problems simplified calculations are often used. For quick results and minimized calculation effort, simplified computations are the appropriate solution. For more detailed information, the numerical simulation of losses is useful, as the basic simulation is often executed to know the electrical behavior. A complete analytical calculation is more useful for basic investigations of circuits, to clearly see the dependencies of the losses on the causal parameters.

In this paragraph, the subject is the complete analytical calculation of the power semiconductor losses. The aim is to be able to predict the losses and most exactly, to clearly show the dependency of the losses on circuit parameters and operating point.

Silicon carbide (SiC) based semiconductor electronic devices and circuits are currently being researched and developed for use in high-temperature, high-power and high frequency conditions under which conventional Si-based semiconductors cannot perform adequately. Though there are different topologies available to minimize switching losses to obtain high efficiency in high power converters [19] the interesting features of SiC material that increase efficiency and enable it to function under such extreme conditions are expected to enable

significant improvements to systems such as electric power management, power distribution and on-board servo motor/actuator drivers due to their superior intrinsic properties in these operating areas. That's why a study in which the temperature dependency is involved is also developed.

Researchers hope to reduce power losses further, and have set a target of cutting losses to 10% of the equivalent Si inverter's losses thus to save energy [6].Compared to an inverter using Si diodes and IGBT devices, the power loss was claimed to be approximately 70% lower and the volume is approximately 25% of the Si-based design [20].

Basic Circuit and Loss Model

For the following calculations we consider an inverter circuit (Figure 142). A basically linear loss model for power semiconductors is assumed. Switching loss energies E_S will be linearized according to eq. (7). Conduction losses P_C for a single semiconductor will be calculated by eq. (8). Here E_{SR} is the rated switching loss energy given for reference commutation voltage V_{ref} and current i_{ref} while V_V and i_V indicate the actual commutation current and voltage respectively. V_0 and r constitute the semiconductors threshold voltage and differential resistance respectively.

$$E_s = E_{SR}\frac{V_V}{V_{ref}}\frac{i_V}{i_{ref}} \qquad (7)$$

$$P_C = V_0 i_V + r\, i_V^2 \qquad (8)$$

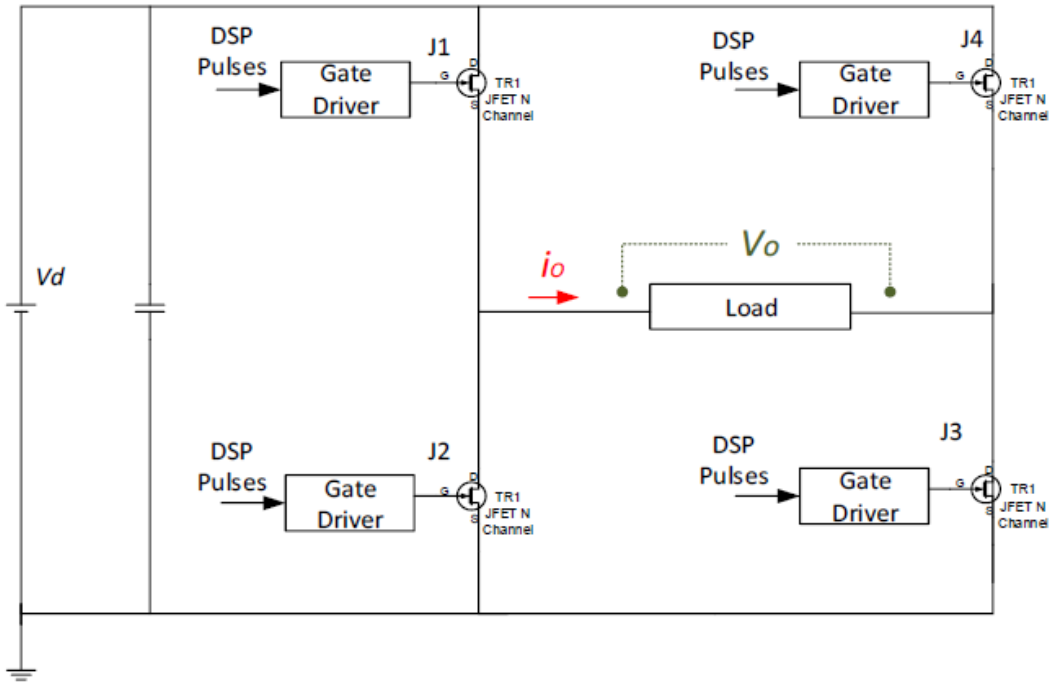


Figure 142. Inverter circuit.

The single phase inverter is regarded as being switched at a constant switching frequency for each switching device which in turn means that they are operated by continuous PWM only. Besides a constant dc link voltage is assumed. For the VSC the load current i_L is one important parameter for the switching losses. As the load current is considered sinusoidal for the following calculations, the converter's pulse rate is assumed to be appropriately high.

Switching Losses

For a given switching frequency f_s, the single phase inverter has the same switching losses for all continuous PWM methods. Switching losses are also independent of the inverter modulation index M and the load power factor PF [12] but increase linearly with switching frequency.

The equation of the switching losses P_{SV} of a single phase VSC with sinusoidal ac line current devices is given by equation (9) from [3].

$$P_{SL} = \frac{2}{\pi} f_s \left(E_{ON,I} + E_{OFF,I} + E_{OFF,D}\right) \frac{V_{dc}}{V_{ref}} \frac{i_L}{i_{ref}} \qquad (9)$$

Here f_s is the switching frequency, $E_{ON,I}$ and $E_{OFF,I}$ are the turn-on and turn-off energies of the semiconductor respectively, $E_{OFF,D}$ is the turn-off energy in the power modules due to the reverse recovery charge current, V_{DC} is the dc link voltage and i_L is the peak value of the ac line current assumed to be sinusoidal. The switching energies provided by data sheets are given for a certain reference voltage V_{ref} equal to the blocking state voltage occurring before the corresponding commutation and a reference current I_{ref} which is the on-state current after this commutation. Note that eq. (9) only remains valid for continuous PWM as the switching losses become dependent on the phase angle when discontinuous PWM is introduced.

Switching Losses and temperature dependence

Next we consider a study in which we use analytical methods to compute the switching losses for different conditions. By [21], the effective switching energy loss of a SPWM controlled inverter is expressed as

$$E_{SW} = \frac{1}{2\pi} \int_{\varphi}^{\varphi+2\pi} E(\theta) d\theta \qquad (10)$$

Further, the switching energy loss is a function of current at a certain temperature. So it can be expressed as a polynomial function of current,

$$(i, temperature) = di^3 + ei^2 + fi \ (\mu J) \qquad (11)$$

where *d*, *e*, *f* are coefficients which are obtained from the curve fitting of the experimental data for the specific temperature.

So, we can find the effective switching power loss at the desired temperature by the following equation,

$$P_{SW} = f_{sw}E_{sw} = f_{sw} \times \left(\frac{2d}{3\pi}I^3 + \frac{e}{4}I^2 + \frac{f}{\pi}I\right) \quad (\mu J) \qquad (12)$$

Forward and Reverse Conduction losses

Conduction losses are not affected by f_s but depend on the modulation strategy, M and power factor PF. For commonly used switching frequencies, conduction losses of the two-level inverter are significantly lower than corresponding switching losses.

In contrast to the switching losses the conduction losses are directly depending on the modulation function that is used. In [3], [4], [8] formulas for reckoning the conduction losses depending on the modulation function are presented. The publications [9] and [10] provide extensive information on how to define a certain modulation function by the distribution of the duty cycles for the two different zero vectors.

Let's consider the modulation waveform of the common carrier based sinusoidal PWM $M_{SPWM}(\omega t)$ and suboptimal space vector PWM $M_{SVM}(\omega t)$ with equal distribution of duty cycles for the two zero vectors. With the knowledge of the relevant modulation function the conduction losses $P_{CL,I}$ of a single semiconductor are expressed by equation (13). Likewise the conduction losses that appear during the reverse conduction $P_{RL,I}$ can be written as in eq. (14). The sum gives the total conduction losses P_{CL} in eq. (15) for all four semiconductors.

$$P_{CL,I} = \frac{V_p i_L}{2\pi} \times \int_0^{\pi} \sin(\omega t) \times \frac{1 + M(t)}{2} d\omega t + \frac{r_{con} i_L^2}{2\pi} \times \int_0^{\pi} \sin^2(\omega t) \times \frac{1 + M(t)}{2} d\omega t \quad (13)$$

$$P_{RL,I} = \frac{V_{p\_r} i_L}{2\pi} \times \int_0^{\pi} \sin(\omega t) \times \frac{1 - M(t)}{2} d\omega t + \frac{r_{con\_r} i_L^2}{2\pi} \times \int_0^{\pi} \sin^2(\omega t) \times \frac{1 - M(t)}{2} d\omega t \quad (14)$$

$$P_{CL} = 4 \times (P_{CL,} + P_{RL,}) \qquad (15)$$

In these equations ω is the load current's angular frequency, $M(t)$ is the modulation function, V_p is the *SiC*'s forward threshold voltage, r_{con} is the SiC's differential resistance during forward conduction, V_{p_r} and r_{con_r} are the reverse threshold voltage and differential resistance respectively. The modulation function M(t) in case of carrier based sinusoidal PWM, $M_{SPWM}(\omega t)$, is a sine wave. Whereas in case of SVPWM this function represented by $M_{SVM}(\omega t)$ which in [10] is defined as a composition of sine and cosine functions with different peak values can be expressed as a Fourier sequence given by equation (15).

$$M_{SVM}(t) = M\sin(\omega t) + \frac{3\sqrt{3}}{8\pi}\sum_{k=0}^{\infty}\left(\frac{\sin(3(4k+1)\omega t)}{18k^2+9k+1} - \frac{\sin(3(4k+3)\omega t)}{18k^2+27k+10}\right) \qquad (15)$$

For the chosen PWM methods equations (13) and (14) turn into expressions (16) and (17).

$$P_{CL,I} = \frac{V_p i_L}{2\pi} \times \left(1 + \frac{M \times \pi}{4} cos\varphi\right) + \frac{r_{con} i_L^2}{2\pi} \times \left(\frac{\pi}{4} + M\left(\frac{2}{3} cos\varphi + F_{SVM}\right)\right) \quad (16)$$

$$P_{RL,I} = \frac{V_{p\_r} i_L}{2\pi} \times \left(1 - \frac{M \times \pi}{4} cos\varphi\right) + \frac{r_{con\_r} i_L^2}{2\pi} \times \left(\frac{\pi}{4} - M\left(\frac{2}{3} cos\varphi + F_{SVM}\right)\right) \quad (17)$$

In these equations M is the modulation index and ϕ is the displacement angle between the fundamental of the voltage waveform and the load current. In case of SVPWM the value of F_{SVM} is given according to equation (16), in case of sine-triangular PWM the value of F_{SVM} equals zero.

$$F_{SVM} = \frac{6\sqrt{3}}{\pi}\sum_{\nu=0}^{\infty}\left(\frac{\cos(k\varphi)}{k^5 - 5k^3 + 4k} - \frac{\cos(l\varphi)}{l^5 - 5l^3 + 4l}\right) \qquad (18)$$

for l=3(4ν+1); k=3(4ν+3).

By comparing the results of equation (18) which are considerably low with the amount of total conduction losses it can be concluded that the term F_{SVM} can be neglected. Thus the conduction losses for SVPWM may be computed in the same way as for sine-triangular PWM as a good approximation. From equation (16) and (17) it becomes obvious that the displacement angle ϕ is another influence parameter for the determination of the conduction losses, except in the case that the rated loss of forward and reverse parameters are equal.

Conduction Losses and temperature dependence

In order to show the dependency of the temperature in the conduction losses like we did for the switching ones, an expression for P_c must be found which involves the on-state resistance of the device.

The conductive losses at a number of points (P_c) were calculated from within the linear region of operation following equation

$$P_c = V \times I \times T \qquad (19)$$

where V is voltage across device, I is the current through the device and T is duty cycle assumed of the pulse for a square-wave PWM.

For SiC JFETs and MOSFETs, the conduction loss is mainly caused by on-state resistance, R_{on}. It is calculated by

$$P_c = I_{rms}^2 \times R_{on} \qquad (20)$$

where I_{rms} is the effective current flowing in the device. For an inverter under SPWM control, the effective current can be expressed as [8]

$$I_{rms} = I\sqrt{\frac{1}{8} + \frac{1}{3\pi}Mcos\varphi} \qquad (21)$$

where M is modulation index, I is the peak of phase current, and φ is the current phase angle with respect to voltage

Therefore, the conduction power loss is

$$P_c = I^2\left(\frac{1}{8} + \frac{1}{3\pi}Mcos\varphi\right) \times R_{on} \qquad (22)$$

the values of R_{on} are functions of device junction temperatures. By letting the on resistance be a quadratic function of current, it can be represented by

$$R_{on} = aT^2 + bT + c\ (m\Omega) \qquad (23)$$

where a, b, c are the obtained coefficients from the curve fitting of Resistance=f(Temperature) figure.

Gate driver power requirement

Here we provide a rough analysis of a gate driver power requirement to be used in a single phase inverter system. Further investigation on the gate drive can be found in chapter 3. The total power by the gate drive can be computed with the following equation

$$P_{GD\_Total} = f \times P_{SW} + P_{GD\_Internal} \qquad (24)$$

where

P_{GD_Total}: total supplied power to the gate drive
P_{SW}: Sum of the charge and the discharge power
$P_{GD\_Internal}$: Power consumed by the gate drive itself

We can compute the switching needs by

$$P_{SW} = Q_{in} \times V_{GG} \qquad (25)$$

where Q_{in} is the required gate charge we need to supply in order to turn-on/off the semiconductor and $V_{GG} = V_{GG+} - V_{GG-}$.
On the other hand the $P_{GD\_Internal}$ is the power we provide during the conduction and blocking state of the device.

Efficiency

The efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{total\_losses}} \qquad (26)$$

The decreased number of output voltage levels and the lower switching frequencies also have a negative impact on the output harmonic performance of the single-phase inverters, but this consideration is beyond the scope of this thesis.

Finally note that for a complete efficiency analysis of an inverter system the DC-link capacitors power losses are given by the following expression:

$$P_c = N \times R_C \times I_{rms}^2 \qquad (27)$$

where N is the number of capacitors used and R_C represents the Equivalent Series Resistance (ESR) of each capacitor. In reality, the ESR of electrolytic capacitors that are commonly used for inverter DC-links, varies with the frequency of capacitor current harmonics but can be considered constant.

5.1.3 Cooling demands

This section discusses the need to control the internal temperature of power electronic components and the factors to be considered in selecting passive components like heat sinks. A crucial criterion for the dimensioning of single phase PWM converters is the cooling of the power semiconductors and thus determination of power dissipation in the semiconductors at certain operating points and its maximum is needed.

With the increase in heat dissipation from microelectronic devices and the reduction in overall form factors, thermal management becomes a more and more important element of electronic product design. Both the performance reliability and life expectancy of electronic

equipment are inversely related to the component temperature of the equipment. The relationship between the reliability and the operating temperature of a typical Silicon and Silicon-Carbide semiconductor device shows that a reduction in the temperature corresponds to an exponential increase in the reliability and life expectancy of the device. Therefore, long life and reliable performance of a component may be achieved by effectively controlling the device operating temperature within the limits set by the device design engineers.

The theoretical upper limit on the internal temperature of a semiconductor device is the so-called intrinsic temperature T_i, which is the temperature at which the intrinsic carrier density in the most lightly doped region of the device equals the majority carrier doping density in that region. If the temperature is exceeded, the rectifying characteristics of the junction are lost because the intrinsic carrier density greatly exceeds the doping density and the depletion region that gives rise to the potential barrier is shorted out by the intrinsic carriers.

In a design process, one of the design inputs is the worst-case junction temperature. Device manufacturers typically guarantee the maximum values of device parameters such as on state conduction voltages, switching times and switching losses at a specified maximum temperature which is for SiC Jfet from Semisouth at 150^{o}C. Our system intended to have high reliability is designed in the worst case design input.

In designing power electronic equipment the heat sink size and weight, its location in the equipment cabinet and surrounding temperature should be taken into account. It is important to be able to mount the heat sinks with their fins in a vertical position with ample room for natural convection of the air without a fan. The possibility of heating by the sun must be considered as part of a worst-case set of design inputs.

A bad thermal design will make the equipment much less reliable than intended. We must keep in mind that the failure rate for semiconductor devices doubles for each 10-15^o C temperature rise above 50^{o}C. Also the leakage currents and switching times are increased while the breakdown voltages is reduced.

Keeping the junction temperature of a power device within reasonable bounds is the joint responsibility of the device manufacturer and the device user. The manufacturer minimizes the thermal resistance $R_{\theta jc}$ between the interior of the device where the power is dissipated and the outside of the case enclosing the device. The device user must provide a heat conduction path between the case of the device and the ambient so that thermal resistance $R_{\theta ca}$ between the case and the ambient (where the heat generated by device operation will ultimately be dissipated) is minimized in a cost-effective manner.

The user's responsibility is made easier by the wide availability of extruded aluminum heat sinks of various shapes that are used for cooling of the power semiconductor devices. The choice of a proper heat sink depends on the allowable junction temperature the device can tolerate. For a worst-case design, the maximum junction temperature $T_{j,max}$, the maximum ambient temperature $T_{a,max,}$ the maximum operating voltage and maximum onstate current are specified. The maximum on-state losses in the power devices can be calculated if the maximum duty ratio, maximum on-state current and maximum on-state resistance are known. The switching losses can be obtained by integrating the instantaneous power loss

with respect to time and averaging it over the switching time period. Therefore, P_{Loss}, which is the sum of the on-state losses and the average switching losses can be estimated.

From this information the maximum allowable junction-to-ambient thermal resistance can be estimated as

$$R_{\theta ja} = \frac{T_{j,max} - T_{a,\max}}{P_{Loss}} \qquad (28)$$

$$R_{\theta cs} = \frac{T_{c,max} - T_{s,\max}}{P_{Loss}} \qquad (29)$$

$$R_{\theta sa} = \frac{T_{s,max} - T_{a,\max}}{P_{Loss}} \qquad (30)$$

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \qquad (31)$$

The junction-to-case thermal resistance $R_{\theta jc}$ can be obtained from the semiconductor device data sheets and the case-to-sink thermal resistance depends on the thermal compound and the insulator used.

The computation method is the following. We can usually find $R_{\theta jc}$, the junction-case thermal resistance of the power transistor or MOSFET itself, from the manufacturer's data. Then add the thermal resistance of the thermal compound and this will give the total junction-to-heat sink resistance. We subtract this from the maximum $R_{\theta ja}$, and we get the maximum allowable heat sink resistance. Then we select a heat sink which will provide no more than this value of thermal resistance. Of course if we have the room, it's always a good idea to use a larger heat sink, with an even lower thermal resistance than the safe maximum. The power transistor will then run even cooler. The general rule of thumb is the larger the heat sink, the lower its thermal resistance.

The heat flow between the semiconductor die and ambient air is modeled as a series of resistances to heat flow; there is a resistance from the die to the device case, from the case to the heat sink, and from the heat sink to the ambient. The sum of these resistances is the total thermal resistance from the die to the ambient. Thermal resistance is defined as temperature rise per unit of power, analogous to electrical resistance, and is expressed in units of degrees Celsius per watt (°C/W). If the device dissipation in watts is known, and the total thermal resistance is calculated, the temperature rise of the die over ambient can be calculated.

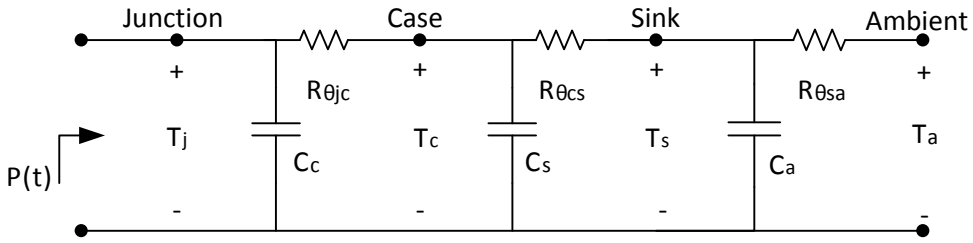


Figure 143. Electrical equivalent of a heatsink.

It is shown that the heat sink adds parasitic capacitances which are source of oscillations. That's why the capacitances must be minimized by using separate ones for each semiconductor device as was mentioned in the previous chapter.

Commercial extruded aluminum heat sinks have a thermal resistance (heat sink to ambient air) ranging from 0.4 °C/W for a large sink meant for TO3 devices, up to as high as 85 °C/W for a clip-on heat sink for a TO92 small plastic case.

Although a heat sink generally provides a much lower thermal resistance to the ambient, when we use one we inevitably introduce additional thermal resistances, each in series with the heat flow: the thermal resistance of the contact between the case and the heat sink $R_{\theta sa}$, which is largely due to tiny amounts of trapped air, and the thermal resistance of any electrical insulating washer (mica or plastic) we might need to use between the case and heat sink. Luckily we can minimize these last resistances by using a thin smear of thermal compound, a special paste which has very low thermal resistance. This can reduce the total case-heat sink thermal resistance to around 1.5°C/W or less.

In general, selecting an appropriate heat sink that meets the required thermal criteria, one needs to examine various parameters that affect not only the heat-sink performance itself, but also the overall performance of the system. The choice of a particular type of heat sink depends largely on the thermal budget allowed for the heat sink and external conditions surrounding the heat sink. It is to be emphasized that there can never be a single value of thermal resistance assigned to a given heat-sink, since the thermal resistance varies with external cooling conditions. When selecting a heat sink, it is necessary to classify the air flow as natural, low flow mixed, or high flow forced convection. Natural convection occurs when there is no externally induced flow and heat transfer relies solely on the free buoyant flow of air surrounding the heat sink. Forced convection occurs when the flow of air is induced by mechanical means, usually a fan or blower. The final step is to determine the required volume of a heat sink.

5.2 Modulations

There are many modulations techniques which are trying to minimize the harmonic component of an inverter circuit. In this section some basic modulation methods are presented in order to further investigate the gate pulses and the output waveforms that our system is going to produce.

5.2.1 Sinusoidal Pulse Width Modulation (SPWM)

In inverter circuits, we would like the output to be sinusoidal with magnitude and frequency controllable. In the simplest approach, the top switch is turned on and off only once in each cycle and a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved. In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage V_{in} is applied at the output. Note that over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period.

In order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal $v_{control}$ at the desire frequency is compared with a triangular waveform v_{tri}, (Figure 6). The triangular waveform v_{tri} is at a switching frequency f_s, which establishes the frequency with which the inverter switches are switched (f_s is also called the carrier frequency). The control signal $v_{control}$ is used to modulate the switch duty ratio and has a frequency f_1 (modulating frequency), which is the desired fundamental frequency of the inverter voltage output, recognizing that the inverter output voltage will not be a perfect sine wave and will contain voltage components at harmonic frequencies of f_1. The amplitude modulation ratio m_a is defined as

$$m_a = \frac{V_{control}}{V_{tri}} \qquad (32)$$

where $v_{control}$ is the peak amplitude of the control signal. The amplitude v_{tri} of the triangular signal is generally kept constant.

The frequency modulation m_f is defined as

$$m_f = \frac{f_s}{f_1} \qquad (33)$$

In the inverter, the switches are controlled based on the comparison between $v_{control}$ and v_{tri}.

J1 is on, J2 off ; if $v_{control} > v_{tri}$ (34)

J3 is on, J4 off ; if $v_{control} > -v_{tri}$ (35)

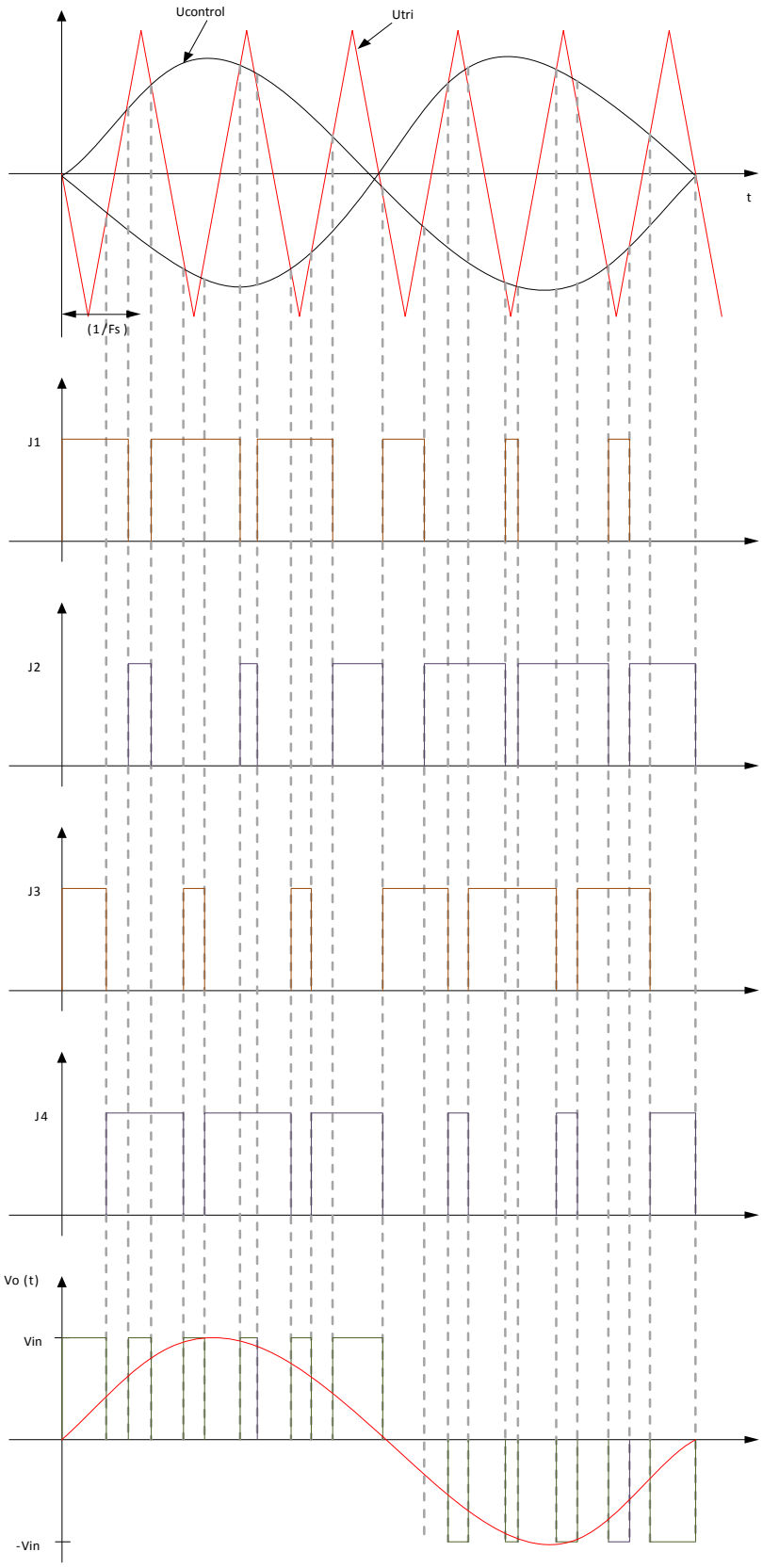


Figure 144. SPWM.

The resulting chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies close to the carrier frequency. Notice that the root mean square value of the ac voltage waveform is still equal to the dc bus voltage, and hence the total harmonic distortion is not affected by the PWM process.

The harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system. Note that controlling the modulation index therefore controls the amplitude of the applied output voltage. With a sufficiently high carrier frequency, the high frequency components do not propagate significantly in the ac network (or load) due the presence of the inductive elements. However, a higher carrier frequency does result in a larger number of switchings per cycle and hence in an increased power loss. Due to SiC Jfet low switching losses a SPWM inverter is able to operate in high frequencies in contrast to the traditional Silicon devices.

Note that with an odd ratio for m_f, the waveform is anti-symmetric over a 360 degree cycle. With an even number, there are harmonics of even order, but in particular also a small dc component. Hence an even number is not recommended for single phase inverters, particularly for small ratios of m_f.

Next we point out three basic things for the SPWM

1 The peak amplitude of the fundamental frequency component is V_o is $m_a$times V_{in}. the amplitude of the fundamental-frequency component of the output voltage varies linearly with m_a. Therefore the range of $m_a$from 0 to 1 is refereed as the linear region.

$$V_{o1} = m_a V_{in}, \qquad m_a \leq 1.0 \qquad (36)$$

and

$$V_{in} < V_{o1} < \frac{4}{\pi} V_{in} \ \ (m_a > 1.0) \qquad (37)$$

The output voltage waveform of leg A is determined by comparison of $v_{control}$ and v_{tri}. The output of inverter leg B is negative of the leg A output, $V_{oA} = -V_{oB}$.

2. The harmonics in the inverter output voltage waveform appear as sidebands around the switching frequency and its multiples, that is around m_f, $2m_f$, $3m_f$ and so on.
The harmonic amplitudes are almost independent of m_f though it defines the frequencies at which they occur. Theoretically the frequencies at which voltage harmonics occur can be indicated as

$$f_h = (jm_f \pm k)_1 \qquad (38)$$

that is the harmonic order h corresponds to the kth sideband of j times the frequency modulation ratio m_f;

$$h = (m_f) \pm k \qquad (39)$$

where the fundamental frequency corresponds to h=1.

3. The harmonic m_f should be an odd integer. Therefore only odd harmonics are present and the even ones disappear from the waveform of V_o. Moreover, only the coefficients of the sine series in the Fourier analysis are finite; those for the cosine series are zero.

Next we discuss the selection of the switching frequency and the frequency modulation m_f. Because of the relative ease in filtering harmonic voltages at high frequencies, it is desirable to use as high a switching frequency as possible. For 50 or 60 Hertz type applications, such as ac motor drives (where the fundamental frequency of the inverter output may be required to be as high as 200Hz), the frequency modulation m_f may be 9 or even less for switching frequencies of less than 2kHz. On the other hand, m_f will be larger than 100Hz for switching frequencies higher than 20kHz.

- Small mf ($m_f \leq 21$)

1. *Synchronous PWM*. For small values of mf, the triangular waveform signal and the control signal should be synchronized to each other. This synchronous PWM requires that m_f be an integer. The reason for using the synchronous PWM is that the asynchronous PWM (where m_f is not an integer) results in subharmonics (of the fundamental frequency) that are very undesirable in most applications. This implies that the triangular waveform frequency varies with the desired inverter frequency.

2. m_f should be an odd integer so that only odd harmonics are present.

- Large m_f ($m_f > 21$)

The amplitudes of subharmonics due to asynchronous PWM are small at large values of m_f. Therefore, at large values of m_f, the asynchronous PWM can be used where the frequency of the triangular waveform is kept constant, whereas the frequency of $v_{control}$ varies, resulting in noninteger values of m_f. However, if the inverter is supplying a load such as an ac motor, the subharmonics at zero or close to zero frequency even though small in amplitude will result in large currents that will be highly undesirable. Therefore, the asynchronous PWM should be avoided.

Finally we refer to the effect of the overmodulation (m_a>1.0). In the previous discussion it was assumed that m_a <1.0, corresponding to a sinusoidal PWM in the linear range. Therefore, the amplitude of the fundamental-frequency voltage varies linearly with m_a. In the range of m_a <1.0, PWM pushes the harmonics into a high-frequency range around the switching frequency and its multiples. In spite of this desirable feature of SPWM in the linear range, one of the drawbacks is that the maximum available of the fundamental-frequency component is not as high as we wish.

To increase further the amplitude of the fundamental-frequency component in the output voltage, m_a is increased beyond 1.0, resulting in what is called overmodulation.

Overmodulation causes the output voltage to contain many more harmonics in the sidebands as compared with the linear range (with $m_a \leq 1.0$). The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. More significantly, with overmodulation, the amplitude of the fundamental-frequency component does not vary linearly with amplitude modulation ratio m_a.

With overmodulation regardless of the values of m_f, it is recommended that a synchronous PWM operation be used, thus meeting the requirements indicated previously for a small value of m_f.

Overmodulation is usually used in induction motor drives while it is avoided in uninterruptible power supplies because of a stringent requirement on minimizing the distortion in the output voltage.

5.2.2 Square-wave switching scheme

In the square wave switching scheme, each switch of the inverter leg is on for one half cycle of the desired output frequency. From Fourier analysis, the peak values of the fundamental frequencies and harmonic components in the inverter output waveform can be obtained for a given input V_{in} as

$$V_{o,n} = \frac{4}{n\pi} V_{in} \sin\left(\frac{n\delta}{2}\right) \qquad (40)$$

It should be noted that the square wave switching is also a special case of the SPWM switching when m_a becomes so large that the control voltage waveform intersects with the triangular waveform only at zero crossing of vcontrol. Therefore, the output voltage is independent of m_a in the square-wave region.

One of the advantages of this operation is that each inverter switch changes its state only twice per cycle, which is important at very high power levels where the solid state switches generally have slower turn-on and turn-off speeds. One of the serious disadvantages is that the inverter is not capable of regulating the output voltage magnitude. Therefore the dc input voltage V_{in} to the inverter must be adjusted in order to control the magnitude of the inverter output voltage.

5.2.3 Space Vector Modulation

While in Sinusoidal PWM the inverter can be thought as three separate push-pull driver stages which create each phase waveform independently, SVM treats the inverter as a single unit.

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM). It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D

amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

To implement space vector modulation a reference signal V_{ref} is sampled with a frequency f_s ($T_s = 1/f_s$). The reference signal may be generated from three separate phase references using the $\alpha\beta\gamma$ transform. The reference vector is then synthesized using a combination of the two adjacent active switching vectors and one or both of the zero vectors. Various strategies of selecting the order of the vectors and which zero vector(s) to use exist. Strategy selection will affect the harmonic content and the switching losses.

More complicated SVM strategies for the unbalanced operation of four-leg three-phase inverters do exist. In these strategies the switching vectors define a 3D shape (a hexagonal prism in $\alpha\beta\gamma$ coordinates or a dodecahedron in abc three-Dimensional Space Vector Modulation in abc coordinates) rather than a 2D hexagon.

In general, SVM is simple and puts in our system less switching losses due to the less frequent switching of the semiconductors in comparison with SPWM.

5.2.4 Conclusions

In this section a discussion between three major modulation techniques was done in order to choose the right one for the single-phase SiC inverter. SVM is mainly used for three-phase inverters and implementation for single-phase would be a challenge.

Moreover the advantages of SPWM like lower power consumption, high power handling capability and easiness to implement and control make it the modulation of our inverter. Also, due to the low switching losses of the new devices (Chapter 2) they give us the opportunity of using SPWM technique in order to face less harmonic effects in the output waveforms.

In the final section the algorithm of SPWM is loaded in DSP and provides the signals in the gate drivers. The modulation ratio m_a equals to 0.8 while the carrier frequency decided to be 5kHz and the modulating frequency 50Hz. The dead time was 1μs. SPWM was also simulated and used in single-phase inverters with Pspice in the next section.

5.3 Simulations

In this section we proceed to the simulation of a single-phase inverter circuit. In the first part we present the simulated output waveforms of the constructed inverter in the final section of the thesis while in the second part a comparison study based on simulations in the same conditions (temperature and parasitic elements) and the power loss theory analysis previously done, is presented between the most important characteristics of traditional silicon and silicon-carbide inverters.

5.3.1 Simulation of a single-phase inverter using DM SiC JFET

The simulated circuit is displayed in *Figure 145*. Our single-phase inverter is exploiting only Normally-on SiC devices produced by Semisouth due to its favorable forward and inverse characteristics in relation with the normally-off Jfet. We have also added parasitic inductances to the simulation circuit to approach the real conditions.

SPWM technique is used with carrier frequency 5 kHz. Output voltage fundamental frequency is 50 Hz and the dead time was chosen 1μs. The R-C snubber circuit investigated in the previous chapter are placed across the semiconductors to minimize the oscillations (R=70 Ω, C=1 nF). The simulation software used is Pspice and the DM VT SiC Jfet SJDP120R085 model is the one created in chapter 2. The gate driver is the ac-coupled studied in chapter 3 (Figure 8).

We assume a DC bus voltage 400 V which provide the system with 1kW power, and the load is an RL load (R=47 Ω, L=0.15 H). The temperature was considered constant and equal with 25^{o} C.

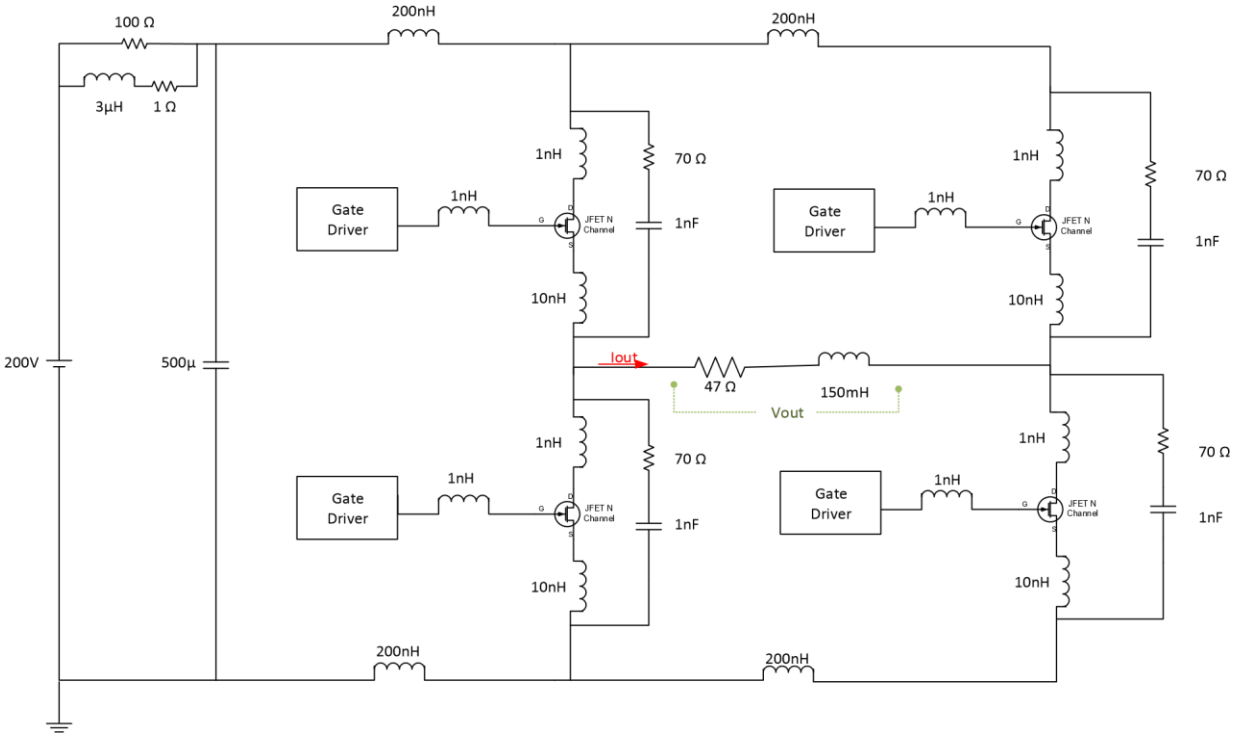


Figure 145. Single-phase SiC Inverter System.

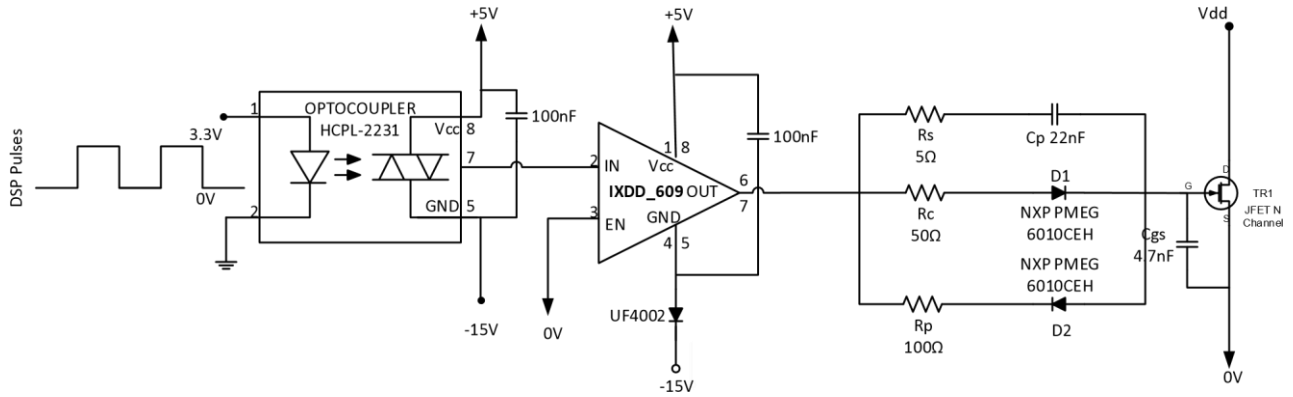


Figure 146. Ac-coupled gate drive circuit.

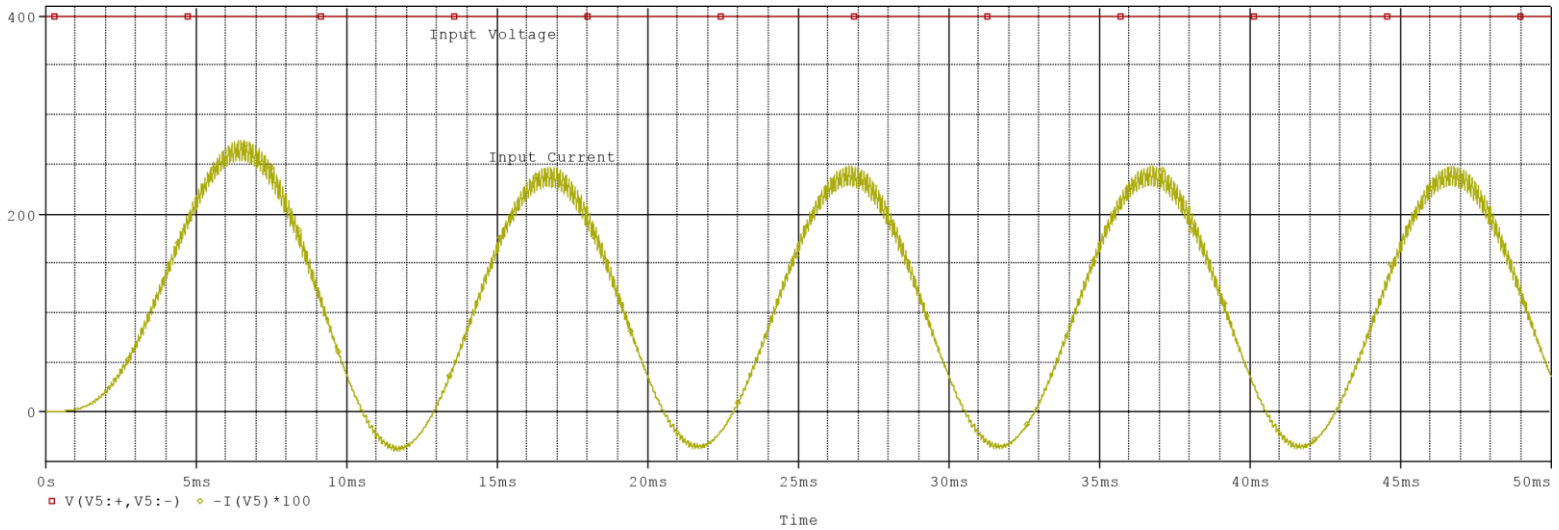


*Figure 147. Input voltage and current (*100) waveform of SPWM Single Phase full bridge inverter system.*

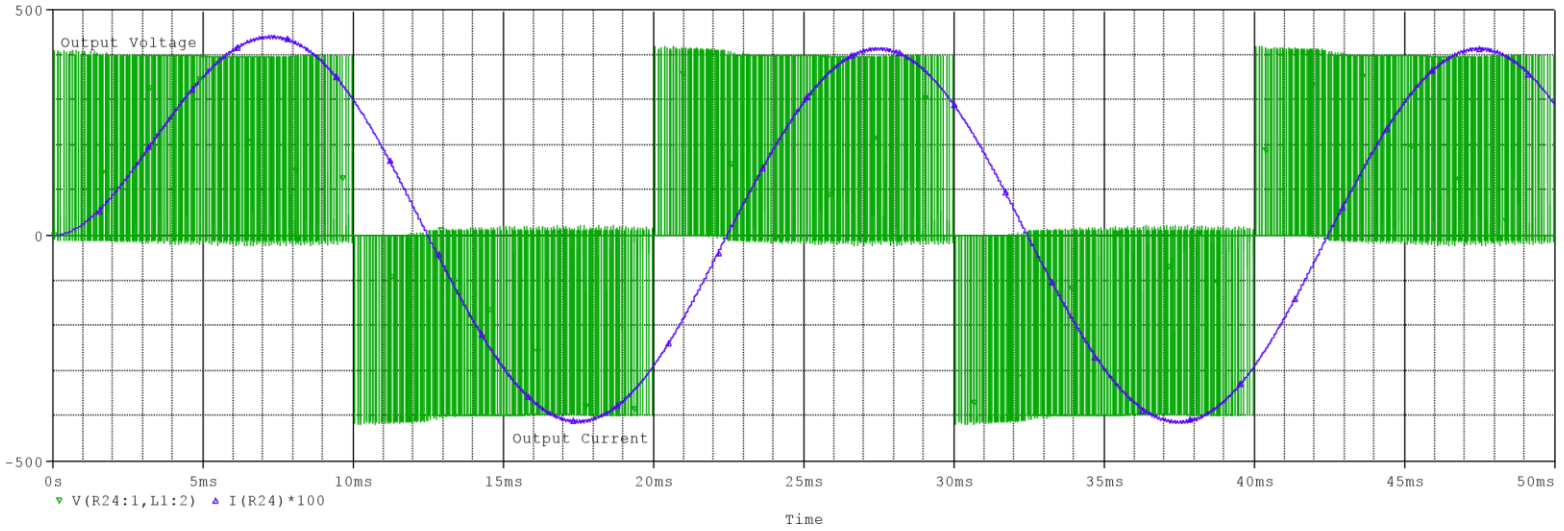


*Figure 148. Output voltage and current (*100) waveform of Single Phase full bridge inverter system using Normally-on SiC JFet devices.*

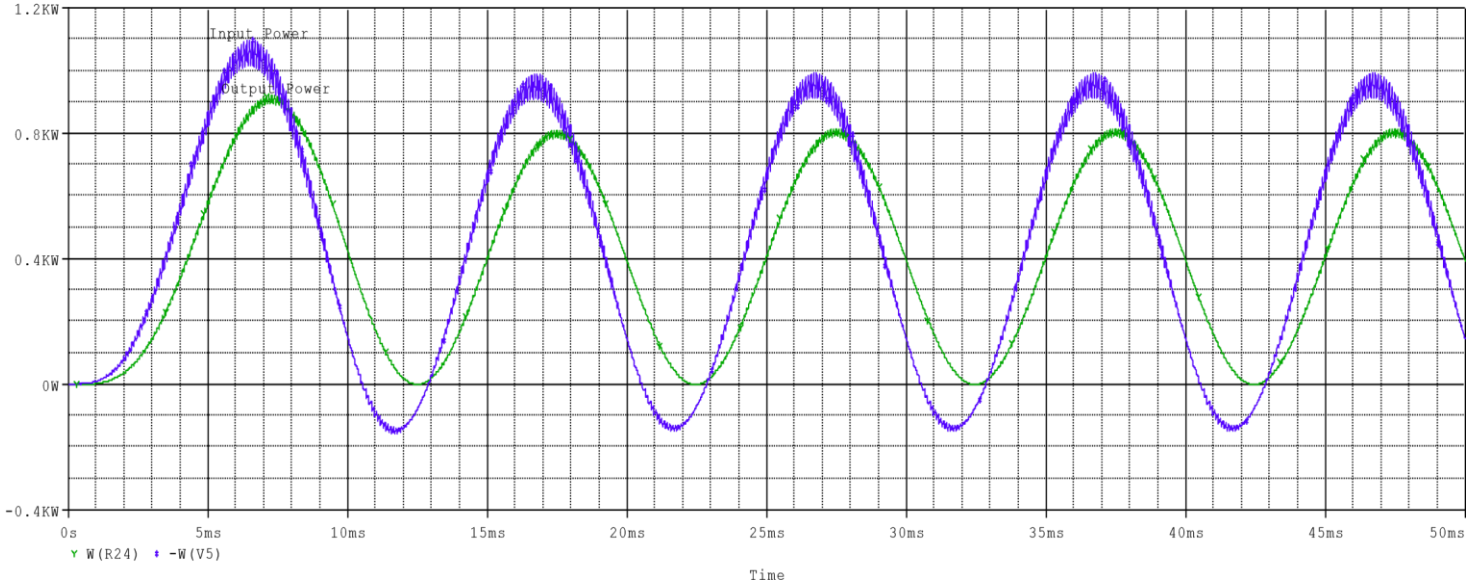


Figure 149. Input and output power waveform of a single phase inverter using Normally-on SiC JFet devices.

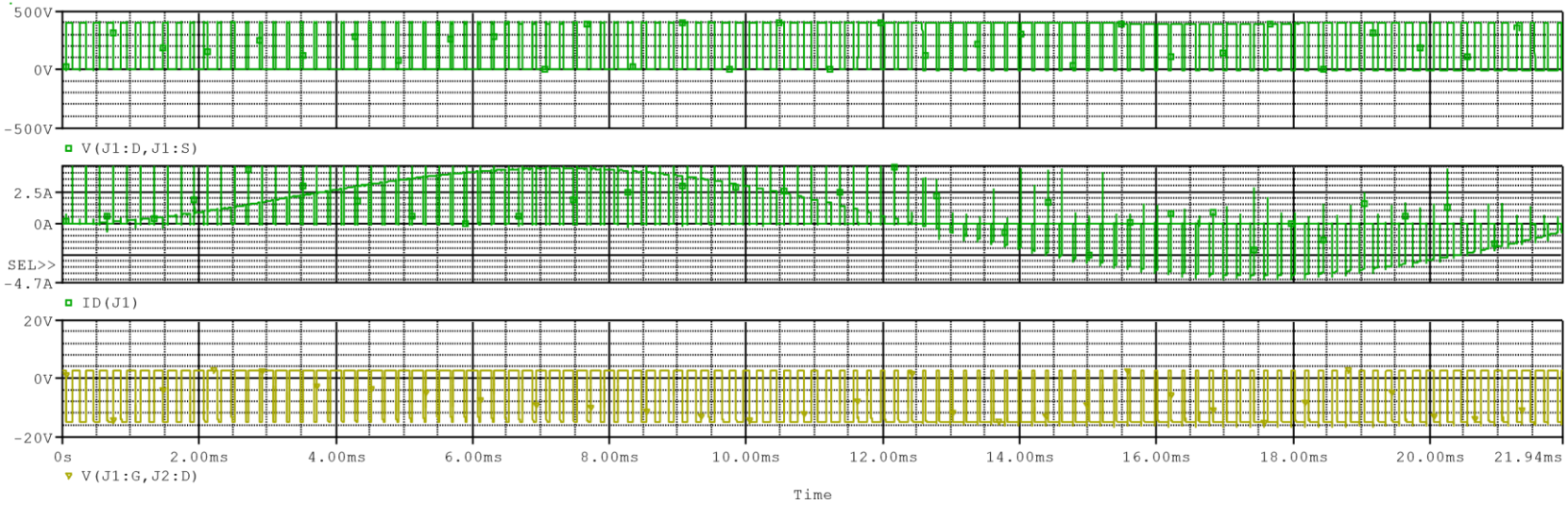


Figure 150. Output voltage, output current, gate-source voltage of J1 DM JFET – spwm pulses.

An inverter was simulated using the DM SiC Jfet SJDP120R085 by Semisouth. The input and output waveforms are shown in *Figure 147* - *Figure 150*. The results of the simulated inverter are summarized in the next table.

	1-Phase inverter using SJDP120R085
Efficiency (%)	95.399645 %
Cooling demands (C/W)	3.846102072 C^{o}/W
Gate driver losses (W)	0.32 W
Conduction losses (W)	0.8 W
Losses during dead time(μW)	350 μW
Switching losses (W)	0.7 W

The efficiency of the inverter was measured 95,4 % while the dominant losses are the forward and reverse conduction ones. The reverse conduction losses happen during the operation of the inverter in interval 2 of Figure 2 where we exploit the reverse conduction properties of the device. These losses are dependent from the load and the power factor of the system which defines the phase lag of the current.

The switching losses have been reduced a lot due to the correct choice of the snubber circuits and the appropriate gate signals provided by our ac-coupled gate driver. The losses during the dead time have been kept very low due to the short dead time (1μs).

Of course the efficiency of the converter may be boosted if we minimize the parasitic elements in the circuit and by placing a filter in the input and output of the system in order to filter out the voltage and current harmonics.

Next we show the effect of adding a SiC antiparallel diode as well as a presentation of Si devices efficiency in the same conditions is displayed.

5.3.2 Analytical study of Silicon and Silicon Carbide based inverters

In this section a comparison study is done based on simulations in Pspice. Inverter circuits using

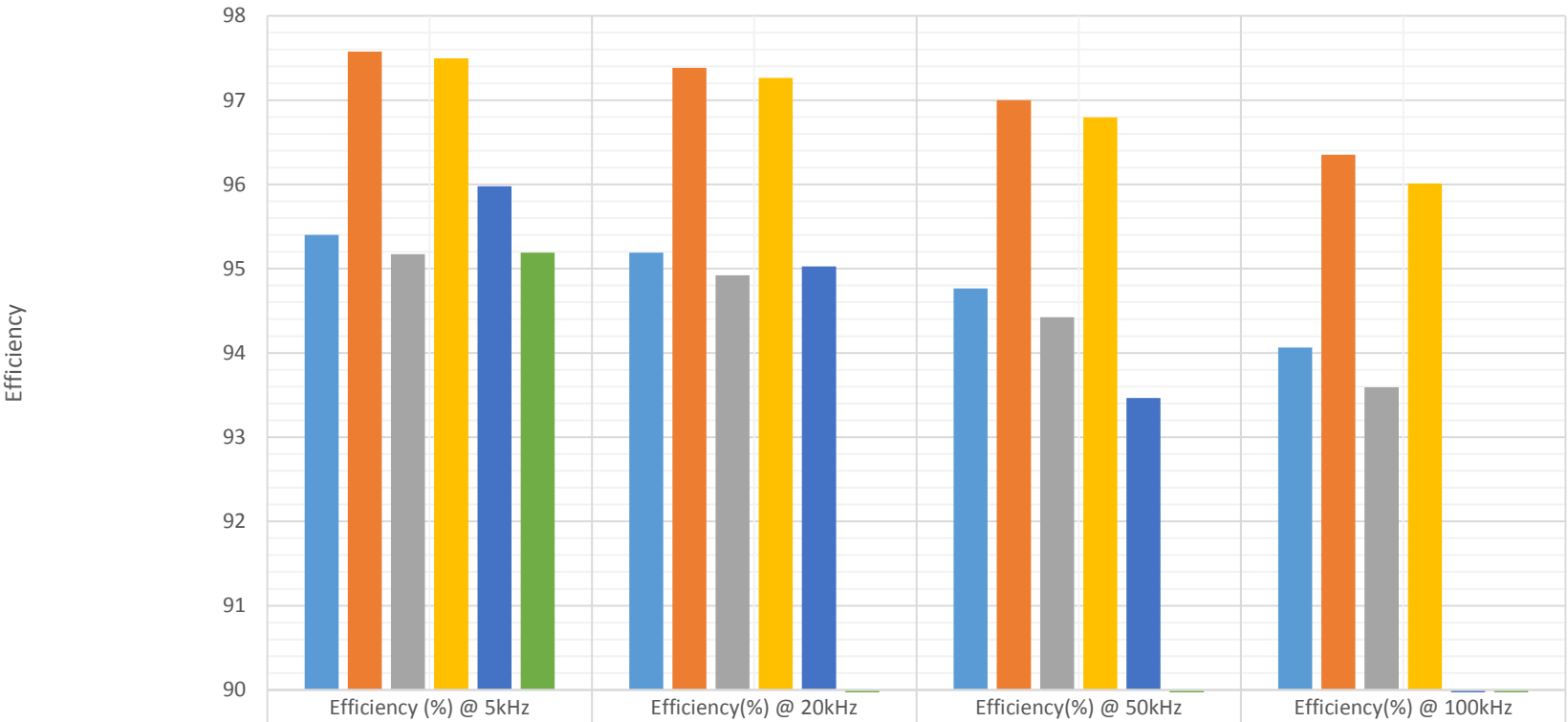
1. Only *DM VT SiC Jfet SJDP120R085*,
2. *DM VT SiC Jfet SJDP120R085* with antiparallel diode *SiC Power Schottky Diode SDP30S120*
3. Only *EM VT SiC Jfet SJEP120R100*
4. *EM VT SiC Jfet SJEP120R100* with antiparallel diode *SiC Power Schottky Diode SDP30S120*
5. 600V MOSFET, *FQPF12N60C* (contains anti-parallel diode)
6. 1200V IGBT, *FGA25N120* (contains anti-parallel diode)

are simulated and compared on the same inverter circuit as in Figure 7. The gate drives used for Mosfet and IGBT can be found in [32].

The input power is 1kW while tests are done for various frequencies in order to evaluate the efficiency of the new SiC devices compared to the traditional Si ones.

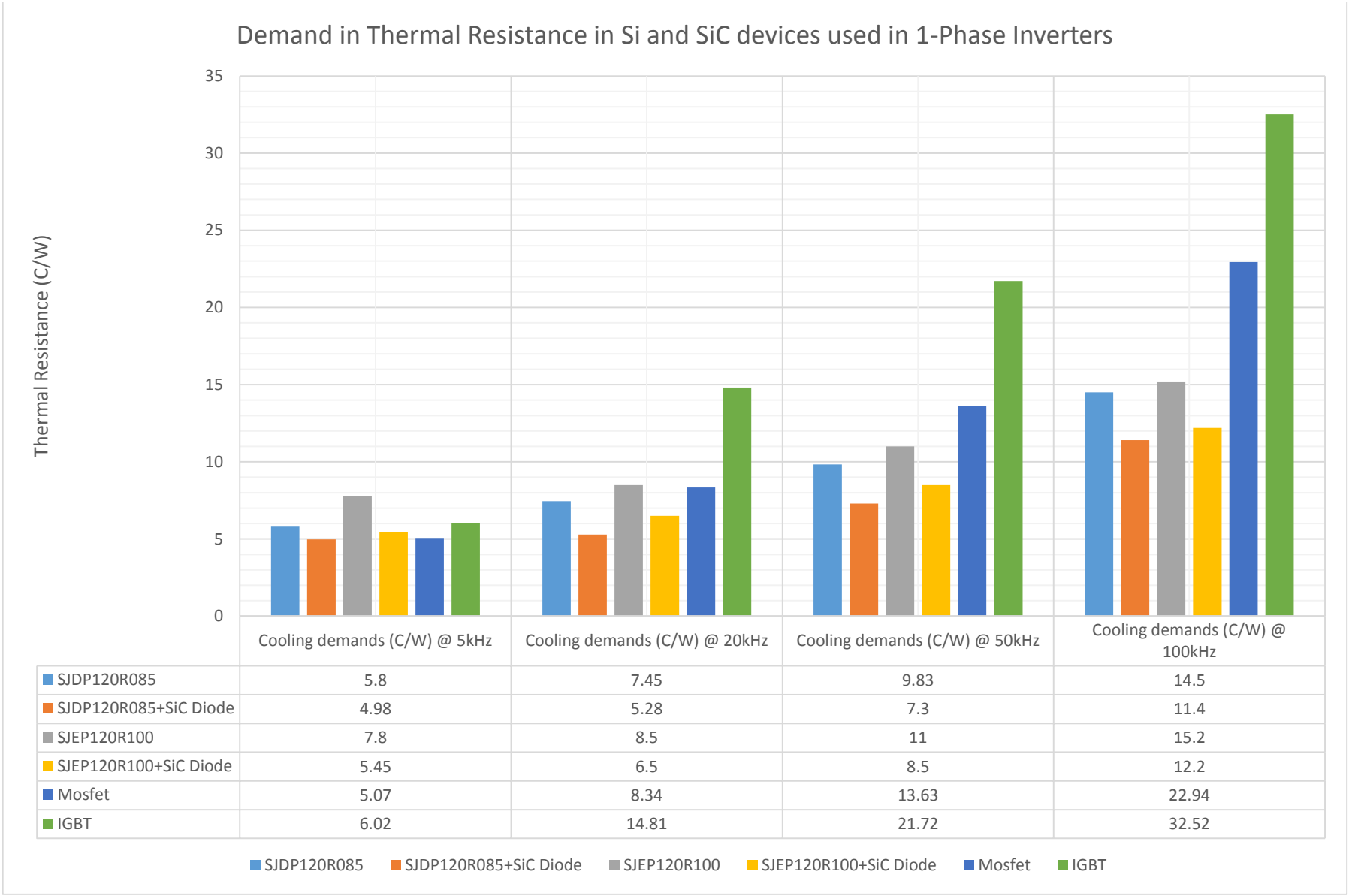
In the next plots we compare the efficiency, cooling demands, gate driver requirements, switching losses for different frequencies. Also the reverse and forward conduction losses as well as the losses during the dead time are shown for all the devices.

Finally a study for the effect of the applied gate voltages in the losses and the efficiency of the SiC JFets DM and EM is done.



	Efficiency (%) @ 5kHz	Efficiency(%) @ 20kHz	Efficiency(%) @ 50kHz	Efficiency(%) @ 100kHz
SJDP120R085	95.399645	95.18837	94.76645	94.063565
SJDP120R085+SiC Diode	97.575678	97.3827	96.99678	96.353598
SJEP120R100	95.172692	94.9223555	94.4230928	93.5917164
SJEP120R100+SiC Diode	97.49777	97.2631355	96.7938728	96.0117944
Mosfet	95.97652	95.0272515	93.464709	88.451852
IGBT	95.19095	88.58889	73.384884	48.044982

Figure 151. Efficiency of Single phase Inverter of different SiC and Si devices for various frequencies.



	Cooling demands (C/W) @ 5kHz	Cooling demands (C/W) @ 20kHz	Cooling demands (C/W) @ 50kHz	Cooling demands (C/W) @ 100kHz
SJDP120R085	5.8	7.45	9.83	14.5
SJDP120R085+SiC Diode	4.98	5.28	7.3	11.4
SJEP120R100	7.8	8.5	11	15.2
SJEP120R100+SiC Diode	5.45	6.5	8.5	12.2
Mosfet	5.07	8.34	13.63	22.94
IGBT	6.02	14.81	21.72	32.52

Figure 152 .Cooling demands for Single phase Inverter of different SiC and Si devices for various frequencies.

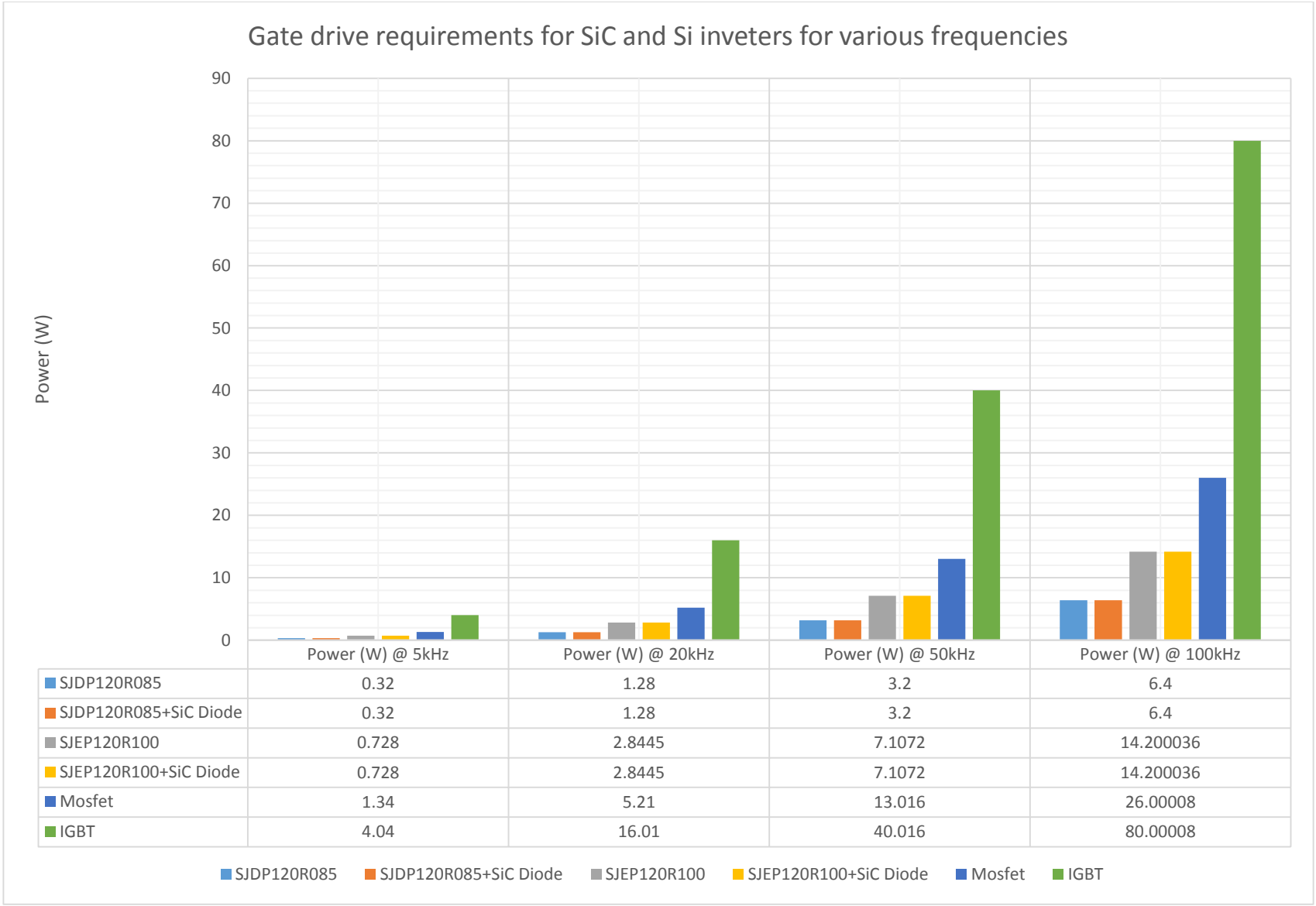


Figure 153. Gate driver power requirements of Single phase Inverter of different SiC and Si devices for various frequencies.

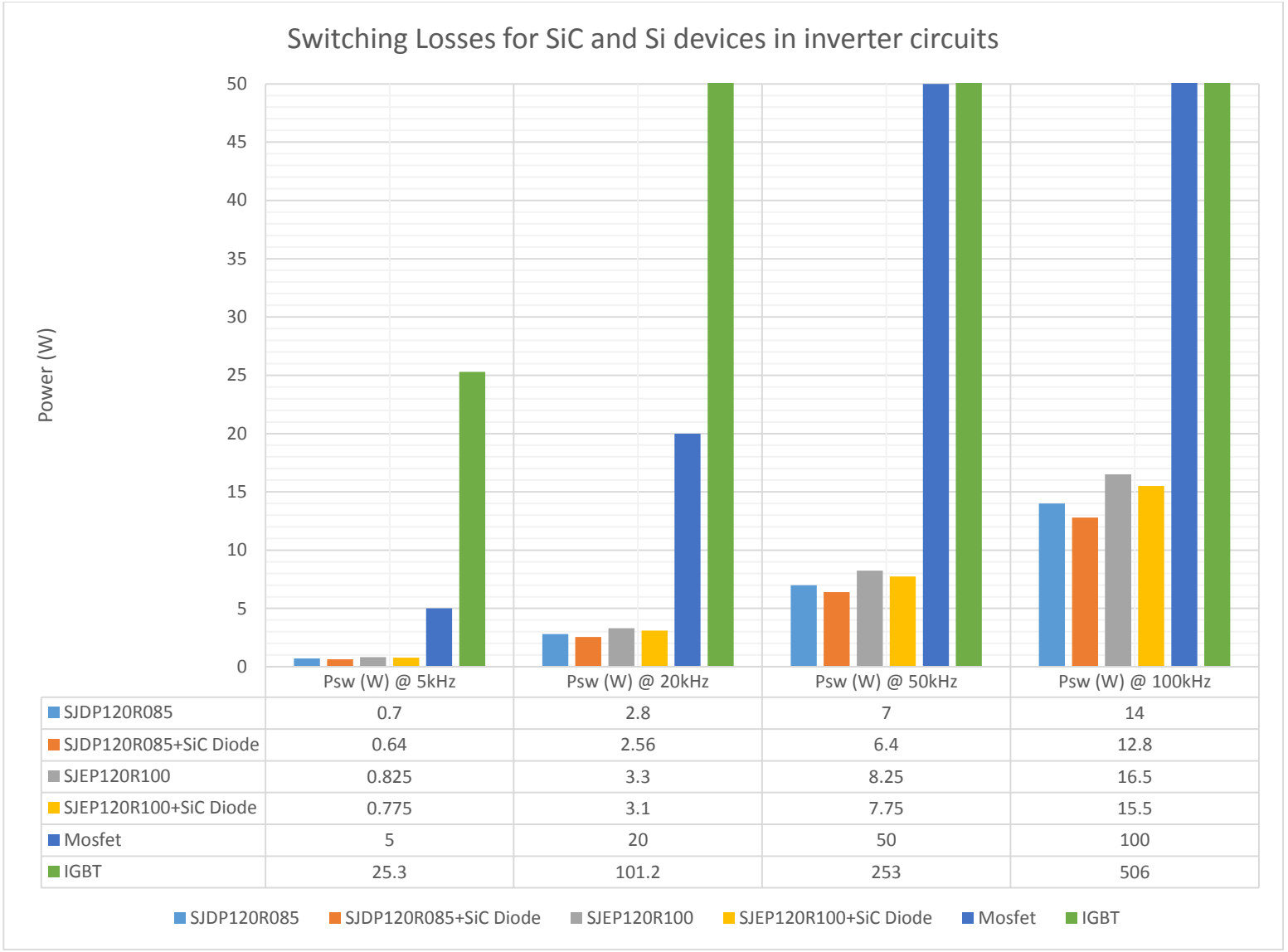


Figure 154. Switching losses of Single phase Inverter of different SiC and Si devices for various frequencies

- In Figure 151 we can see the efficiency for various frequencies. The inverter based on SiC JFETs and SiC freewheeling diodes exhibit the best performance. After it is the Depletion-Mode device and then the Mosfet with the Enhancement-Mode based inverter. As the frequency grows the SiC inverter efficiency remains constant and above 94% while the Si devices for over 20 kHz can't be used in systems due to their excessive losses. The difference for SiC inverters with and without freewheeling diodes is less than 2% and can be reduced more if better boards will be designed and output filters will be used. So we can say that for a home-use SiC inverter of low nominal power the use of antiparallel diodes are not necessary.

- As far as the cooling demands, Figure 152, is concerned it is obvious the advantage of using SiC devices. The thermal resistance is defined as the temperature rise per unit of power. So as much larger it is, the bigger the heat sink. The cooling demands for SiC are almost the same for all the frequencies while they are growing very fast for all the Si devices. That means that the SiC based inverters may be smaller, less heavy and as they don't need antiparallel diodes less expensive.

- Generally the requirements for the gate driver are not significant. The normally-on needs a peak current only during the turn-on and turn-off as during the conduction and blocking state the current is very small (~μA), that's why in Figure 153 we can see that it has the lower power demand. The normally-off needs more power due to the fact that it needs ~100mA in order to keep the channel on or off. But again they are very small. On the other hand the Si devices and especially the IGBT which was until today the dominant semiconductor choice for high power rating inverters has more power requirements.

- Finally, the switching losses for SiC devices are extremely low for low frequencies and acceptable as the frequency is growing. From Figure 154 it is obvious the reason why we can't use Si devices in high frequencies. Hence, it is clear that the switching energy losses of the SiC JFET are significantly lower than those of the Si IGBT and Mosfet under the same conditions. It can switch between on-state and off state with much lower dynamic energy loss per switching cycle. Also at the same allowable switching loss the SiC JFET could operate at higher frequency. The reduction in switching losses by using SiC enable the converter to operate at higher switching frequency with improved efficiency. Consequently the size of the output filter and other system costs could be reduced.

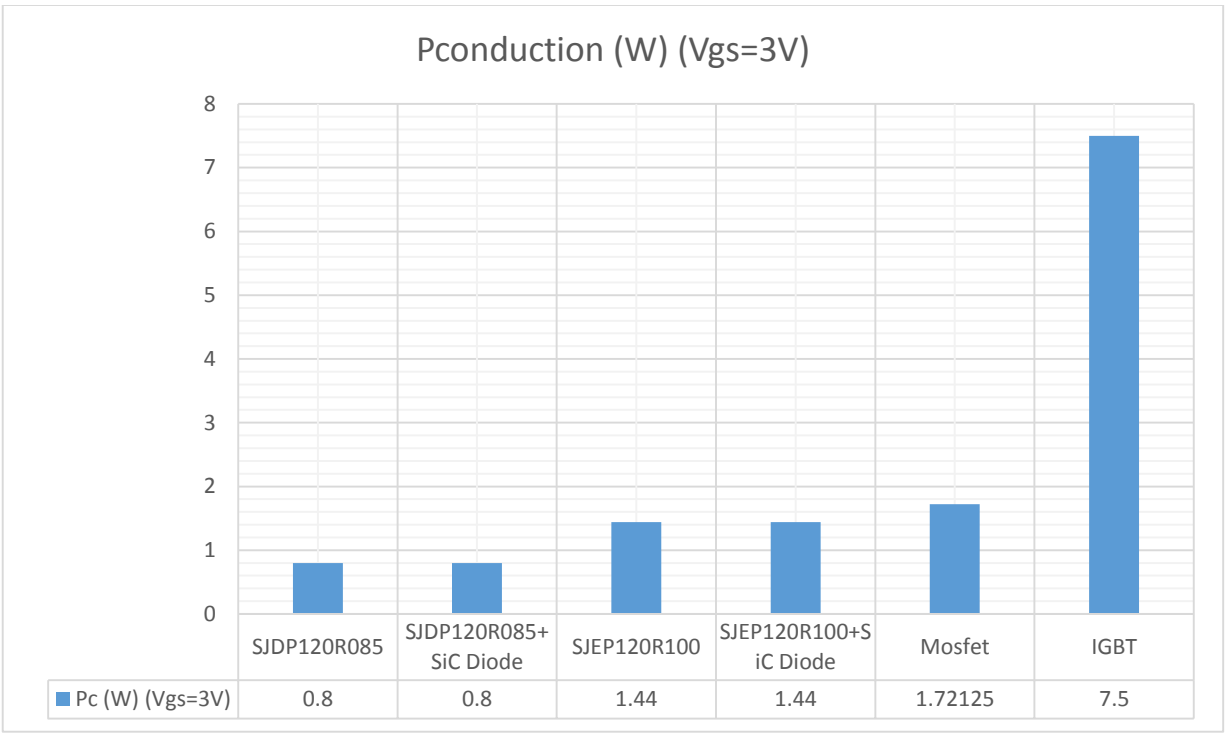


Figure 155. Conduction losses of SiC and Si devices in single phase inverter circuit.

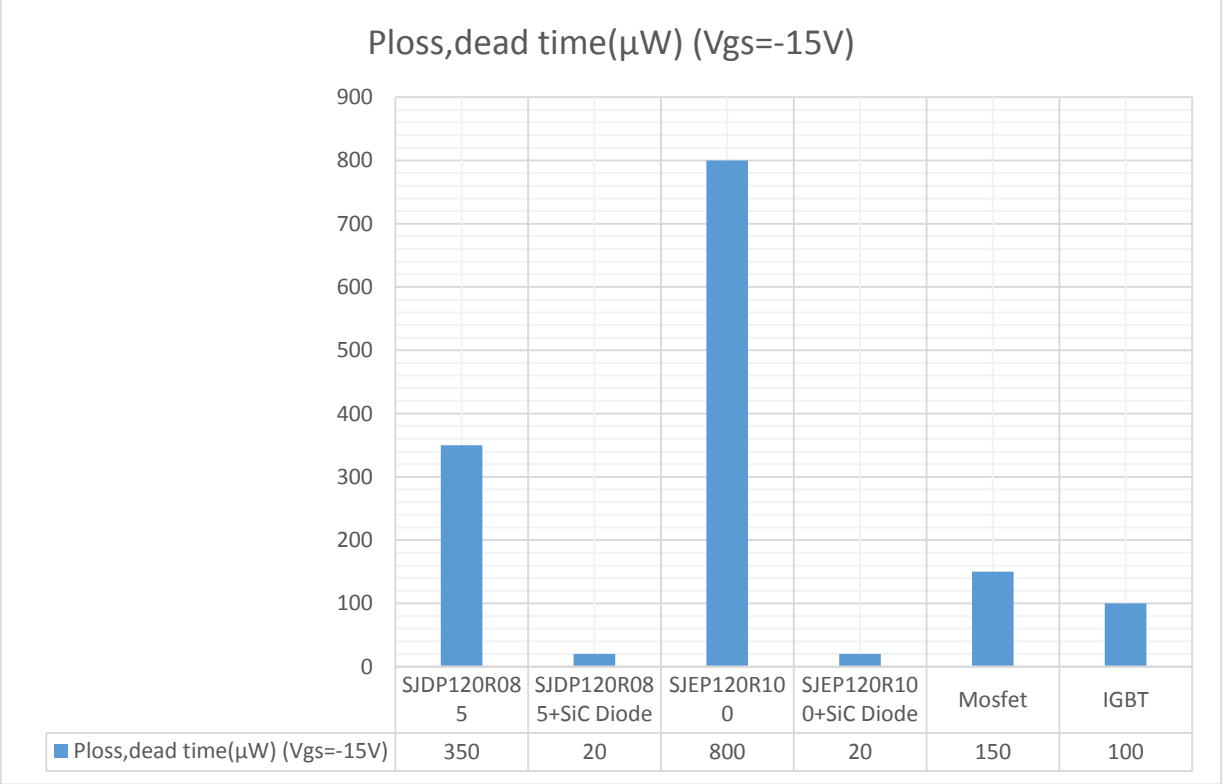
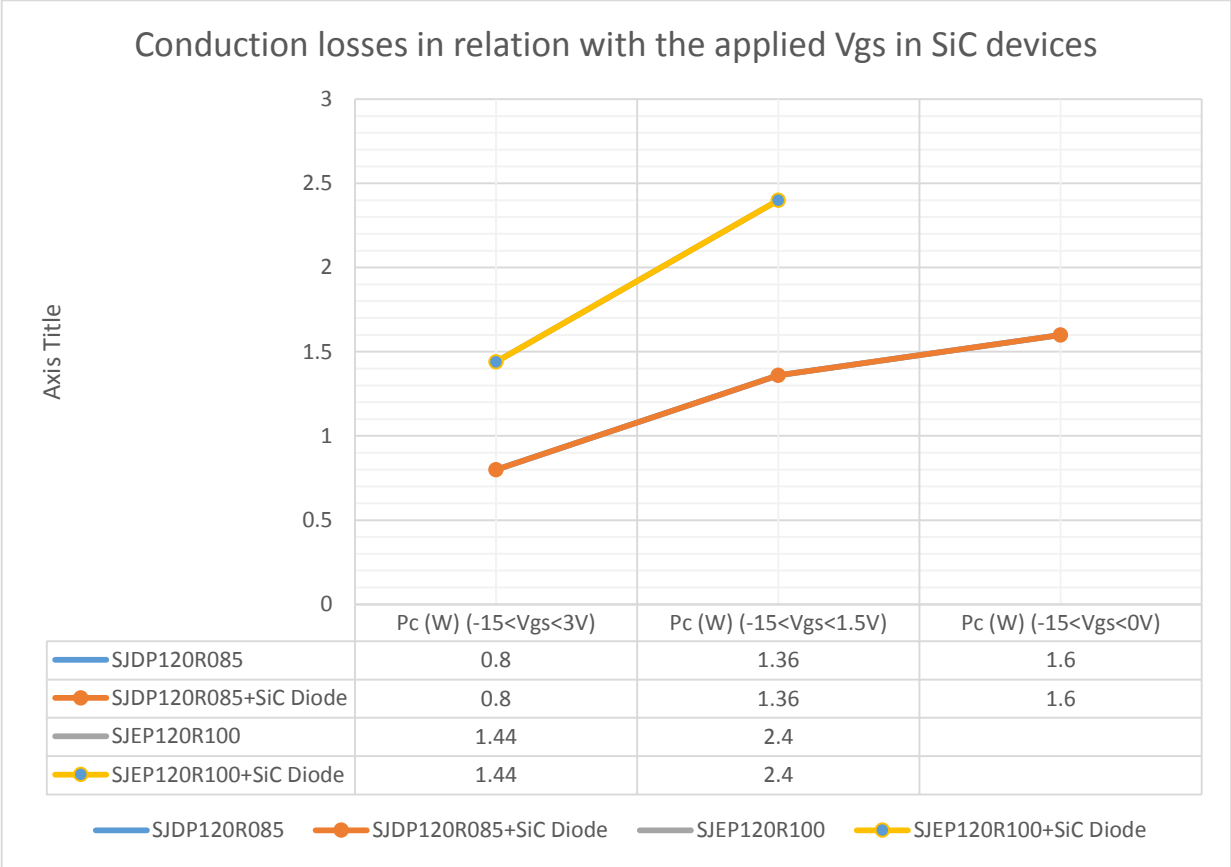


Figure 156. Power losses during dead time in Single Phase inverter circuits.

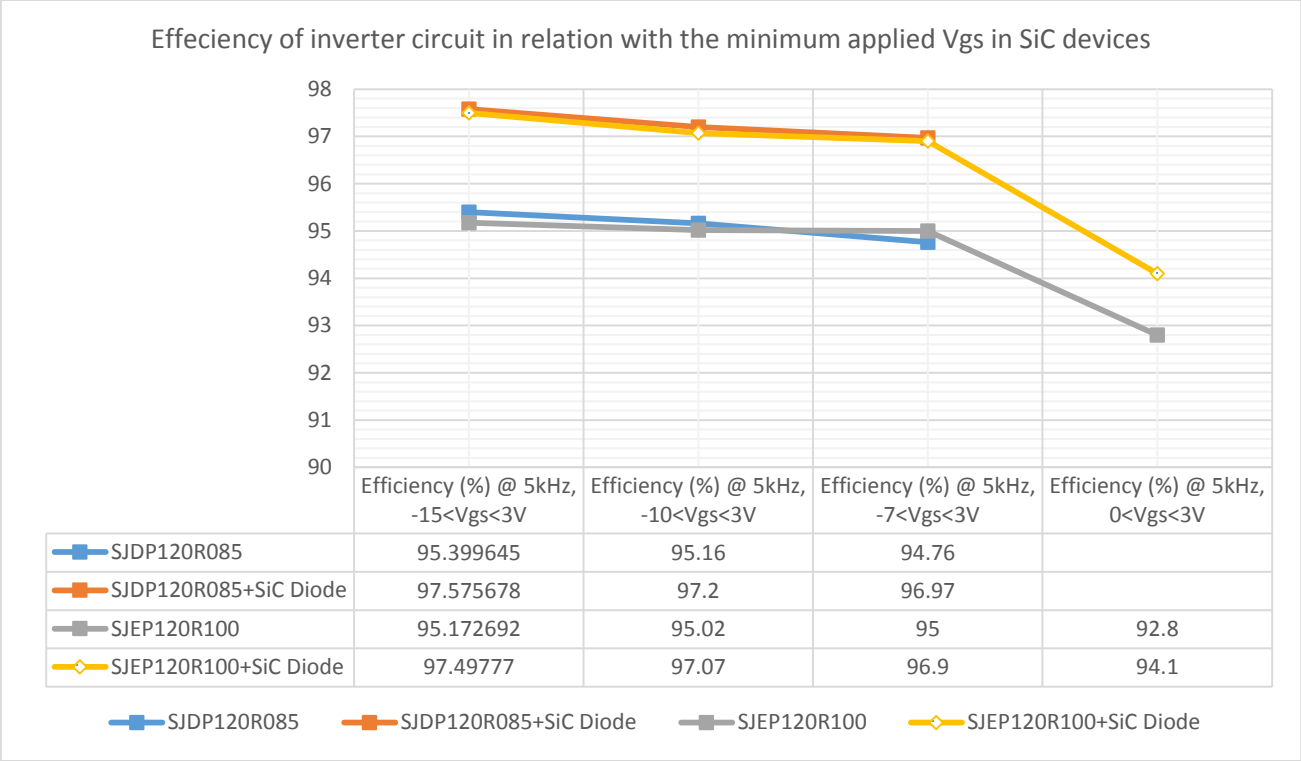
In *Figure 155*-*Figure 156* we show the detailed losses of all the devices used for the simulations. During forward conduction the on-state resistance for SiC is 0.085-0.100 Ω while for the Si Mosfet it is 0.650 and for Si IGBT there is a constant voltage drop 2V. That's why the SiC devices exhibit the less conduction losses.

For the reverse conduction losses which happen during interval 2 in *Figure 140* as we have explained previously, the SiC has more but they are acceptable as we have seen from the overall efficiency of the inverter in *Figure 151*. We note on this point that Si IGBT package contains an antiparallel diode and Si Mosfet is usually used with one as the body diode is not operational. That means that only the SiC devices can be used without freewheeling diodes and if we can sacrifice about 1% in the overall performance of one inverter with low power rating we gain in cost and size. In general, anti-paralleled diodes can be much smaller in size because they only conduct in a very short period during dead time.



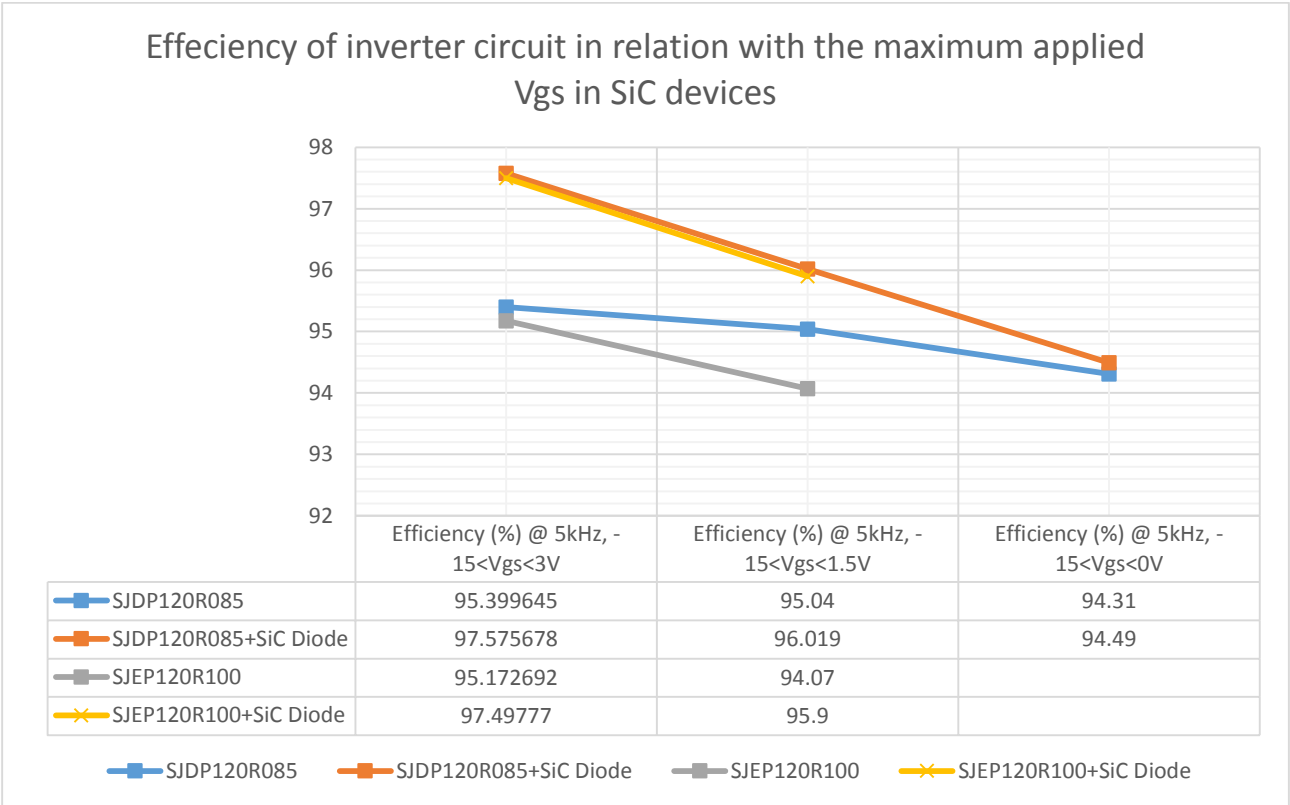
	Pc (W) (-15<Vgs<3V)	Pc (W) (-15<Vgs<1.5V)	Pc (W) (-15<Vgs<0V)
SJDP120R085	0.8	1.36	1.6
SJDP120R085+SiC Diode	0.8	1.36	1.6
SJEP120R100	1.44	2.4	
SJEP120R100+SiC Diode	1.44	2.4	

Figure 157. Conduction losses of SiC devices in function with gate voltage.



	Efficiency (%) @ 5kHz, -15<Vgs<3V	Efficiency (%) @ 5kHz, -10<Vgs<3V	Efficiency (%) @ 5kHz, -7<Vgs<3V	Efficiency (%) @ 5kHz, 0<Vgs<3V
SJDP120R085	95.399645	95.16	94.76	
SJDP120R085+SiC Diode	97.575678	97.2	96.97	
SJEP120R100	95.172692	95.02	95	92.8
SJEP120R100+SiC Diode	97.49777	97.07	96.9	94.1

Figure 158. Efficiency of SiC devices in function with gate voltage.



	Efficiency (%) @ 5kHz, -15<Vgs<3V	Efficiency (%) @ 5kHz, -15<Vgs<1.5V	Efficiency (%) @ 5kHz, -15<Vgs<0V
SJDP120R085	95.399645	95.04	94.31
SJDP120R085+SiC Diode	97.575678	96.019	94.49
SJEP120R100	95.172692	94.07	
SJEP120R100+SiC Diode	97.49777	95.9	

Figure 159. Efficiency of SiC devices in function with gate voltage.

Next we show the conduction losses in relation with the gate-source voltage in SiC devices. By increasing the forward bias we change the penetration of the depletion region in the channel. That means that the more the maximum applied gate-source voltage is the less losses we have. From *Figure 159* the improvement in the efficiency from increasing 1V V_{GS} is ~2%.

Although by changing the forward bias the efficiency may increase more than 2%, the results are different for the minimum applied gate voltage. As we can see in *Figure 159* the efficiency improves up to 1% by decreasing 7V the gate-source voltage. But as we are approaching the threshold voltage we don't improve a lot the efficiency as the blocking state losses are increasing because of the reduction in the blocking capability of the device.

5.3.3 Conclusions

The key advantages of SiC power switches like small switching energy loss and high operating junction temperatures over the conventional Si-IGBT are demonstrated with calculated results. The physical and electronic properties of SiC, when used as a power device, can lead to power devices that perform excellently at high power levels and high frequencies with increased efficiency, reduced inverter weight, size and cost. With a lower total power loss compared to the Si devices, the efficiency of SiC inverters is found to be 95% even at high frequency of 100 kHz. So it can be considered as the device of choice in high switching frequency applications where the losses in IGBT are prohibitive. At higher junction temperature, the advantage of the SiC JFET widens because of the stronger temperature dependence of the IGBT tail currents over temperature.

The switching frequency of more than 50 kHz is not possible for most of the high power Si power devices due to the extreme high power loss and demanding cooling requirements. With the low on-resistance and switching energies, these SiC switches can bring an enabling technology to not only increase the system efficiency, but reduce total system cost through reduced size and weight.

5.4 Construction of a Single-Phase Inverter

SiC power devices and modules are becoming popular and readily available commercially, from companies such as Semisouth, Cree, etc. According to the results in the previous section, there are several perceived advantages with these SiC over Si based devices such as reduced energy losses and high switching frequency, which assist to increase the efficiency and reduce the converter weight and size

The SiC JFET inverters have relatively high efficiency at all powers, switching frequency, and temperature ranges. Compared to Si inverters, the advantage is more obvious at high frequency and high temperature. With more development of SiC semiconductor technology, the efficiency of inverters based on future SiC products will be further improved and thus the cost will be lower.

This section describes the concept, the design, the construction, and experimental investigation of a 0.75 kW inverter with Depletion-Mode Silicon Carbide Junction Field Effect Transistors. The inverter was designed to have an efficiency 96%. Due to the low losses free convection cooling could be used. Since no fans are used the reliability can be increased compared to solutions with fans. A special gate-drive solution was applied forcing the transistors to switch very fast resulting in very low switching losses. As the output power is almost equal to the input power a special effort was done to precisely determine the amount of semiconductor power losses. A detailed analysis of the measurements shows that the efficiency of the inverter is approximately 96% at 0.75 kW.

In order to reach a high efficiency it is necessary to study on-state losses, switching losses, and driver losses and optimize them. Due to the remarkably low power losses (lower than 30 W), the need for cooling equipment is exceptionally low. A natural convection heat sink without a fan seems to be fully sufficient for this single-phase inverter. Thus, the reduced size of the cooling system is not the only benefit with the proposed design, but also the remarkably low levels of acoustic noise and the, potentially, increased reliability due to the elimination of the fan.

The main reasons for using DM SiC Jfet were:

- Low on-state resistance with the lowest dependence on temperature rise among different SiC JFET designs.
- Possibility to use the JFET as an anti-parallel diode when the current is negative (lower voltage drop than a Schottky diode).
- Less switching losses and therefore cooling demands than the EM SiC Jfet.

The experimental verification of the 0.75 kW SiC inverter was the following. The converter was loaded with an R = 47 Ω, L= 150 mH load and the input and output powers were measured with an advanced power meter while the power was increased in small steps. It was realized that accuracy of the electrical measurements was not sufficient in order to determine power losses in the range of 0.75 kW. But the accuracy of the predicted switching losses is not the most important aspect in the design process since the on-state losses are

expected to be the dominant loss contribution (~70%). With the switching speeds used, 5 kHz can actually be considered to be a comparably low switching frequency.

SPWM technique is used with carrier frequency 5kHz and fundamental output voltage frequency 50Hz. The gate driver is the one in Figure 8 with a range $-15 \leq V_{gs} \leq 3$. We note that in our application we could use V_{gs}=-10V but we didn't in order to reduce the blocking state losses.

Next we present the experimental plots of the inverter.

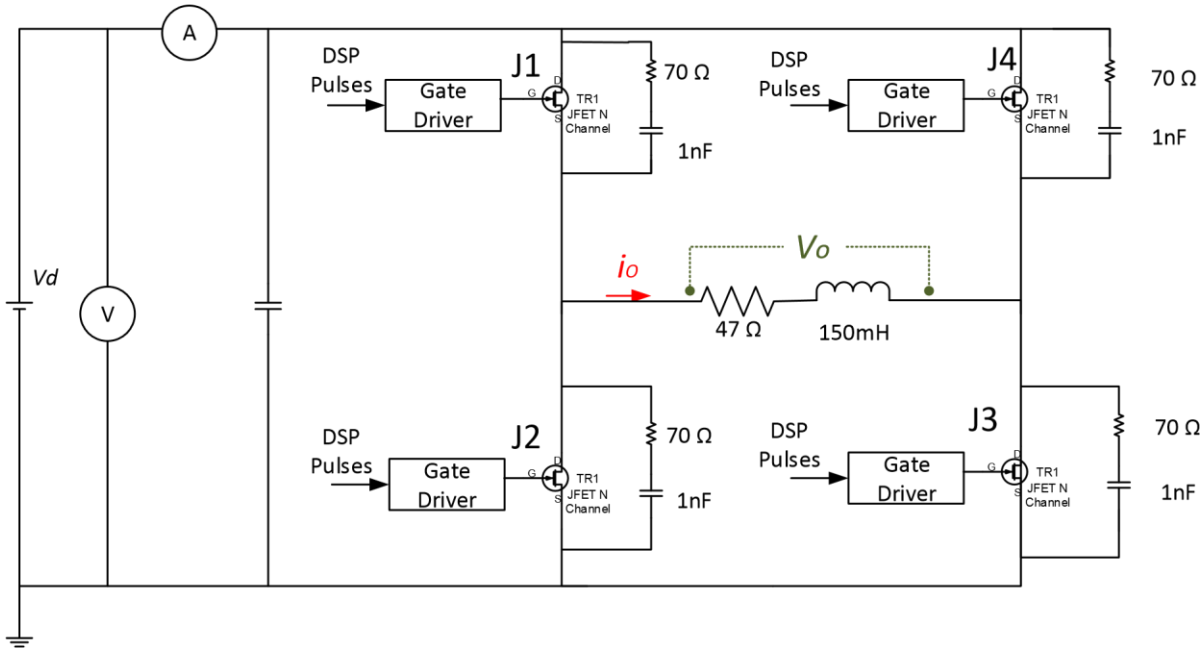


Figure 160. Schematic of the constructed inverter.

In the following figure we see the input and output waveforms from which we calculate the power and thus the efficiency.

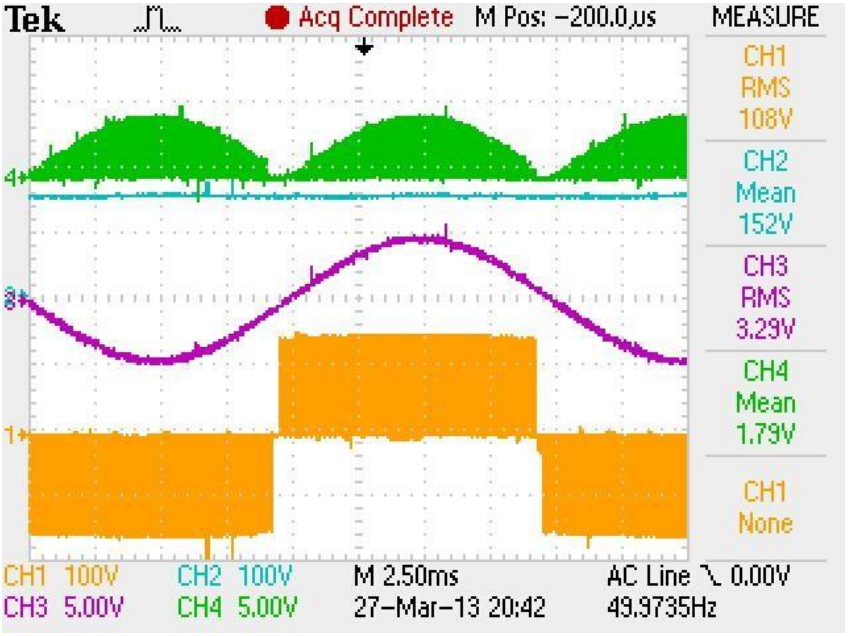


Figure 161. Input and output waveforms of the inverter. Green is the input current and blue the input voltage. Purple and orange is the output voltage and current respectively.

In *Figure 162* we see the input waveforms with a dc voltage 150V and input current 5A which means input power 750 W. In *Figure 163* the output voltage and current are shown.

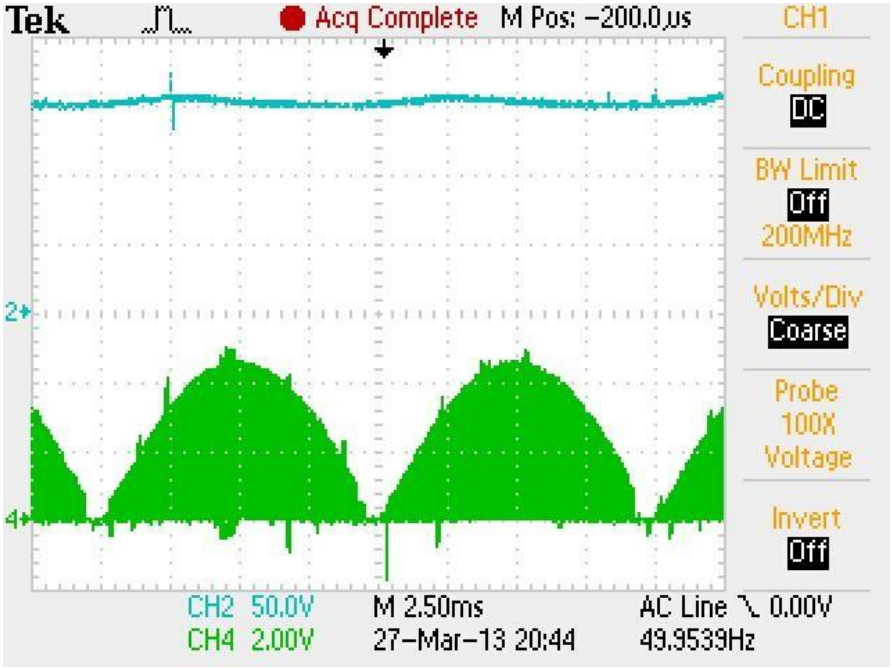


Figure 162. Input waveforms.

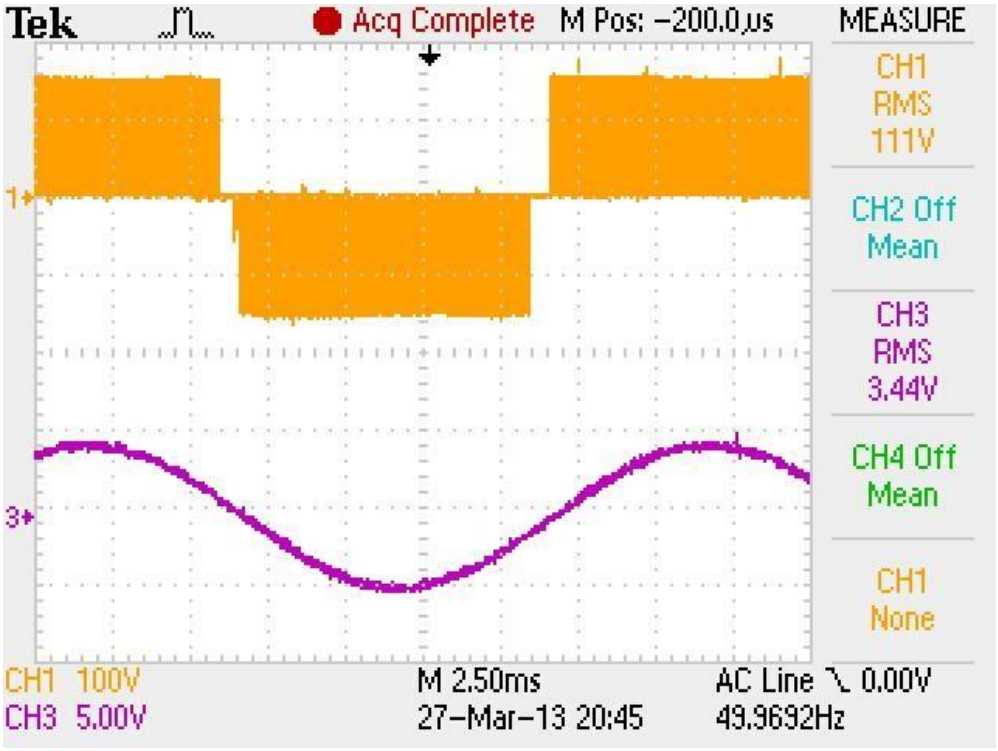


Figure 163. Output waveforms.

Special care has been given to avoid conditions like this below which is called Miller effect.

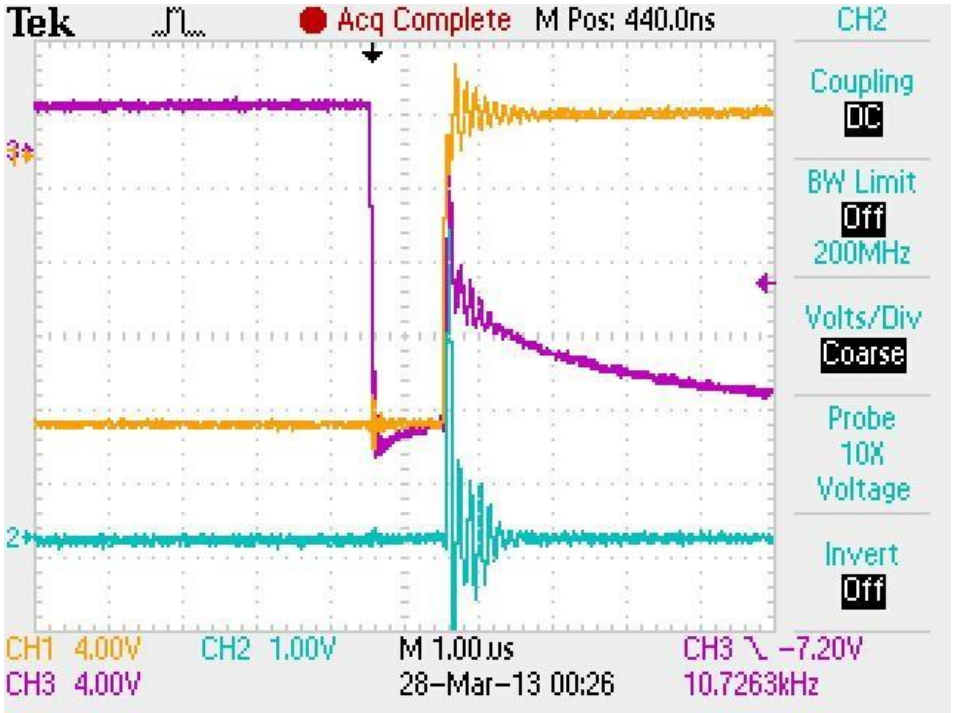


Figure 164. Miller effect in leg A. Gate pulse of J1(purple), pulse of J2(purple)

The pulses and the output waveforms for one semiconductor (J1) are shown below.

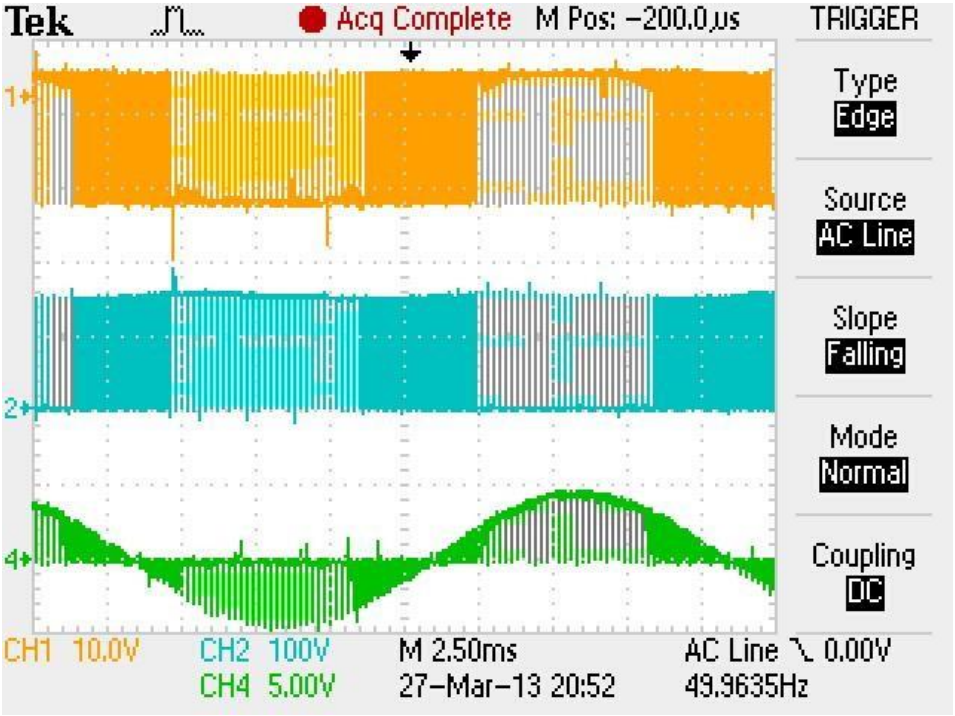


Figure 29. SPWM pulses, voltage and current in J1.

The turn-on time for J1 is shown below.

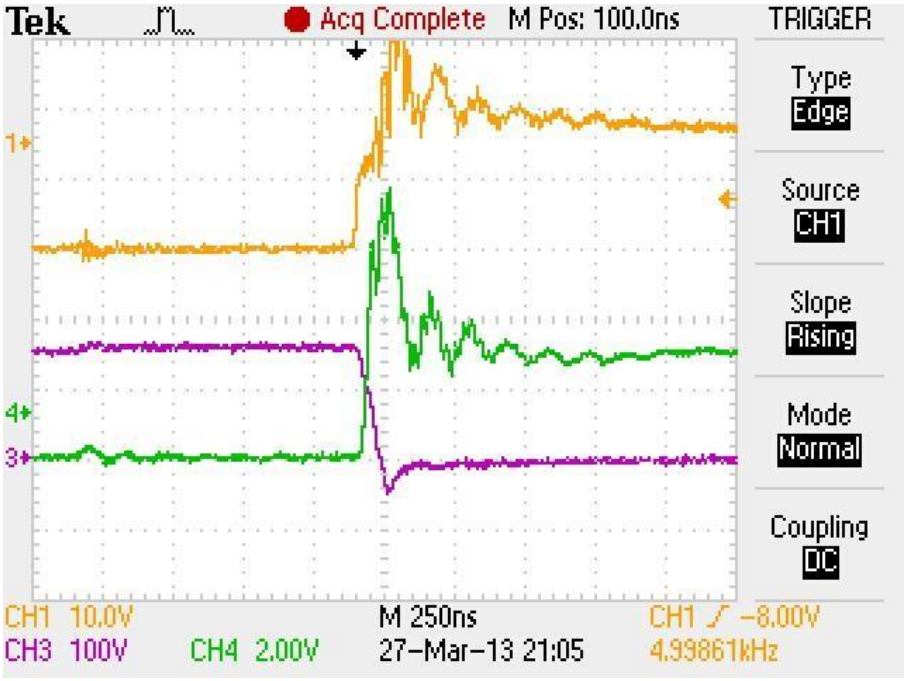


Figure 30. Gate pulse of J1 (green), J3 (yellow), and voltage at J1(purple)

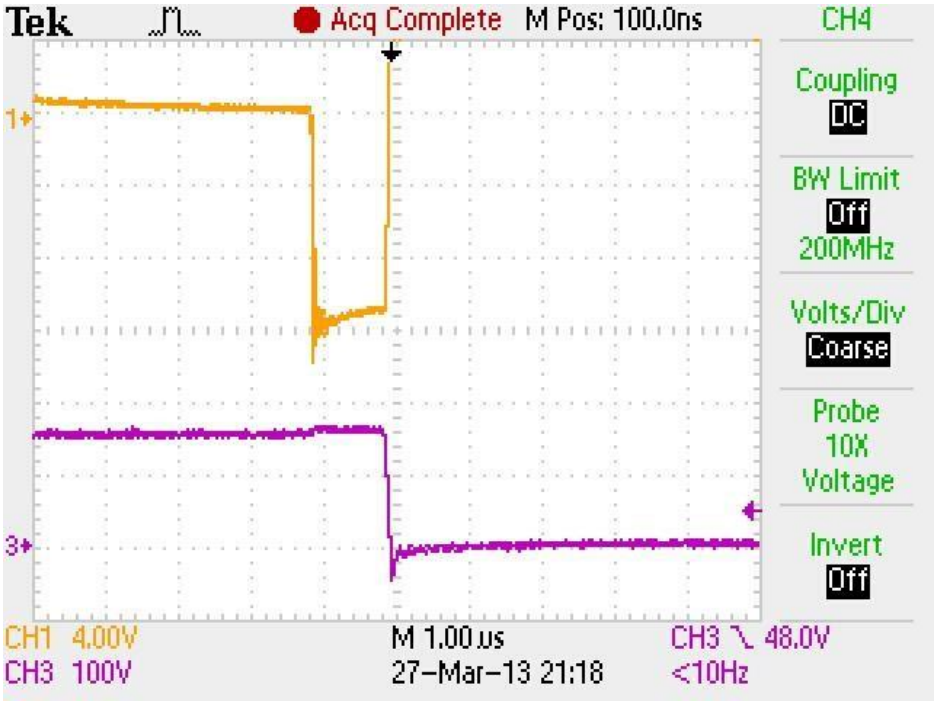


Figure 31. Voltage drop of J1 (yellow) during dead time and voltage at J2(purple).

In this section the construction method of a single phase SiC inverter was shown. The efficiency was measured 96% which is according to the simulations (~95.4%). It can be further improved by placing an output filter for the voltage and current harmonics. The key to reach in much higher efficiencies is a combination of parallel connection of SiC JFETs, using the JFET also as an anti-parallel diode, and a high switching speed [25]. The addition of a freewheeling diode was redundant for this power level. Consequently, a certain amount of the cost increase imposed by the, potentially costly, SiC devices can be reduced at the same time as the complexity is reduced and the availability can be increased.

Investigation was made partly as analytical considerations based on theory and simulations, especially the loss and efficiency estimations, and partly experimentally on an existing SiC inverter. Further work can be directed to inverter efficiency evaluation under high temperature.

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