ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ

ΣΧΟΛΗ ΗΛΕΚΤΡΟΛΟΓΩΝ ΜΗΧΑΝΙΚΩΝ και ΜΗΧΑΝΙΚΩΝ ΥΠΟΛΟΓΙΣΤΩΝ

ΤΟΜΕΑΣ ΕΠΙΚΟΙΝΩΝΙΩΝ, ΗΛΕΚΤΡΟΝΙΚΗΣ και ΣΥΣΤΗΜΑΤΩΝ ΠΛΗΡΟΦΟΡΙΚΗΣ

Σχεδίαση και Υλοποίηση Ολοκληρωμένου Ενεργού Μίκτη στη D Ζώνη Συχνοτήτων σε Τεχνολογία BiCMOS 0,13μm

ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

της

ΦΙΛΙΠΠΑΣ ΣΟΥΜΠΑΣΑΚΟΥ

Επιβλέπων: Ιωάννης Παπανάνος

Καθηγητής Ε.Μ.Π.

ΕΡΓΑΣΤΗΡΙΟ ΗΛΕΚΤΡΟΝΙΚΗΣ

Αθήνα, Σεπτέμβριος 2022

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Εγκρίθηκε από την τριμελή εξεταστική επιτροπή την /2022.

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Σουμπασάκου Φιλίππα
Διπλωματούχος Ηλεκτρολόγος Μηχανικός
και Μηχανικός Υπολογιστών Ε.Μ.Π.

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Απαγορεύεται η αντιγραφή, αποθήκευση και διανομή της παρούσας εργασίας, εξ ολοκλήρου ή τμήματος αυτής, για εμπορικό σκοπό. Επιτρέπεται η ανατύπωση, αποθήκευση και διανομή για σκοπό μη κερδοσκοπικό, εκπαιδευτικής ή ερευνητικής φύσης, υπό την προϋπόθεση να αναφέρεται η πηγή προέλευσης και να διατηρείται το παρόν μήνυμα. Ερωτήματα που αφορούν τη χρήση της εργασίας για κερδοσκοπικό σκοπό πρέπει να απευθύνονται προς τον συγγραφέα.

Οι απόψεις και τα συμπεράσματα που περιέχονται σε αυτό το έγγραφο εκφράζουν τον συγγραφέα και δεν πρέπει να ερμηνευθεί ότι αντιπροσωπεύουν τις επίσημες θέσεις του Εθνικού Μετσόβιου Πολυτεχνείου.

Περίληψη

Αντικείμενο της παρούσας διπλωματικής εργασίας αποτελεί η σχεδίαση και η υλοποίηση ενός ολοκληρωμένου, up-converting και down-converting, διπλά εξισορροπημένου, ενεργού μίκτη, συνδεσμολογίας gilbert cell, σε τεχνολογία SiGe BiCMOS 0.13μm, με λειτουργία στην D ζώνη του φάσματος των ραδιοσυχνοτήτων, με κεντρική συχνότητα στα 145GHz. Η εργασία αυτή αποτέλεσε μέρος ενός ομαδικού project και, πιο συγκεκριμένα, της σχεδίασης και υλοποίησης ενός πομποδέκτη, τεχνολογίας 6G (130GHz έως 170GHz), ενσύρματης επικοινωνίας μικρού-μέτριου μήκος χρησιμοποιώντας πλαστικούς κυματοδηγούς (PMF). Εφαρμογές της ομαδικής εργασίας αφορούν σύγχρονα και μελλοντικά προϊόντα της τεχνολογίας 6G.

Στα ακόλουθα κεφάλαια γίνεται θεωρητική ανάλυση των τηλεπικοινωνιακών αλυσίδων, των κατηγοριών των μικτών και των χαρακτηριστικών τους. Ακολουθεί παρουσίαση της τεχνολογίας που επελέχθη, της αρχιτεκτονικής και της μεθοδολογίας που ακολουθήθηκε και των αποτελεσμάτων των προσομοιώσεων των ανωτέρω. Έπειτα, ακολουθεί η σχεδίαση του κυκλώματος σε φυσικό επίπεδο (layout), όπου με κατάλληλες ηλεκτρομαγνητικές προσομοιώσεις, εξάγονται τα τελικά αποτελέσματα προσμοιώσεων.

Η εστίαση των επιδόσεων του design έγινε στη γραμμικότητα, στο κέρδος μετατροπής, και την ευρυζωνικότητα, επιτυγχάνοντας, συνολικά, τα απαιτούμενα μεγέθη.

Λέξεις- Κλειδιά: Ενεργός Μίκτης, 145GHz, BiCMOS, conversion gain , gilbert cell, up-converter, down-converter

Abstract

The subject of this thesis is the design and implementation of an integrated, up-converting and down-converting, double balanced, active mixer, in gilbert cell topology, in SiGe BiCMOS 0.13μm technology, operating in the D band of the radio frequency spectrum, with a center frequency of 145GHz. This work was part of a team project and, more specifically, the design and implementation of a transceiver, 6G technology (130GHz to 170GHz), a short-medium range datalink using Polymer Microwave Fibers (PMF). Applications of the group project concern current and future 6G technology products.

The following chapters provide a theoretical analysis of telecommunication chains, mixer classifications and their characteristics. This is followed by a presentation of the technology chosen, the architecture and methodology followed and the results of the simulations of the above. Then, the circuit design in physical plane (layout) follows, where with appropriate electromagnetic simulations, the final simulation results are extracted.

The focus of the design performance was on linearity, conversion gain, and the frequency range, achieving, overall, the required quantities.

Key words: Active Mixer, 145GHz, BiCMOS, conversion gain , gilbert cell, up-converter, down-converter

Ευχαριστίες

Θα ήθελα, αρχικά, να ευχαριστήσω τον καθηγητή μου Ιωάννη Παπανάνο για την εμπιστοσύνη που μου έδειξε αναθέτοντάς μου το θέμα της διπλωματικής μου εργασίας και της καθοδήγησης που μου προσέφερε για την ολοκλήρωσή της. Επίσης, τον ευχαριστώ για την ευκαιρία που μου προσέφερε να βρεθώ στο επαγγελματικό περιβάλλον της εταιρείας Infineon Technologies AG, στο πλαίσιο της διπλωματικής μου εργασίας, στην οποία απέκτησα πολύτιμες γνώσεις και εμπειρίες και γνώρισα καλούς φίλους, αλλά και για τις συμβουλές και τη βοήθειά του για τη μετέπειτα επαγγελματική μου ζωή. Ευχαριστώ, επίσης, τον Franz Dielacher που μου έδωσε την ευκαιρία να εργαστώ στην ομάδα του και τον Siegfried Krainer για την ομαλή συνεργασία και την καθοδήγηση.

Μία μεγάλη ευχαριστία οφείλω στο φίλο και συνεργάτη Βασίλειο Μανουρά, υποψήφιο διδάκτορα του καθηγητή Ιωάννη Παπανάνου, για την καθοριστική συμβολή και βοήθεια στην διπλωματική μου εργασία, την υποστήριξη στις προκλήσεις που προέκυψαν και τις γνώσεις που μου προσέφερε. Έπειτα, θα ήθελα να ευχαριστήσω τους συνεργάτες και φίλους Βασίλειο Λιακόνη, υποψήφιο διδάκτορα του καθηγητή Ιωάννη Παπανάνου, και Παντελεήμων Γαβαλά, για τη συνεργασία και τη βοήθειά τους καθ'ολη τη διάρκεια της διπλωματικής και των σπουδών μου.

Στη συνέχεια, ευχαριστώ θερμά όλους τους φίλους μου, τους παλιούς αλλά και τους νέους, για τη διαρκή υποστήριξη, τις συμβουλές και τις ευχάριστες στιγμές. Ειδικά, μεγάλο ευχαριστώ οφείλω στη φίλη μου Κωνσταντίνα Στεργίου και στο φίλο μου Απόστολο Βελάνη.

Τέλος, το μεγαλύτερο ευχαριστώ οφείλω στους γονείς μου, Ιωάννη και Αικατερίνη, και τις αδελφές μου Βασιλική και Αρτεμησία, για ό,τι μου έχουν προσφέρει ανιδιοτελώς και όσα συνεχίζουν να μου προσφέρουν καθημερινά. Ειδικά, τον πατέρα μου και την αδελφή μου Αρτεμησία θα ήθελα να τους ευχαριστήσω ξεχωριστά και ως συναδέλφους, για την καθοδήγηση και τις συμβουλές.

Εκτεταμένη Περίληψη

Με τα πρώτα βήματα της τεχνολογίας 5G, έχουν ήδη διαμορφωθεί νέες ιδέες και καινοτόμα σχέδια για την τεχνολογία 6G. Το 6G θα εισάγει τη νέα κοινωνία επικοινωνιών του 2030 παρέχοντας πρόσθετες δυνατότητες και τεχνολογίες για την εξυπηρέτηση των χρηστών [1]. Παγκοσμίως, οι οργανισμοί διερευνούν τον καινοτόμο τομέα των THz τεχνολογιών, αναμένοντας τα επόμενα χρόνια να έχουν απεριόριστη και πλήρη ασύρματη επικοινωνία, για εφαρμογές ραντάρ, πλοήγησης, εντοπισμού θέσης, ανίχνευσης, επικοινωνιών κ.λπ. [2], [3]. Οι απαιτήσεις, επομένως, για τα νέα δίκτυα 6G αφορούν τη διαχείριση του φάσματος και της ισχύος, τον μέγιστο ρυθμό δεδομένων, την καθυστέρηση, τη χωρητικότητα και την κινητικότητα. Πιο συγκεκριμένα, ο μέγιστος ρυθμός δεδομένων αναμένεται να υπερβαίνει το 1 Tb/s, δηλαδή 100 φορές υψηλότερος από το 5G, ο ρυθμός δεδομένων που βιώνει ο χρήστης 1Gb/s, δηλαδή 10 φορές υψηλότερος από το 5G, η καθυστέρηση 10-100 μs, η πυκνότητα δικτύου 10 φορές υψηλότερη από το 5G, η ενεργειακή απόδοση 10-100 και η αποδοτικότητα φάσματος 5-10 φορές υψηλότερη από το 5G [4].

Ορισμένα πλεονεκτήματα της νέας ζώνης συχνοτήτων είναι το γεγονός ότι δεν υπάρχει "φασματική συμφόρηση" και, επιπλέον, η κλίμακα σχεδίασης είναι πολύ μικρότερη. Το μέγεθος της κεραίας εξαρτάται από το μήκος κύματος του σήματος, επομένως, ο χώρος που καταλαμβάνει μειώνεται σημαντικά και τα αναλογικά και ψηφιακά κυκλώματα γίνονται επίσης πολύ μικρότερα, όπως υποδηλώνει η τεχνολογία των 130 nm που χρησιμοποιήθηκε για την παρούσα διατριβή. Η παρούσα διατριβή ασχολείται με τη σχεδίαση και την υλοποίηση ενός ολοκληρωμένου τετραγωνικού διαμορφωτή I/Q D-Band, ενός από τα πιο κρίσιμα blocks στους σύγχρονους πομπούς mm-wave και sub-THz [5]. Υλοποιήσεις τέτοιων διαμορφωτών I/Q D-Band περιλαμβάνονται σε αρκετές πρόσφατες εφαρμογές 6G και πέραν του 5G [6], [7], [8].

Τηλεπικοινωνιακή Αλυσίδα

Τόσο στις ψηφιακές όσο και στις αναλογικές επικοινωνίες, το σύστημα επικοινωνίας περιλαμβάνει το σύστημα πομπού και το σύστημα δέκτη μεταξύ των οποίων παρεμβάλλεται το κανάλι μετάδοσης. Η διαφορά μεταξύ των αναλογικών και των ψηφιακών συστημάτων έγκειται στη μορφή του μεταδιδόμενου σήματος, στην επεξεργασία του σήματος και στους στόχους απόδοσης.

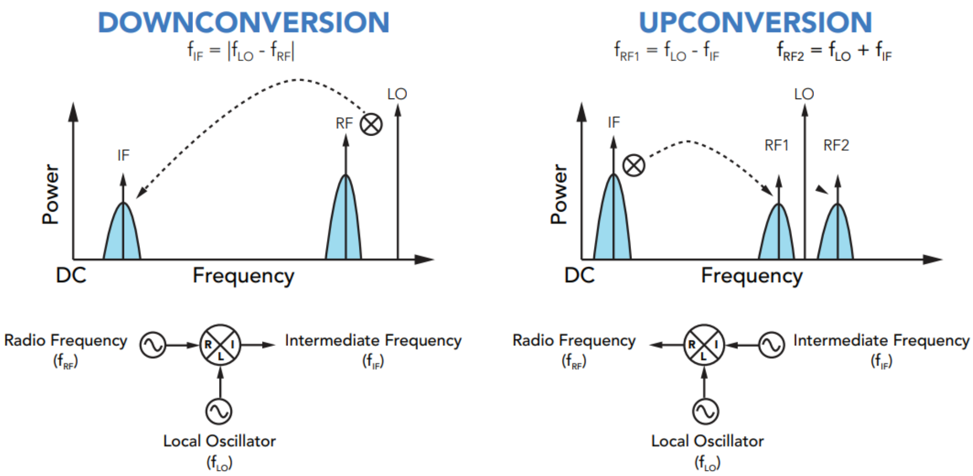
Γενικότερα, ο πομπός εκτελεί επεξεργασία βασικής ζώνης, διαμόρφωση, ενίσχυση και φιλτράρισμα για την αποφυγή διαρροής σε γειτονικά κανάλια. Από την άλλη πλευρά, ο δέκτης εκτελεί φιλτράρισμα, αποδιαμόρφωση και ενίσχυση, ενώ κυρίως, επεξεργάζεται το επιλεγμένο κανάλι απορρίπτοντας, επαρκώς, ισχυρές γειτονικές παρεμβολές.

Ο μίκτης

Ο μίκτης είναι ένα από τα πιο κρίσιμα blocks στους σύγχρονους πομποδέκτες κυμάτων mm και υπο-THz [5]. Η θέση του στην αλυσίδα του πομποδέκτη απεικονίζεται παραπάνω. Αναλυτικότερα, στον πομπό, ο μίκτης βρίσκεται συνήθως πριν από τον ενισχυτή ισχύος (PA), όπου ο ρόλος του είναι να μεταφέρει το επιθυμητό σήμα σε υψηλότερες συχνότητες πριν από την ενίσχυση και την τελική μεταφορά του μέσω του καναλιού. Στο δέκτη, ο μίκτης τοποθετείται συχνά μετά τον ενισχυτή χαμηλού θορύβου (LNA) και στόχος του είναι η μεταφορά του λαμβανόμενου σήματος σε χαμηλότερες συχνότητες πριν αυτό σταλεί προς επεξεργασία από τη συσκευή.

Ένας μίκτης συχνοτήτων είναι ένα ηλεκτρονικό κύκλωμα τριών θυρών, στο οποίο ορίζονται οι θύρες εισόδου και η θύρα εξόδου. Ο ιδανικός μίκτης μετατροπής προς τα πάνω έχει δύο θύρες εισόδου, αυτές της φέρουσας συχνότητας, που συνήθως παρέχονται από έναν τοπικό ταλαντωτή (LO), και της ενδιάμεσης συχνότητας (IF) και μία θύρα εξόδου ραδιοσυχνότητας (RF). Στην περίπτωση του μίκτη μετατροπέα προς τα κάτω, οι θύρες IF και RF αντιστρέφονται και, επομένως, η θύρα RF είναι θύρα εισόδου και η θύρα IF θύρα εξόδου.

Με τον όρο μίξη RF εννοούμε τον πολλαπλασιασμό δύο σημάτων για τη δημιουργία νέων σημάτων, σε νέες συχνότητες, παράγωγα των συχνοτήτων των αρχικών σημάτων. Γενικότερα, όταν δύο σήματα, fin1 και fin2, διέρχονται από ένα μη γραμμικό κύκλωμα, τότε στην έξοδο του κυκλώματος δημιουργούνται πρόσθετα σήματα στο άθροισμα και στη διαφορά των δύο αρχικών συχνοτήτων (fin1+fin2) και (fin1-fin2) αντίστοιχα. Τέτοια μη γραμμικά στοιχεία σε ένα κύκλωμα, που δρουν ως πολλαπλασιαστές, μπορεί να είναι μια δίοδος και ενεργά στοιχεία, όπως τα BJTs και HBTs, τα οποία βασίζονται στις εκθετικές I-V χαρακτηριστικές της pn ένωση ή τα MOSFETs ή τα HEMTs, που ακολουθούν τη συμπεριφορά τετραγωνικού νόμου σε χαμηλές πραγματικές τάσεις πύλης, αλλά σε κόμβους νανοκλίμακας συμπεριφέρονται γραμμικά.



Σχήμα 1: Ορισμοί της μετατροπής προς τα κάτω και της μετατροπής προς τα πάνω.

Η επιλογή των θυρών IF ή RF για σήμα εισόδου εξαρτάται από την εφαρμογή του μίκτη. Όταν η επιθυμητή συχνότητα εξόδου είναι χαμηλότερη από τη συχνότητα εισόδου, τότε έχουμε μετατροπή προς τα κάτω και η θύρα RF είναι θύρα εισόδου και η θύρα IF είναι θύρα εξόδου. Σε αυτή την περίπτωση, η εξίσωση (1) που περιγράφει τη λειτουργία του μίκτη, στο πεδίο του φάσματος, είναι η ακόλουθη:

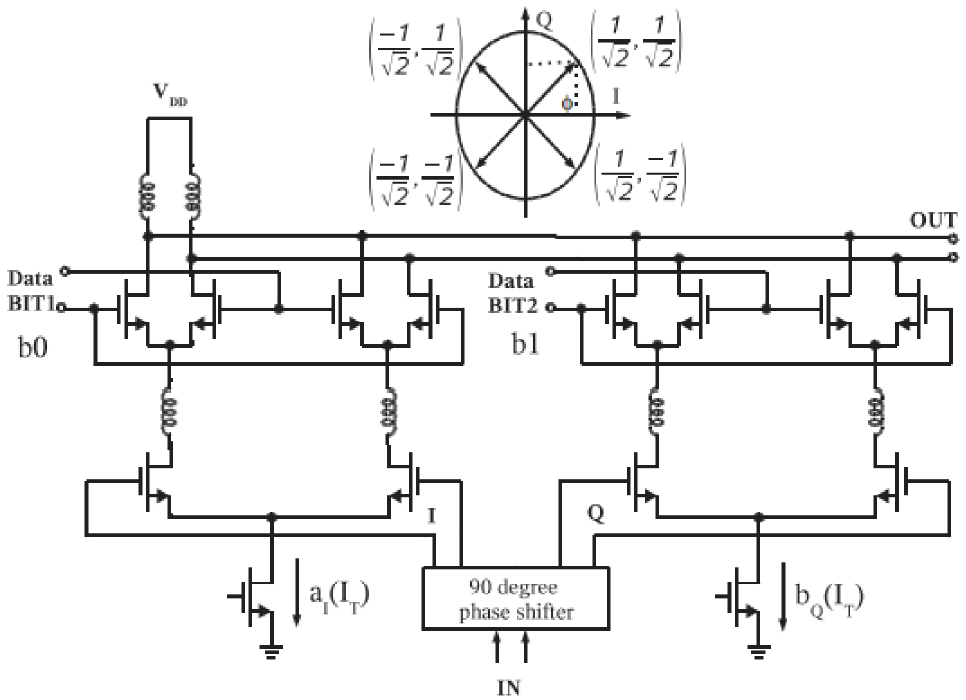
fIF = |fLO - fRF| (1)

Στην αντίθετη περίπτωση, όταν η επιθυμητή συχνότητα εξόδου είναι υψηλότερη από τη συχνότητα εισόδου, τότε η διαδικασία ονομάζεται μετατροπή προς τα πάνω και η IF είναι η θύρα εισόδου, ενώ η RF είναι η θύρα εξόδου, οπότε ισχύει η ακόλουθη εξίσωση (2):

fRF = fLO ± fIF (2)

Η αθροιστική συχνότητα fRF = fLO + fIF είναι γνωστή ως άνω πλευρική ζώνη (USB) και η διαφορά fRF = fLO - fIF ονομάζεται κάτω πλευρική ζώνη (LSB).

Οι διαμορφωτές (modulators) μπορούν να συνθέσουν κυκλώματα, για παράδειγμα τοπολογίες Gilbert, για να παράγουν αντίγραφα I και Q του φέροντος σήματος (quadrature modulation) [5]. Χρησιμοποιούν υβρίδια 90 μοιρών του σήματος και στις δύο διαφορικές θύρες εισόδου και ανάλογα με την επιθυμητή πλευρική ζώνη, τίθεται το πρόσημο. Στο σχήμα 2, παρουσιάζεται ένα παράδειγμα διαμορφωτή, βασισμένο σε τοπολογία Gilbert.



Σχήμα 2: Σχηματική αναπαράσταση CMOS ενός διαμορφωτή QPSK κύματος mm που βασίζεται σεquadrature modulation και Gilbert cells.

Σε αντίθεση με τους μίκτες, τα μειονεκτήματά τους είναι ότι καταλαμβάνουν μεγαλύτερη επιφάνεια στο chip και ότι απαιτούν μεγαλύτερη ισχύ, αλλά, ένα κύριο πλεονέκτημα είναι η απόρριψη εικόνας (image rejection) που μπορεί να επιτευχθεί.

Δίκτυα προσαρμογής [14]

Σε αντίθεση με τις χαμηλές συχνότητες όπου το μήκος κύματος του σήματος υπερβαίνει το ένα μέτρο, στις υψηλές συχνότητες η ηλεκτρική απόσταση μεταξύ των ακροδεκτών του κυκλώματος και των εξωτερικών ακροδεκτών γίνεται συγκρίσιμη με το μήκος κύματος του σήματος. Οι αναντιστοιχίες σύνθετης αντίστασης σε κάθε πλευρά προκαλούν ανακλάσεις που μπορούν να μειώσουν σημαντικά την ισχύ του σήματος που φτάνει στο κύκλωμα προορισμού. Η τυπική τιμή σύνθετης αντίστασης που επιβάλλεται από τον τυποποιημένο εξοπλισμό δοκιμών είναι 50Ω.

Επιπλέον, προκειμένου να εξασφαλιστεί η μέγιστη δυνατή μεταφορά ισχύος μεταξύ της πηγής σήματος και ενός κυκλώματος, η αντίσταση εισόδου του ενισχυτή, ZIN, πρέπει να ταιριάζει με εκείνη της πηγής σήματος, ZS, και, πιο συγκεκριμένα, πρέπει να ακολουθεί την εξίσωση Zin = ZS* (συζυγής προσαρμογή). Το ίδιο ισχύει και για τη μέγιστη μεταφορά ισχύος από το κύκλωμα στο φορτίο του. Η σύνθετη αντίσταση εξόδου του κυκλώματος, ZOUT, πρέπει να προσαρμόζεται στην αντίσταση φορτίου, ZL. Επομένως, πρέπει να εισαχθούν τα αντίστοιχα δίκτυα προσαρμογής μεταξύ του κυκλώματος και της πηγής σήματος και μεταξύ του ενισχυτή και του φορτίου.

Συχνά, σε εφαρμογές υψηλών συχνοτήτων, οι ZS και ZL είναι ίσες με μια πραγματική αντίσταση Z0.

Η επίδοση ενός μίκτη καθορίζεται από πολλές παραμέτρους. Αυτές οι παράμετροι επίδοσης περιγράφουν συνοπτικά την ποιότητα και τις δυνατότητες λειτουργίας του μίκτη. Οι σημαντικότερες παράμετροι είναι οι παρακάτω:

1. Προσαρμογή (Matching) στις θύρες RF, LO και IF

2. Κέρδος Μετατροπής (Conversion Gain, CG)

3. Εικόνα Θορύβου (Noise Figure, NF)

4. Γραμμικότητα (Linearity)

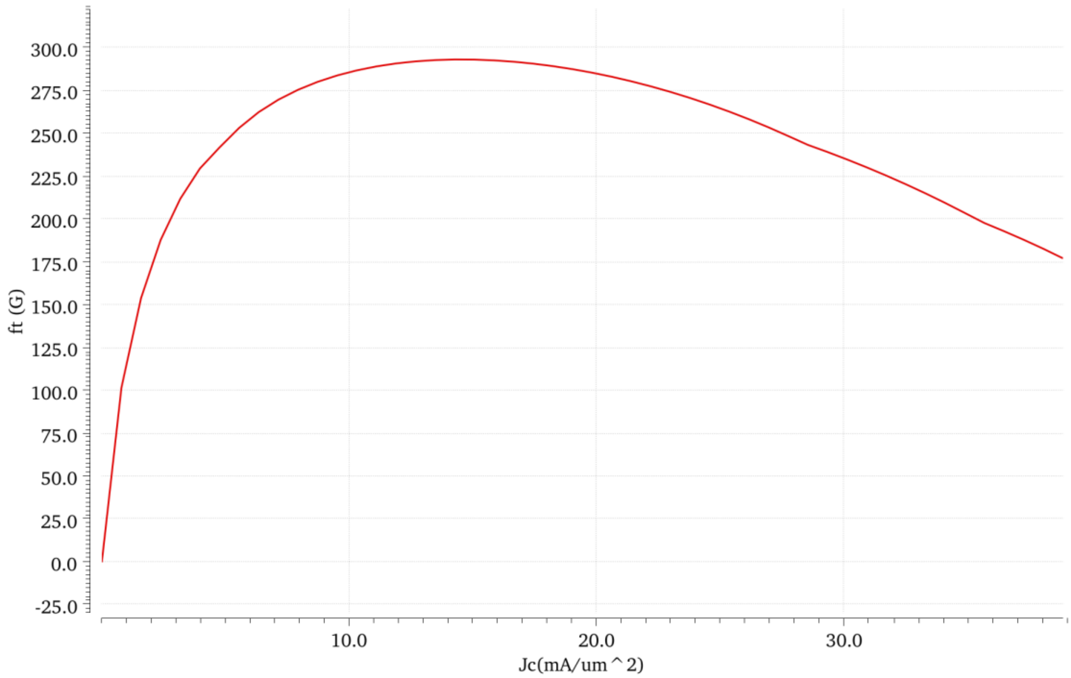
i. Σημείο Συμπίεσης 1-dB (1-dB Compression Point)

ii. Παραμόρφωση Ενδοδιαμόρφωσης και Σημείο Παρεμβολής 3ης τάξης (Third Order Intercept Point, IP3)

5. Απομόνωση μεταξύ Θυρών (Port-to-Port Isolation)

7. Ευστάθεια

Για το σωστό σχεδιασμό είναι σκόπιμο να έχουμε στη διάθεσή μας μια εκτίμηση της πυκνότητας ρεύματος, για τη βέλτιστη ταχύτητα της συσκευής. Το σχήμα 3 δείχνει ότι, το υψηλότερο κέρδος μοναδιαίας συχνότητας (συχνότητα διέλευσης) fT~280 GHz επιτυγχάνεται όταν ο συλλέκτης του τρανζίστορ διαρρέεται από πυκνότητα ρεύματος περίπου 14 mA/μm2.



Σχήμα 3: Διάγραμμα της συχνότητας fT σε σχέση με το ρεύμα συλλέκτη για ένα HBT υψηλής ταχύτητας, επιφάνειας 0,22 x 10um^2.

Η σχεδίαση πραγματοποιήθηκε στο περιβάλλον Virtuoso® της Cadence®, ενώ η τεχνολογία κατασκευής του μίκτη, είναι η B11HFC της Infineon Technologies. Επιχειρείται η παρουσίαση των προδιαγραφών της εν λόγω σχεδίασης, η ροή της σχεδίασης και η ανάλυση των τεχνικών εμποδίων που συναντήθηκαν κατά τη διάρκεια της διαδικασίας σύνθεσης του μίκτη.

Η ροή σχεδιασμού περιλαμβάνει τα ακόλουθα βασικά σημεία:

1. Καθορισμός των προδιαγραφών για την απόδοση του ενισχυτή.

2. Επιλογή των τρανζίστορ που χαρακτηρίζουν την ενεργό διάταξη του μίκτη, με βάση τα μοντέλα τρανζίστορ της τεχνολογίας.

3. Σχεδιασμός του κυκλώματος μίξης με ιδανικά παθητικά στοιχεία της βιβλιοθήκης αναλογικών lib και ενεργά HBT της τεχνολογίας.

4. Αντικατάσταση των ιδανικών παθητικών στοιχείων με πραγματικά μοντέλα της τεχνολογίας, σχεδιασμός κυκλωμάτων εισόδου και εξόδου και εξαγωγή αποτελεσμάτων γραφικής προσομοίωσης (Cadence Virtuoso® Spectre®).

5. Σχεδιασμός διάταξης, εξαγωγή παρασιτικών αντιστάσεων, αυτεπαγωγών, χωρητικοτήτων και αμοιβαίων αυτεπαγωγών σε επιλεγμένα τμήματα (εξαγωγή RLCK)

και προσομοίωση της διάταξης στο πρόγραμμα ηλεκτρομαγνητικής προσομοίωσης ADS Momentum.

6. Εξαγωγή γραφικών αποτελεσμάτων προσομοίωσης (Cadence spectre) της διάταξης που προσομοιώθηκε με ηλεκτρομαγνητική προσομοίωση για τον χαρακτηρισμό της απόδοσης και της ορθής λειτουργίας του μίκτη.

7. Έλεγχος DRC (Design-Rule Checker) και LVS (Layout versus Schematic).

Η σειρά των παραπάνω βημάτων δεν είναι αυστηρή αλλά επαναλαμβάνονται μέχρι να επιτευχθεί η επιθυμητή λειτουργία του κυκλώματος.

Στόχοι για τις επιδόσεις του μίκτη

Για τον μίκτη της παρούσας διατριβής τέθηκαν ορισμένα λειτουργικά όρια τόσο για την αυτόνομη λειτουργία του όσο και για τη λειτουργία του στο πλαίσιο του ομαδικού έργου. Τα όρια αυτά αφορούν τα μεγέθη που έχουν εξηγηθεί λεπτομερώς προηγουμένως ως προς τη σημασία και τη λειτουργικότητα και είναι η γραμμικότητα, το κέρδος μετατροπής, η προσαρμογή εισόδου/εξόδου, η κατανάλωση και η ευρυζωνικότητα. Ονομαστικά, οι προδιαγραφές αυτές παρουσιάζονται παρακάτω.

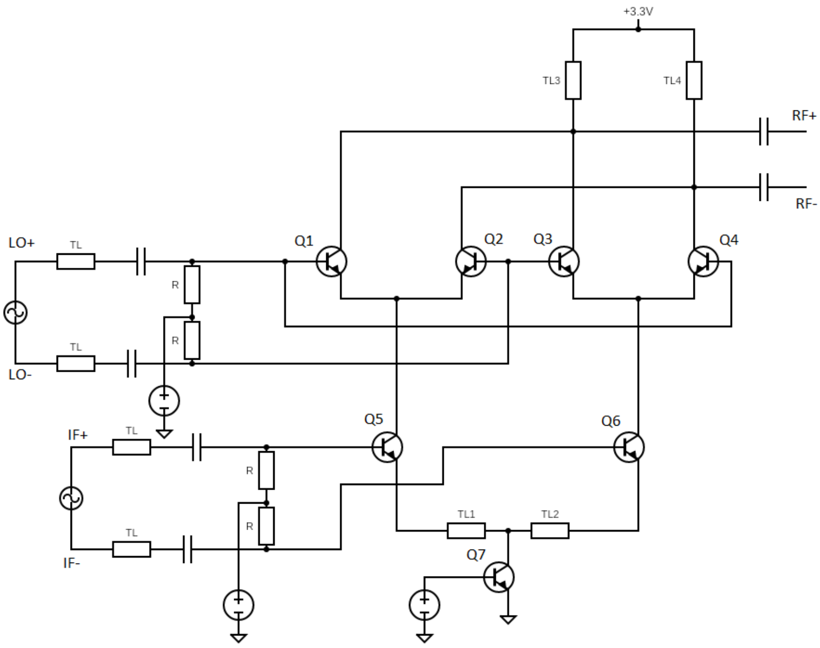
Βασικές προδιαγραφές για τον μίκτη QDB:

- IF εύρος ζώνης: 1-20 GHz
- 3dB IF ισχύς σήματος dBm ~ -40 → -15 dBm
- LO ισχύς ~ -5 dBm → 5 dBm
- 3dB RF εύρος ζώνης: 30GHz (130GHz-160GHz)
- SSB κέρδος μετατροπής: 0 – 10 dB
- OP1dB > -18 dBm
- OIP3 > -7 dBm
- IRR > 20 dBc
- LO-to-RF απομόνωση > 30 dB
- Pdc < 100mW
- Τερματισμοί στα 100Ω

Σχεδίαση μίκτη

Ο ενεργός μίκτης που σχεδιάστηκε είναι διπλά εξισορροπημένος, σε Gilbert τοπολογία, όπως φαίνεται στο Σχήμα 2. Όλες οι ενεργές διατάξεις είναι HBT, με το ίδιο πλάτος μάσκας εκπομπού 0,22 μm. Το διακοπτικό στάδιο αποτελείται από δύο ζεύγη [10] Q1, Q2, Q3 και Q4, με μήκος μάσκας εκπομπού ίσο με 2,7 μm, και είναι πολωμένα κοντά στην περιοχή pinch-off, λειτουργώντας ως διακόπτες. Για τη βαθμίδα διαγωγιμότητας, τα τρανζίστορ Q5 και Q6, με μήκη μάσκας εκπομπού ίσα με 4,5 μm, μετατρέπουν το σήμα τάσης IF σε ρεύμα και πολώνονται στη βέλτιστη πυκνότητα ρεύματος για μέγιστη ft [2]. Το ρεύμα ουράς ρέει μέσω του HBT Q7 το οποίο έχει μήκος μάσκας εκπομπού 10 μm.

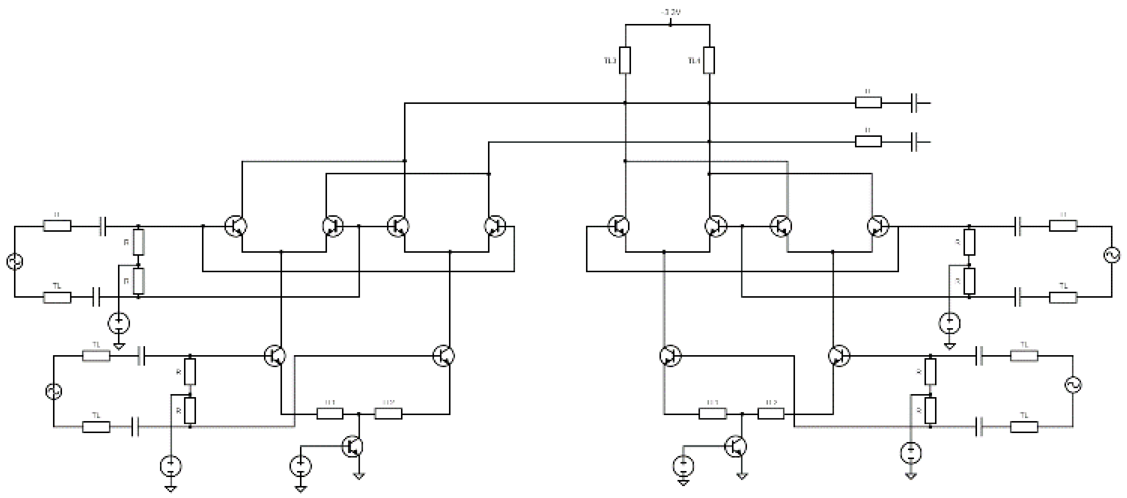
Οι γραμμές μεταφοράς TL1 και TL2 χρησιμοποιούνται για τον επαγωγικό εκφυλισμό εκπομπού, βελτιώνοντας τη γραμμικότητα του μίκτη, ενώ οι γραμμές TL3, TL4 στην έξοδο, χρησιμοποιούνται για την επιβολή του επιτευχθέντος κέρδους μετατροπής [10]. Δίκτυα προσαρμογής εντός του κυκλώματος που αποτελούνται από πυκνωτές MIM, γραμμές μεταφοράς και αντιστάσεις TaN προστίθενται στις θύρες LO, IF και RF για να επιτευχθεί ο ευρυζωνικός συντονισμός συχνότητας. Η κυψέλη του μίκτη βρίσκεται υπό τάση τροφοδοσίας 3,3 V, ενώ η πόλωση κάθε HBT πραγματοποιείται με εξωτερικά ελεγχόμενες ανεξάρτητες πηγές τάσης μέσω αντιστάσεων πολυπυριτίου.



Σχήμα 4. Σχηματική αναπαράσταση της προτεινόμενης κυψέλης μίξης D-Band.

Σχεδίαση διαμορφωτή

Ο διαμορφωτής αποτελείται από δύο κυψέλες μίκτη ανοδικής μετατροπής, με την ίδια τοπολογία όπως φαίνεται στο Σχ. 5. Οι δύο μίκτες λειτουργούν τετραγωνικά, διαμορφώνοντας τα διαφορικά σήματα I και Q με τα διαφορικά σήματα LOI (φάση 0μοίρες) και LOQ (φάση 90μοίρες) αντίστοιχα [11]. Με αυτόν τον τρόπο επιτυγχάνεται ο λόγος απόρριψης εικόνας χωρίς τη χρήση πρόσθετου φιλτραρίσματος [5].

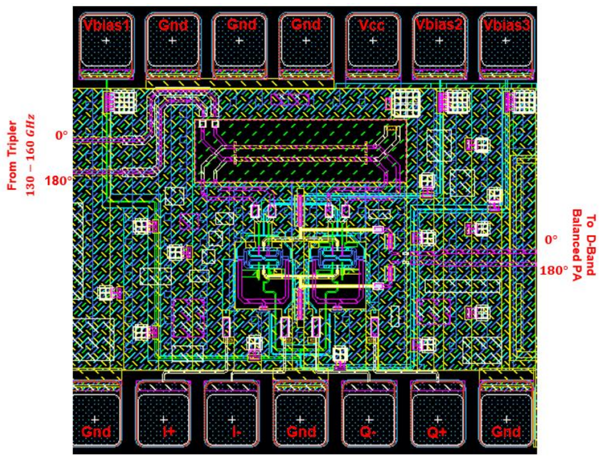


Σχ. 5. Σχηματική αναπαράσταση του προτεινόμενου διαμορφωτή μετατροπής προς τα πάνω χαμηλής πλευρικής ζώνης.

Σχεδίαση Layout

Ο διαμορφωτής I/Q υλοποιείται σε διεργασία SiGe BiCMOS 130 nm με συχνότητα διέλευσης f_T = 250 GHz και συχνότητα ταλάντωσης f_max = 370 GHz. Η τεχνολογία διαθέτει 6 στρώματα χαλκού και ένα ανώτερο μεταλλικό στρώμα αλουμινίου. Διατίθενται επίσης πυκνωτές MIM, αντιστάσεις πολυπυριτίου και TaN. Το ενδιάμεσο μέταλλο 4 χρησιμοποιείται ως γείωση αναφοράς, ενώ το μέταλλο 3 χρησιμοποιείται ως επίπεδο τροφοδοσίας. Τα κατώτερα μέταλλα 1, 2 χρησιμοποιούνται για διασυνδέσεις συνεχούς ρεύματος. Τα παχιά ανώτερα μέταλλα 5 και 6 χαμηλών απωλειών υλοποιούν όλες τις δομές RF προσφέροντας μειωμένη χωρητική σύζευξη με τη γείωση.

Προκειμένου να παρέχονται οι κατάλληλες φάσεις LO στις βάσεις των HBTs του σταδίου μεταγωγής, παρεμβάλλεται ένας καλά καθορισμένος διαφορικός συζεύκτης LO μεταξύ του κυκλώματος παραγωγής LO και του διαμορφωτή. Τέλος, η διάταξη υλοποιήθηκε με το εργαλείο Cadence Layout και η τελική σχεδίαση απεικονίζεται στο σχήμα 6.



Σχήμα 6. Τελική διάταξη του προτεινόμενου διαμορφωτή I/Q.

Αποτελέσματα προσομοίωσης

Η λειτουργία υψηλής συχνότητας του προτεινόμενου διαμορφωτή I/Q απαιτεί ακριβή μοντελοποίηση των μεταλλικών διασυνδέσεων των τρανζίστορ. Έτσι, χρησιμοποιείται RC parasitic extraction μέχρι το μέταλλο 4 για όλα τα επιλεγμένα HBTs ενώ η διασύνδεση μέχρι το κορυφαίο μέταλλο 6 καθώς και όλες οι δομές RF και τα δίκτυα προσαρμογής προσομοιώνονται EM μέσω του Momentum ADS.

Μια σύνοψη των αποτελεσμάτων της προσομοίωσης σε σύγκριση με τις αρχικές προδιαγραφές παρουσιάζεται στον πίνακα I.

TABLE I. SUMMARY OF SIMULATION RESULTS

Metrics	***Specification***	***Simulated***
SSB Conversion Gain	0-10dB	> 5 dB
OP1dB	> -18dB	> -12dBm
OIP3	> -7 dBm	> -7 dBm
Power Consumption	< 100mW	~ 90mW
LO Rejection	> 30dB	~ 40 dB
Sideband Suppression	> 35 dB	~ 40 dB

CONTENTS

CHAPTER 1: INTRODUCTION

Radio Frequency Spectrum and 5th & 6th Generation Mobile Communications

Electromagnetic energy travels in waves ranging from long-length radio waves to very short gamma rays. Wavelength, which is a kind of classification of electromagnetic waves, is one of their most important characteristics. For example, the energy involved in an electromagnetic wave depends on the wavelength and is inversely proportional to it, or equivalently, proportional to its frequency. Then, different electronic devices detect different wavelengths of electromagnetic energy, so a number of applications in telecommunications are classified by wavelength. In particular, mobile communications are subject to the radio frequency spectrum from the order of kHz to GHz.

In summary, the radio frequency bands can be defined as follows in Table I:

mm-wave frequency band	Frequency Range (GHz)
Q band	30 to 50 GHz
U band	40 to 60 GHz
V band	50 to 75 GHz
E band	60 to 90 GHz
W band	75 to 110 GHz
F band	90 to 140 GHz
D band	110 to 170 GHz
G band	110 to 300 GHz

Table 1.1: Classification of millimeter-wave frequency bands.

The transmission of the signal in space can be achieved by modulating the signal in terms of amplitude (AM), frequency (FM) and phase (PM), or by a combination of the former, in both analog and digital modulations. Internationally, the demand for spectrum is constantly increasing with the growth in the number of electronic devices, which makes the electromagnetic spectrum an important resource. Therefore, there is a constant need to develop new technologies and spectrum management techniques to optimally serve users. In recent years, research has turned to exploiting the higher frequency spectrum, which remained unused, thus aiming at millimeter wave operating frequencies.

With the first steps of 5G technology, new ideas and innovative plans have already been formed for 6G technology. The 6G will introduce the new communications society of 2030 providing additional capabilities and technologies to serve users [1]. Worldwide, organizations are exploring the innovative field of THz technologies, expecting in the next few years to have unlimited and full wireless communication, for radar, navigation, positioning, sensing, communications applications, etc [2], [3]. The requirements, therefore, for the new 6G networks relate to spectrum and power management, peak data rate, latency, capacity and mobility. More specifically, peak data rate is expected to exceed 1 Tb/s, i.e. 100 times higher than 5G, user-experienced data rate 1Gb/s, i.e. 10 times higher than 5G, latency 10-100 μs, 10 times higher network density than 5G, energy efficiency 10-100 and spectrum efficiency 5-10 times higher than 5G [4].

Some advantages of the new frequency band are the fact that there is no "spectral congestion" and, in addition, the scale of the design is much smaller. The size of the antenna depends on the wavelength of the signal, therefore, the space it occupies is significantly reduced, and the analog and digital circuits also become much smaller, as suggested by the 130nm technology used for this thesis. This thesis deals with the design and implementation of an integrated D-Band quadrature I/Q modulator, one of the most critical blocks in modern mm-wave and sub-THz transmitters [5]. Implementations of such D-Band I/Q modulators are included in several recent 6G and beyond 5G applications [6], [7], [8].

In figure 1.1 [9] the three latest telecom technologies, the 4^{th} 5^{th} and 6^{th} generation, are presented, comparing applications and other technology features.

		4G	5G	6G
Usage Scenarios		• MBB	• eMBB • URLLC • mMTC	• FeMBB • ERLLC • umMTC • LDHMC • ELPC
Applications		• High-Definition Videos • Voice • Mobile TV • Mobile Internet • Mobile Pay	• VR/AR/360° Videos • UHD Videos • V2X • IoT • Smart City/Factory/Home • Telemedicine • Wearable Devices	• Holographic Verticals and Society • Tactile/Haptic Internet • Full-Sensory Digital Sensing and Reality • Fully Automated Driving • Industrial Internet • Space Travel • Deep-Sea Sightseeing • Internet of Bio-Nano-Things
Network Characteristics		Flat and All-IP	• Cloudization • Softwarization • Virtualization • Slicing	• Intelligentization • Cloudization • Softwarization • Virtualization • Slicing
Service Objects		People	Connection (People and Things)	Interaction (People and World)
KPI	Peak Data Rate	100 Mb/s	20 Gb/s	≥1 Tb/s
	Experienced Data Rate	10 Mb/s	0.1 Gb/s	1 Gb/s
	Spectrum Efficiency	1×	3× that of 4G	5–10× that of 5G
	Network Energy Efficiency	1×	10–100× that of 4G	10–100× that of 5G
	Area Traffic Capacity	0.1 Mb/s/m^2	10 Mb/s/m^2	1 Gb/s/m^2
	Connectivity Density	10^5 Devices/km^2	10^6 Devices/km^2	10^7 Devices/km^2
	Latency	10 ms	1 ms	10–100 μs
	Mobility	350 km/h	500 km/h	≥1,000 km/h
Technologies		• OFDM • MIMO • Turbo Code • Carrier Aggregation • Hetnet • ICIC • D2D Communications • Unlicensed Spectrum	• mm-Wave Communications • Massive MIMO • LDPC and Polar Codes • Flexible Frame Structure • Ultradense Networks • NOMA • Cloud/Fog/Edge Computing • SDN/NFV/Network Slicing	• THz Communications • SM-MIMO • LIS and HBF • OAM Multiplexing • Laser and VLC • Blockchain-Based Spectrum Sharing • Quantum Communications and Computing • AI/Machine Learning

Figure 1. 1: The network features of 4G, 5G, and the future 6G.

CHAPTER 2: MIXER THEORY

2.1 Transmitter-Receiver (Transceiver) Chain [10]

In both digital and analog communications, the communication system includes the transmitter system and the receiver system among which the transmission channel interferes. The difference between the analog and digital systems lies in the form of the transmitted signal, the signal processing and the performance goals.

More generally, the transmitter performs baseband processing, modulation, amplification and filtering to avoid leakage to adjacent channels. On the other hand, the receiver performs filtering, demodulation and amplification, while primarily, processing the selected channel by rejecting, adequately, strong adjacent interference.

2.1.1 The Transmitter

The transmitter's aim is to embody the digital information, in the form of a signal, to the modulated signal and to couple the modulated signal to the transmission channel. In addition, it gives the signal the ability to self-correct, so that the telecommunications system is more robust. For this purpose, it uses FEC coding, which detects and corrects possible errors in the information digits. In the subsequent stages, the information digits with the extra digits of the encoding are formed into symbols, with a grouping that depends on the type of modulation used. After the signal is converted from digital to analog, in the next stages, baseband filtering is performed and signal mixing, to shift the signal spectrum to the desired frequency band. Then the signal is filtered, by a bandpass filter, to reject unwanted frequency bands, and amplified through the PA, before, finally, being sent to the antenna for transmission of the signal in space. This amplification is fundamental, in order the signal to be transferred for a long distance, however, is not ideally linear, thus causing some distortion. Such distortions could be spectral spread, causing adjacent channel interference. The way to avoid this problem is the addition of a bandpass filter (BPF). A short illustration of the chain that was elaborated above is illustrated in figure 2.1.

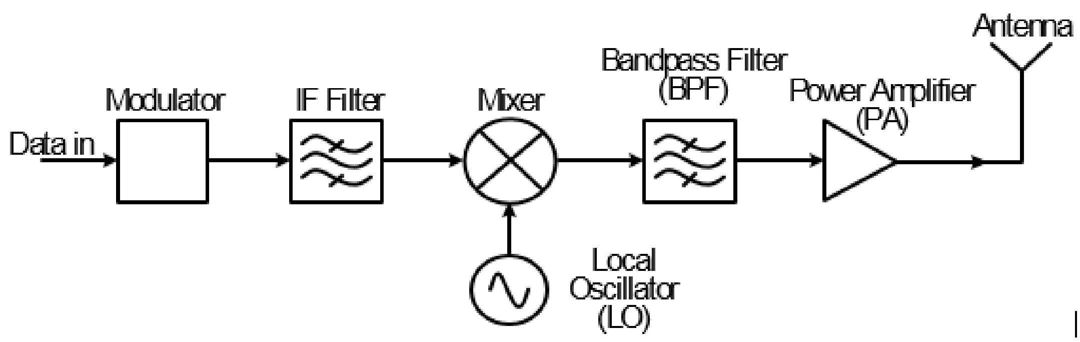


Figure 2. 1: Illustration of a telecommunication transmitter chain.

2.1.2 The Channel

The modulated signals are transmitted either wirelessly or wired. Sometimes, both modes may be combined to achieve the telecommunication link. In wireless transmission, the telecommunication channel is the ground atmosphere and ground surface, which is exploited due to the reflections it causes, and the natural and artificial obstacles that affect electromagnetic waves. In wired transmission, the telecommunication channel is a wired transmission medium, such as coaxial cable, optical fiber or metallic waveguide. It should be noted that within the group research, of which this thesis was a part, a new approach to wired transmission, the plastic waveguide (Polymer Microwave Fiber - PMF), was used.

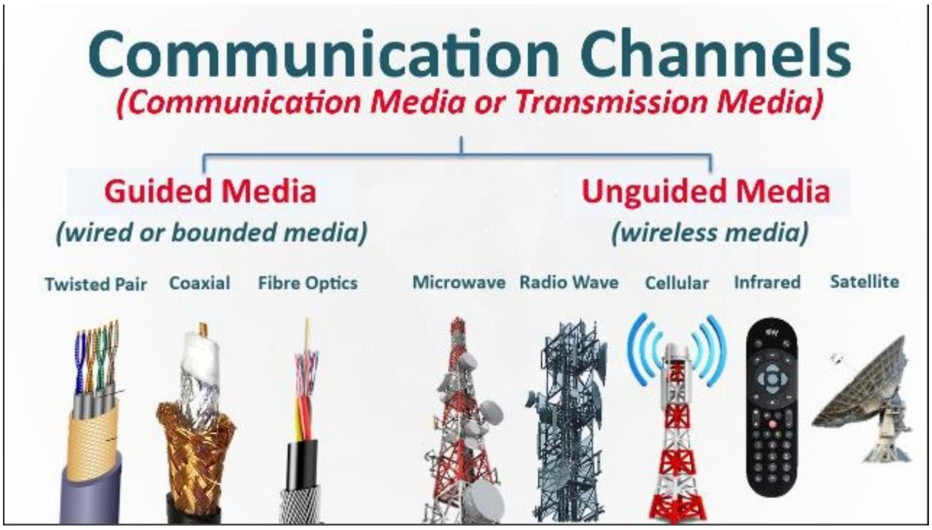


Figure 2. 2: Types of communication channels

2.1.3 The Receiver

In turn, the receiver consists of a number of functional units, where depending on the application there are possible variations. In general, it consists of electronic filters, which isolate the desired signal from the multitude of signals collected by the receiver antenna, a low-noise electronic amplifier, one or more frequency mixers, depending on the modulation technique, an intermediate frequency amplifier, followed by the digital demodulation units.

For digital demodulation, a demodulator is used, whose role is to map symbols, received from the environment and processed by the previous stages, into digits, using a decision circuit that decides which point of the constellation of the digital modulation scheme was transmitted through the received symbol. The stream of received digits resulting from the digital modulation is then processed by the FEC decoder, if used in the transmission system, to keep the information digits. Finally, the information is derived from the receiving system as a digital data stream that is routed to the device.

Depending on the application and device requirements, the order and type of the transmitter’s and receiver’s devices might vary. In addition, the receiver’s system is required to consist of units designed with a low equivalent noise temperature, in order to minimize the noise in the signal. It is significant, the low noise amplification, implemented by the LNA, to be placed immediately after the receiver’s antenna, to limit the noise added to the signal by the channel.

A representative structure of the receiver telecommunication chain is shown in figure 2.3.

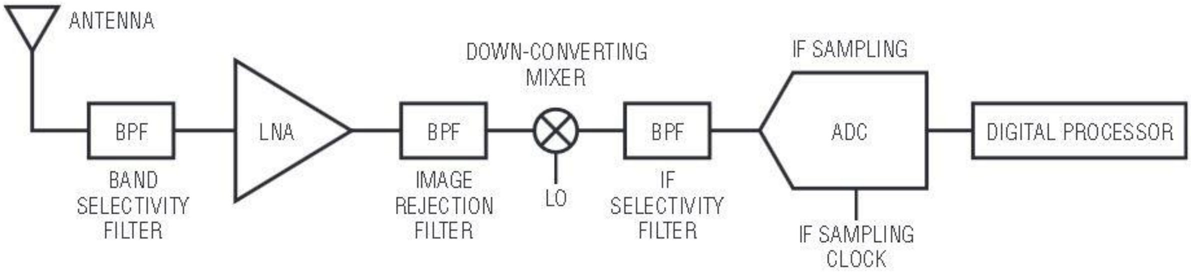


Figure 2. 3: Illustration of a telecommunication receiver chain

2.1.4 The Mixer

The mixer is one of the most critical blocks in modern mm-wave and sub-THz transmitters [5]. It's position in the transceiver chain is depicted above. In more detail, at the transmitter, the mixer is usually found before the Power Amplifier (PA), where its role is to convert the desired signal at higher frequencies before its amplification and final transfer through the channel. At the receiver, the mixer is often placed after the Low Noise Amplifier (LNA) and its target is to convert the received signal to lower frequencies before it is sent to be processed by the device.

2.2 Mixing and Modulation [11], [12]

As mentioned above, one of the most important functions in the transceiver chain is that of mixing. RF mixing enables the desired signal to be frequency-shifted, so that, for example, its processing is carried out at low frequencies, where it is easier to manage, while its transmission on the channel is carried out at higher frequencies, depending on the requirements of the system.

A frequency mixer is a three-port electronic circuit, in which the input ports and the output port are defined. The ideal up-converter mixer has two input ports, those of Frequency Carrier, usually provided by a local oscillator (LO), and Intermediate Frequency (IF) and one output port of Radio Frequency (RF). In the case of the down-converter mixer, the IF and RF ports are reversed and, therefore, the RF port is an input port and the IF port is an output port.

By RF mixing we mean the multiplication of two signals to create new signals, at new frequencies, derivatives of the frequencies of the original signals. More generally, when two signals, f_{in1} and f_{in2}, pass through a non-linear circuit, then additional signals are created at the output of the circuit at the sum and difference of the two original frequencies ($f_{in1}+f_{in2}$) and ($f_{in1}-f_{in2}$) respectively. Such non-linear elements in a circuit, acting as multipliers, can be a diode and active elements, such as BJTs and HBTs, that are relying on the exponential I-V characteristics of the pn junction or MOSFETs or HEMTs, that follow the square-law behavior at low effective gate voltages, but in nanoscale nodes they behave linearly. Generally, MOSFETs have weaker non-linear behavior than BJTs. This means that bipolar devices produce more multiplication products, that needs to be removed.

If we consider the two input signals as sine waves, then as shown in figure 2.4, at the output we expect a signal in which the sum and the difference of the input signals co-exist. Due to the fact that the mixer is a non-linear circuit, as mentioned previously, at the output, harmonics of the original signals appear. In order to eliminate these harmonics, filters are used at the input and output ports LO, IF, RF to select the appropriate frequencies of interest. However, not only harmonics have to be suppressed, but, also, input signals (LO, IF or RF) that could appear at the output (RF or IF) as leakage frequencies.

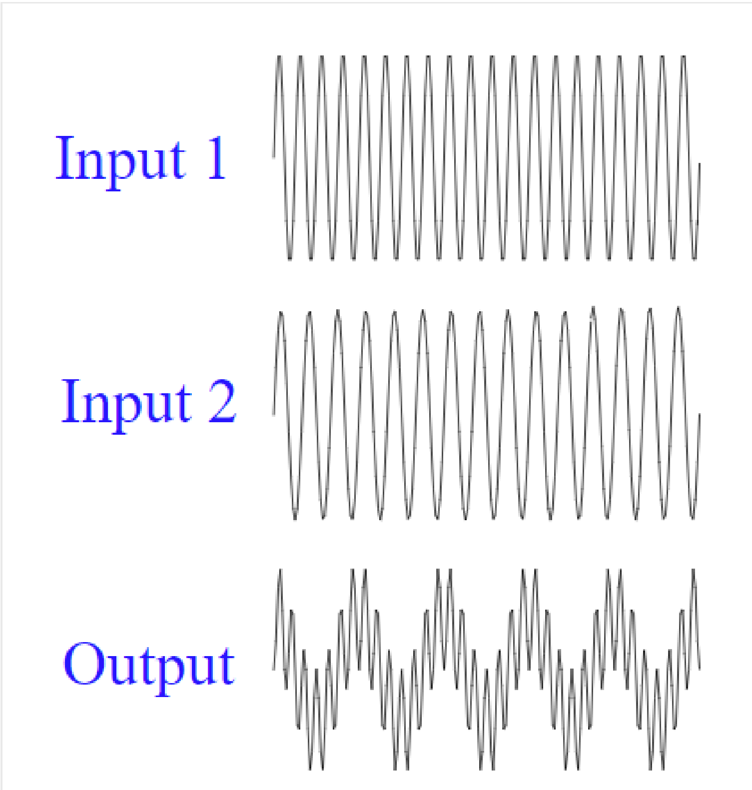


Figure 2. 4: Mixing or multiplying two sine signals together

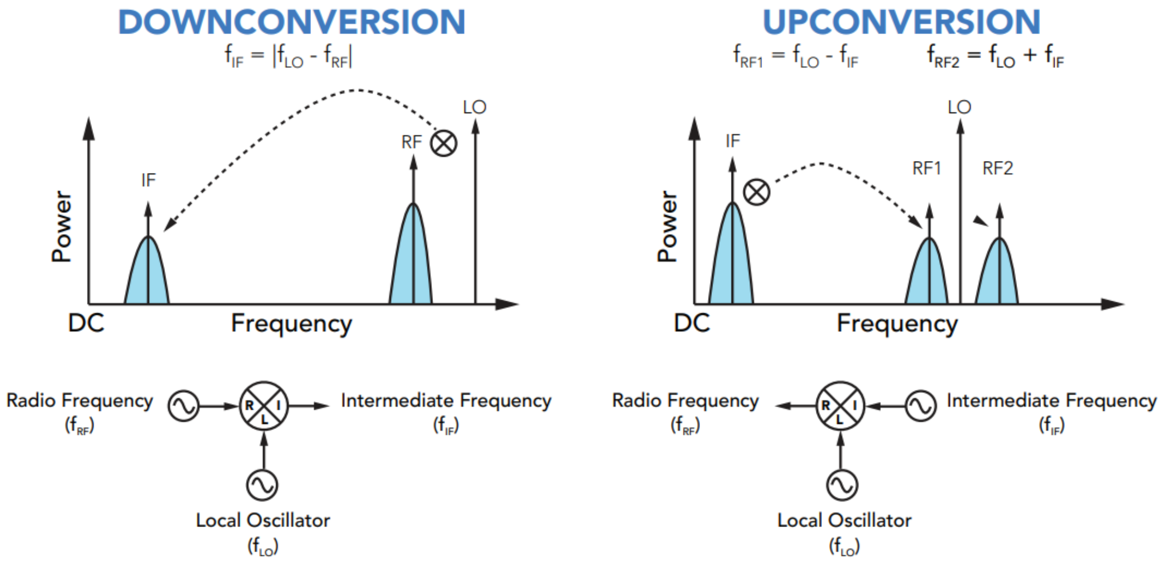


Figure 2. 5: Definitions of down-conversion and up-conversion.

The choice of IF or RF ports for input mapping depends on the mixer application. When the desired output frequency is lower than input frequency, then we have down-conversion and the RF port is an input port and the IF port is an output port. In this case, the equation (1) describing the operation of the mixer, in the spectrum domain, is the following:

$f_{IF} = |f_{LO} - f_{RF}|$ (1)

In the opposite case, when the desired output frequency is higher than the input, then the process is called up-conversion and IF is the input port, while RF is the output port, so the following equation (2) applies:

$f_{RF} = f_{LO} \pm f_{IF}$ (2)

These cases are also described in figure 2.5. The sum frequency $f_{RF} = f_{LO} + f_{IF}$ is known as upper sideband (USB) and the difference $f_{RF} = f_{LO} - f_{IF}$ is called lower sideband (LSB), as illustrated at figure 2.6 [5]. Regarding of the desired output frequency somebody can either choose the upper or the lower sideband, which are always separated by 2*ωIF in frequency. The other sideband, the undesired one, is often called image frequency (IM), or, image. Several techniques exist for image rejection, including band-stop filters, centered at the image frequency. Same logic applies to the receiver too. However, the rejection of the image frequency, also means that half of the output power is lost.

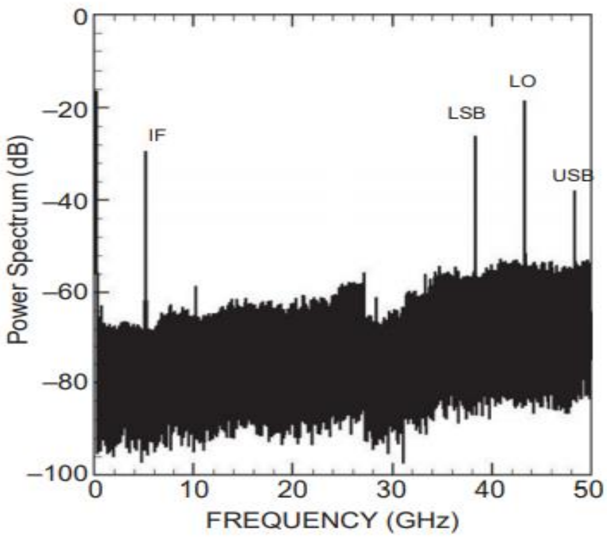


Figure 2. 6: Measured spectrum at the RF output of an upconversion mixer showing the IF signal at 5GHz, the LO at 43GHz and the USB and LSB signals at 38GHz and 48GHz, respectively.

Modulators can synthesize circuits, for example gilbert cells, to generate replicas I and Q of the carrier signal, based on quadrature generation [5]. They employ 90 degrees hybrids of the signal in both input differential ports, and depending on the desired sideband, the sign is set. In figure 2.7, an example of a modulator, based on gilbert cells, is presented.

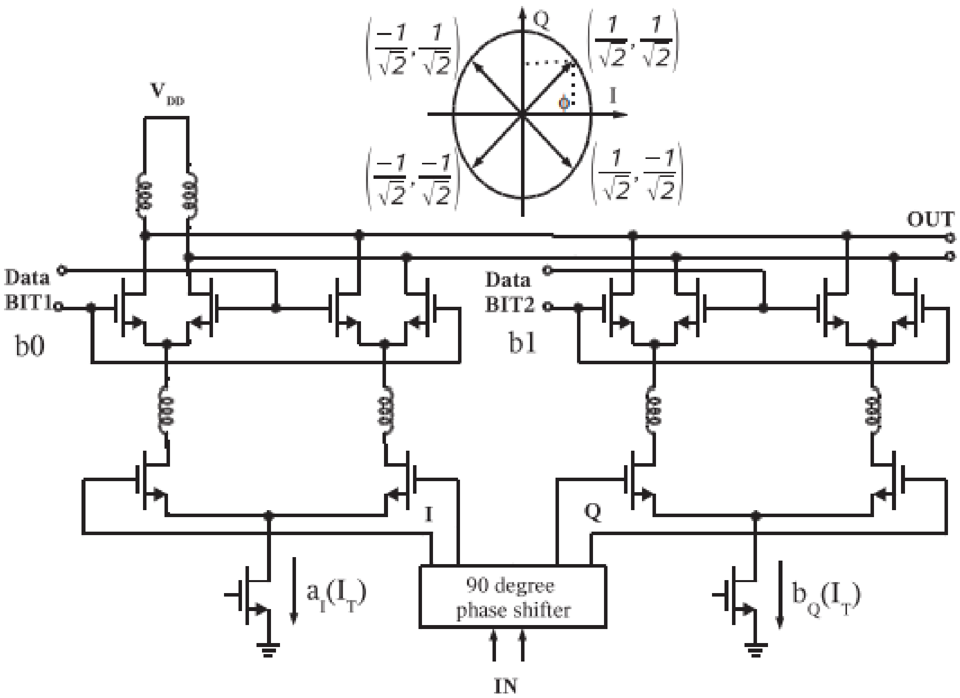


Figure 2. 7: CMOS schematic of a mm-wave QPSK modulator based on quadrature and Gilbert cells.

Contrary to mixers their disadvantages are that they occupy larger area on the chip and that they require higher power, but, a main advantage is the image rejection that can be achieved.

For the mathematical analysis of the mixer block [13] we begin with the emitter-coupled pair, figure 2.8, as it follows.

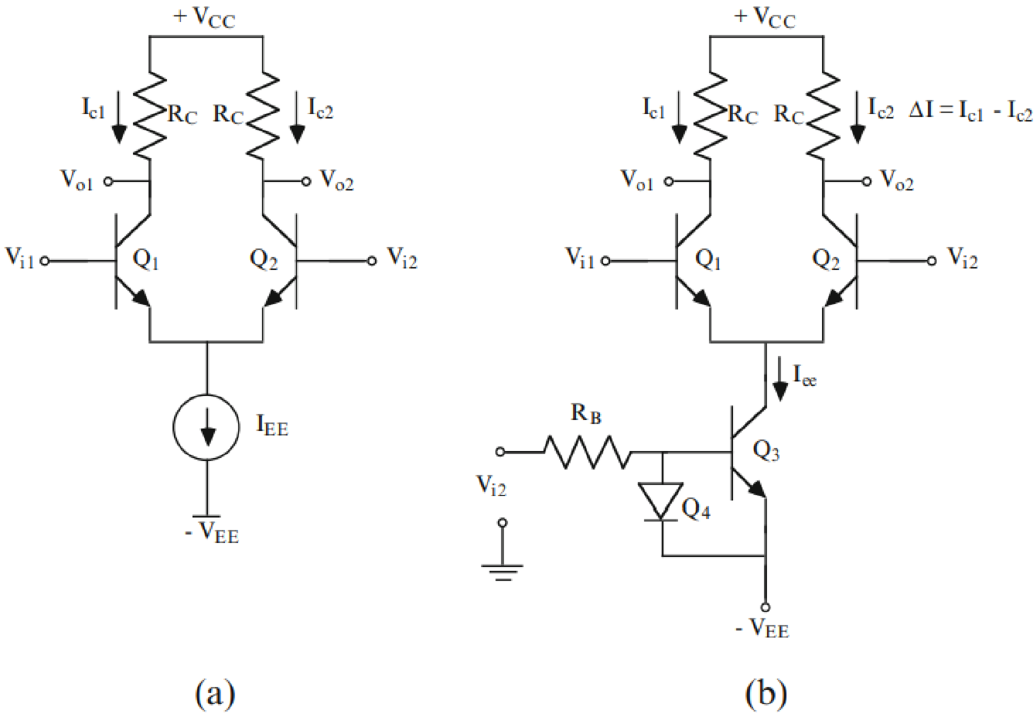


Figure 2. 8: (a) A simple emitter-coupled pair. (b) A second input introduced through Iee.

The collector currents, that are generated, are given by the equations (3) and (4), that associate the inputs with the output currents:

$$I_{C1} = \frac{I_{EE}}{2}\left[1 + \tanh\left(\frac{d}{2}\right)\right] \quad (3)$$

$$I_{C2} = \frac{I_{EE}}{2}\left[1 - \tanh\left(\frac{d}{2}\right)\right] \quad (4)$$

Where $d = \frac{u_{i1}}{V_t}$ and $u_{i1} = V_{i1} - V_{i2}$ is the differential-mode input signal.

The differential output voltage is

$$u_o = V_{o1} - V_{o2} = -R_c(I_{C1} - I_{C2}) = -I_{EE}R_C \tanh\left(\frac{d}{2}\right) \quad (5)$$

for small signals, $d \ll 1$, and $\tanh\left(\frac{d}{2}\right) \approx \frac{d}{2}$ and

$$u_o \approx -I_{EE}R_C\left(\frac{u_{i1}}{2V_t}\right) \quad (6)$$

Adding a second input at the tail current I_{EE}, as shown in figure 2.8.b, we get

$$V_{i2} = u_{i2} + V_{B2} \quad (7)$$

Then the total common-emitter current source is:

$$I_{EE} \approx \frac{V_{i2} - V_{BEon} - (-V_{EE})}{R_B} = \frac{u_{i2}}{R_B} + I_{EE} \quad (8)$$

Then, the differential output voltage of the ECP can be expressed as:

$$u_o = -\frac{R_C}{R_B}\frac{u_{i1}u_{i2}}{2V_t} - \frac{R_C I_{EE} u_{i1}}{2V_t} = u_{om} + f(I_{EE}, u_{i1}) \quad (9)$$

u_{om} is the term of interest in the mixer and can be expressed as

$$u_{om} = -Ku_{i1}u_{i2} \quad (10)$$

where

$$K = \frac{R_C}{R_B}\frac{1}{2V_t} \quad (11)$$

One common technic to eliminate the second term of the output equation is to use the following circuit in figure 2.9.

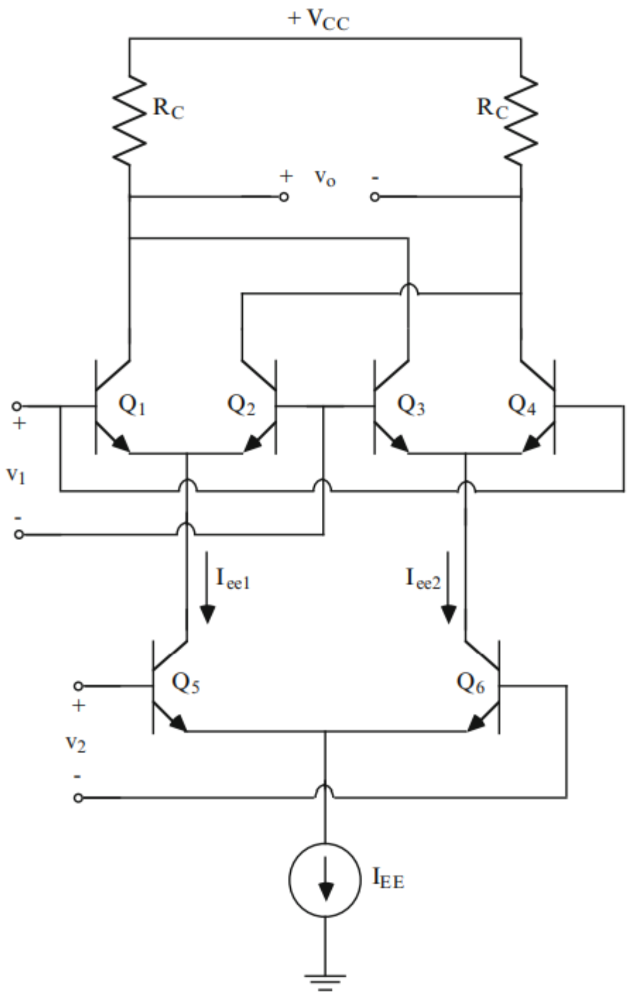


Figure 2. 9: A fully balanced four-quadrant multiplier circuit.

In which the two common-emitter current sources are also out of phase and are given by the equations:

$$I_{ee1} = I_{EE} + i_{ee} \quad (12)$$

$$I_{ee2} = I_{EE} - i_{ee} \quad (13)$$

And the output is then

$$u_o = -[(I_1 - I_2) + (I_3 - I_4)]R_C \qquad (14)$$

$$= -\left[I_{EE}\tanh\left(\frac{u_{i1}}{2V_t}\right) + I_{EE2}\tanh\left(-\frac{u_{i1}}{2V_t}\right)\right]R_C$$

$$= -(I_{EE1} - I_{EE2})R_C\tanh\left(\frac{u_{i1}}{2V_t}\right)$$

$$= u_{om} = -\frac{R_C I_{EE}}{4V_t^2}\, u_{i1}u_{i2}$$

The above circuit is referred as fully balanced four-quadrant multiplier. As the output equation indicates, the circuit has the same relative behavior for all input vi1 - vi2 combinations, but is dependent of the input signal's sign.

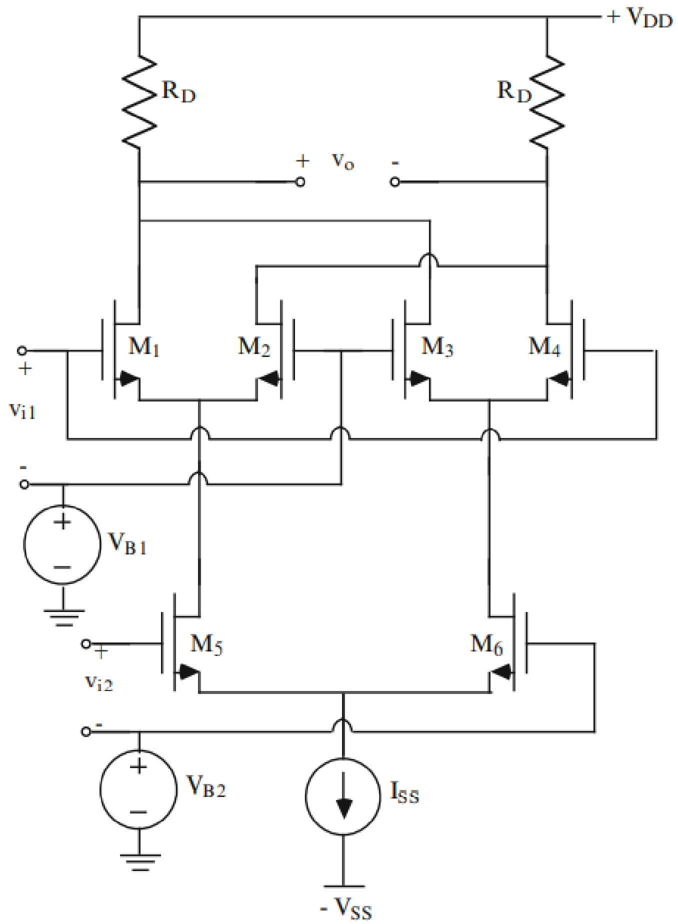


Figure 2. 10: A MOS analog multiplier using source-coupled pairs.

To formalize the mixer operation, we assume now that in both inputs, i1, i2, sinusoidal signals are implemented, as follows,

$$V_{i1} = V_{i1A} cos\omega_1 t \quad (15)$$

$$V_{i2} = V_{i2A} cos\omega_2 t \quad (16)$$

Assuming that the mixer has a constant gain K, the output, as proven from the previous analysis is

$$V_{out} = \frac{K}{2} V_{i1A} V_{i2A} [\cos(\omega_1 - \omega_2)\, t + \cos(\omega_1 + \omega_2)\, t] \quad (17)$$

2.3 Matching Networks [14]

In contrast to low frequencies where the wavelength of the signal exceeds one meter, at high frequencies the electrical distance between the circuit's pads and the external terminals becomes comparable to the wavelength of the signal length. The impedance mismatches at either side cause reflections that can significantly reduce the signal strength that reach the destination circuit. The typical impedance value imposed by standard test equipment is 50Ω.

In addition, in order to ensure maximum power transfer between the signal source and a circuit, the input impedance of the amplifier, Z_{IN}, must match that of the signal source, Z_S and, more specifically, it must follow the equation $Z_{in} = Z_S^*$ (conjugate matching). The same applies to the maximum power transfer from the circuit to the its load. The output impedance of the circuit, Z_{OUT}, must be matched to load impedance, Z_L. Therefore, the corresponding matching networks must be introduced between the circuit and the signal source and between the amplifier and the load.

Often, in high frequency applications, Z_S and Z_L are equal to an actual impedance Z_0.

2.4 S-Parameters [15]

At microwave and mm-wave frequencies the S-parameters, as well as the ABCD parameters, play a primary role thanks to the ease of extraction and measurement.

The S-parameters are defined by the ratios of incident and reflected power waves. The normalized incident, a_j, and reflected, b_i, power wave is written respectively as shown below.

$a_j = V_j^+ /\sqrt{Z0}$ and $b_i = V_i^- /\sqrt{Z0}$ (18)

First, the scattering matrix (19) is used to derive the equations that describe the relations between a_j, b_i and S-parameters. It consists of the equations of S_{ij} with the normalized incident voltage waves ai and the normalized reflected voltage waves b_i.

$$\begin{bmatrix} b_1 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \times \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} \qquad (19)$$

Where

$S_{ij} = b_i /a_j \; [a_k = 0 \; for \; k \neq j]$ (20)

In the above equation indexes i and j indicate the ports. Thus, S_{ij} is the coefficient transmission from the port j to port i. It can be found by driving the port j with an incident wave a_j and by measuring the reflected wave bi coming out of the port i, while the incident waves at all ports other than j are equal to zero, and these ports shall be terminated with adjusted loads to avoid reflections. S_{ii} represents the reflection coefficient on port i when all other ports are ports are terminated at adjusted loads. Also, S-parameters are normalized with respect to the same reference resistance Z_0, for all ports.

For example, for the two-port circuit, in figure 11, we have the following coefficients:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (21) \rightarrow$$

$b_1 = S_{11}a_1 + S_{12}a_2$

$b_2 = S_{21}a_1 + S_{22}a_2$

Where,

S_{11}, known as the input reflection coefficient or input return loss,

S_{12}, known as reverse gain or bipolar isolation,

S_{21}, known as bipolar power gain, and

S_{22}, known as output reflection coefficient or output return loss.

The S-parameters are usually expressed in dB scale as 20log10(S_{ij})

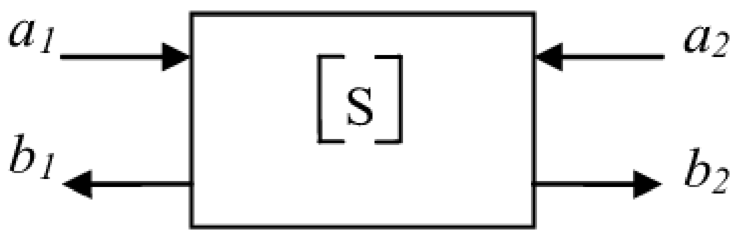


Figure 2. 11: Incident a_i and reflected b_i waves in a 2-port.

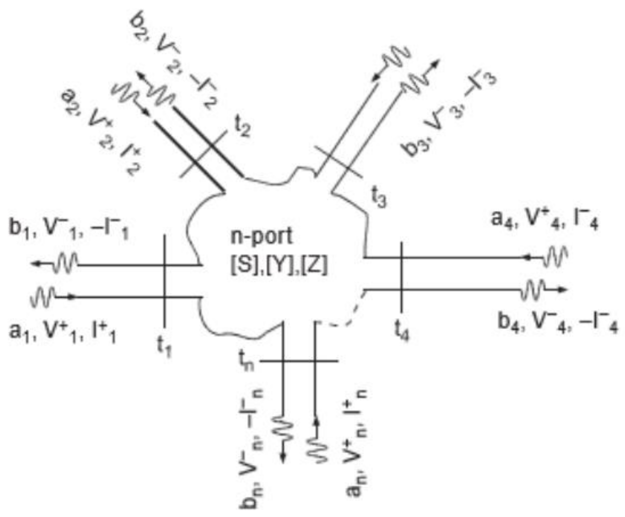


Figure 2. 12: Incident a_i and reflected b_i waves in a n-port.

2.5 Mixer specification [5], [12], [16]

2.5.1 Conversion gain

Conversion gain (or loss) is a fundamental metric for the performance of a mixer. It represents the small signal transfer function from the IF input (for upconverters) to the RF output and vice versa for the downconverter (equation). Conversion gain is more often measured as power gain, as it can be measured with more accuracy at the input and output ports. It can be seen that the local oscillator (LO) input does not feature in this figure, although, conversion gain depends on the LO power, as the transconductance is modulated by the large LO signal.

$$CG_{dB} = 10\log\left(\frac{P_{IF}}{P_{RF}}\right) \quad (22)$$

Correspondingly, conversion gain can be expressed as voltage gain

$$CG_{dB} = 20\log\left(\frac{V_{IF,RMS}}{V_{RF,RMS}}\right) \quad (23)$$

We should point out that this gain refers to two signals in different frequencies, thus explaining the term “conversion”.

Conversion gain can be maximized using the appropriate matching networks to all mixer ports, LO, RF and IF. This means that conjugately matched impedances with the input impedance of the port should be used, in order to minimize power losses, due to reflections. Matching networks, also, contributes to noise minimization.

By definition, passive mixers exhibit conversion loss and active mixers exhibit conversion gain, when operating at proper conditions.

2.5.2 Linearity

Even though mixers are implemented with non-linear devices, it is desired the mixer to be linear in its operation spectrum. The more linear, the better its performance and quality.

It can be expressed using two specifications:

i. 1dB compression point P1dB
ii. Third-order intercept point at the input, IIP3

2.5.2.1 1dB compression point P1dB

The 1 dB compression point is an important parameter used to evaluate the linearity degradation of a circuit due to distortion.

An ideal mixer would operate linearly, i.e. for every 1 dB increase in the input level, the output port would increase by 1dB too. However, a point is reached where the output cannot handle the signal, and it starts to level out. This usually happens at higher power levels for the input and beyond these levels the signal is getting compressed.

The 1 dB compression point, is the point at which the output deviates from the linear curve by 1 dB, as shown in figure 13. The specification normally refers to the input power level (IF level for upconverters) at which this compression occurs and, of course, the higher the 1dB compression point the better. In other words, the 1dB compression point is an indicator of the maximum input power level entered by the input port (IF or RF).

The 1 dB compression point is easy to measure and it provides a useful comparison between mixer to see what their high-level performance is like.

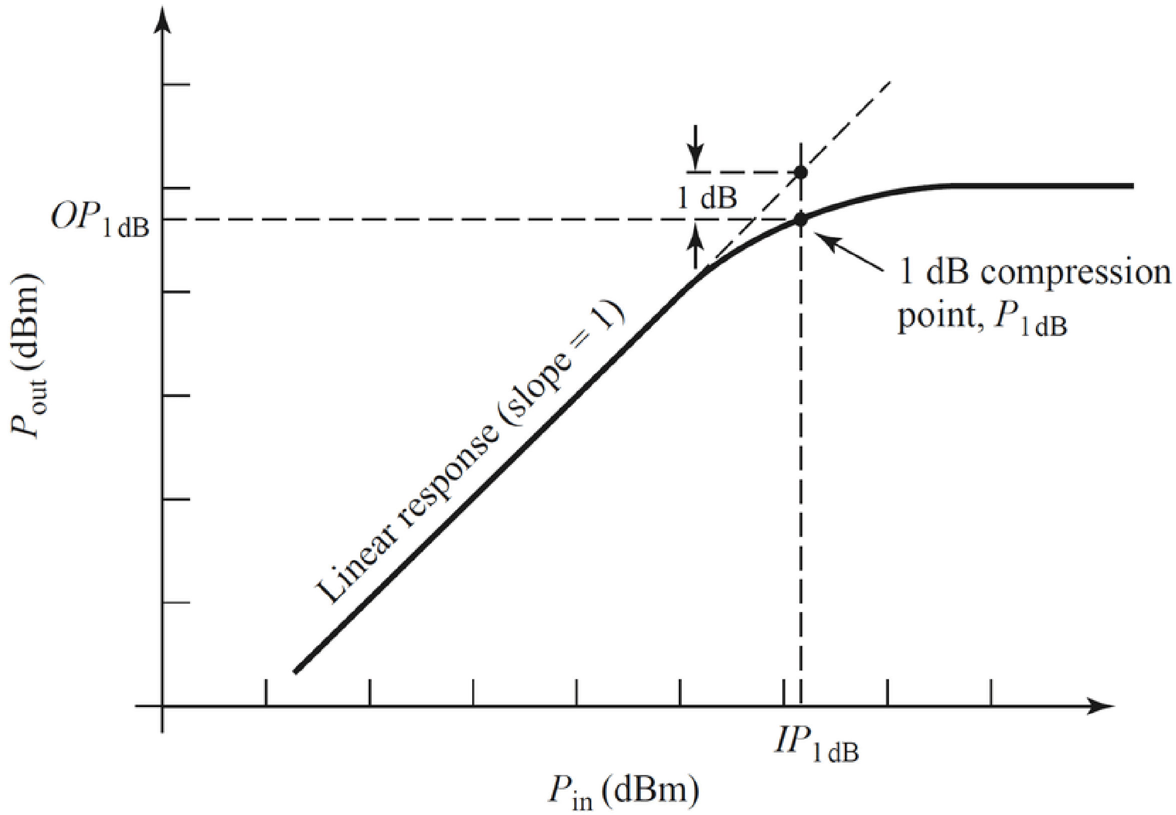


Figure 2. 13: 1dB compression point illustration.

2.5.2.2 Third-order intercept point at the input, IIP3

RF mixers usually suffer from the level of unwanted, additional signals that are generated within the mixing process, due to non-linearities, that can deteriorate the overall performance. Such non-linearities can be caused when two signals, that have a small difference in the frequency, are driven in this device and at the output intermodulation products (IM) are generated on the sum and difference of the multiples of the input frequencies, as shown in figure 14.

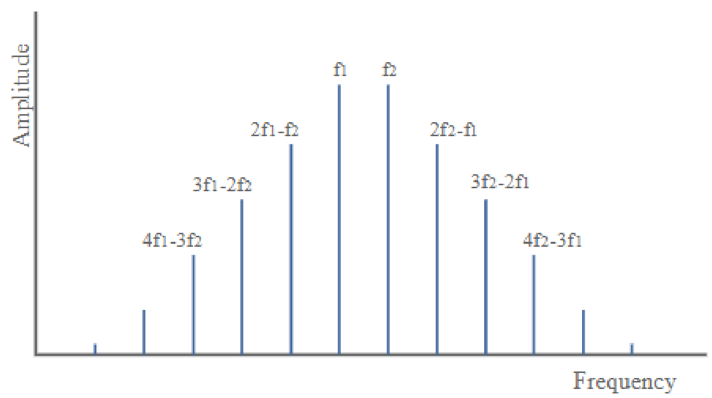


Figure 2. 14: The spectrum of intermodulation products from two signals.

The nth-order intercept point of a mixer (or amplifier) is an important parameter to evaluate the performance and the most commonly used is the 3rd. The 3rd order intercept point is a hypothetical point where the power of the third order products will have the same power level as the fundamental, as illustrated in figure 15.

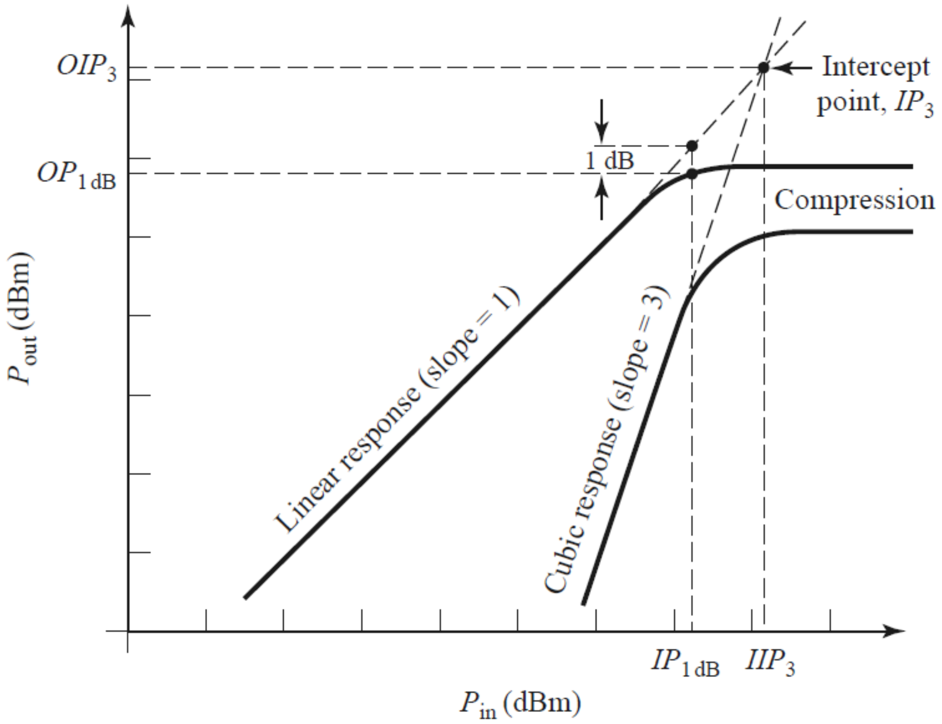


Figure 2. 15: Third-order intercept point, IP3, illustration.

The third order intercept point of a mixer of any other device is theoretical because it lies well beyond the saturation level of the device, and it many cases it would be well beyond the point at which damage occurred, especially in the case of a mixer. However, it is still a useful metric to provide information for the distortion generated by the circuit while the power levels rise.

The IP3 point can be defined for either the input or output ports. The input third order intercept point is often designated as IIP3 and the one at the output is designated OIP3. These intercept points differ in level by an amount equal to the small signal gain (or loss) of the mixer.

Two main ways exist for the definition of intercept points:

Based upon the intermodulation products: The most common approach is to apply to the input of the RF mixer two sine wave signals that have a small frequency difference, ω1 and ω2. The intermodulation products then appear at spacing equal to the input tones, and the levels can be measured. The third order products appear at three times the frequency spacing of the two signals either side of them.

The frequencies of these intermodulation products are given from the equation

$f_{IM} = \pm q f_1 \pm r f_2 \pm p f_{LO}$ (2.24)

Where variables q,r and p are positive integer numbers.

For the 3rd order IP we focus on the 3-order intermodulation distortion products, the $IM3$, $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ and especially the difference terms $2\omega_1$-ω_2-ω_{LO} and $2\omega_2$- ω_1-ω_{LO}, which are located in the output passband (RF for up-converters and IF for down-converters), figure 16.

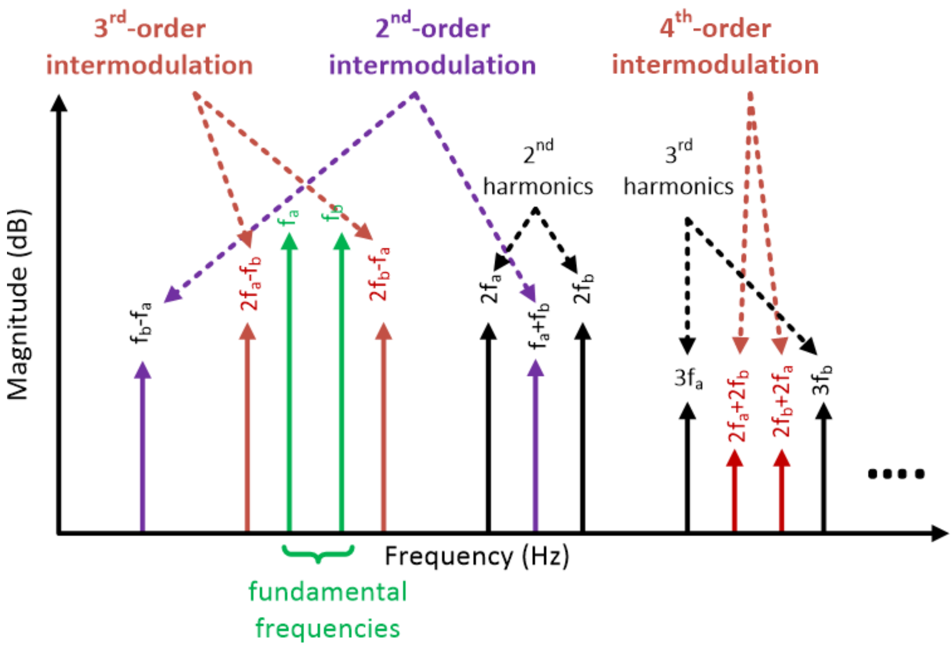


Figure 2. 16: Intermodulation products at the output of a mixer, for f_a, f_b and f_{LO} input frequencies.

Based upon harmonics: An alternative method is to use a single signal, and then the products appear at multiples of the input tone. The third order product is at three times the fundamental.

2.5.3 Isolation

With this term we describe the interaction between the IF, LO and RF ports. We mainly focus on the following definitions:

- LO to IF, $IS_{LO\text{-}IF}$
- LO to RF, $IS_{LO\text{-}RF}$
- IF to LO, $IS_{IF\text{-}LO}$

Higher isolation is always the goal in the RF mixer and if not accomplished, signal leakages are noticed between different ports. For example, if the local oscillator leaks through the input port, it could rise intermodulation distortion and if it leaks through the output port it deteriorates the overall performance. The later was a major problem addressed in the present thesis, and is presented in the following chapters.

Isolation can be achieved by the appropriate choice of mixer topology and/or filtering. Ideally, the output port (IF or RF) impedance should be a short circuit at the LO frequency and at all its harmonics. This will prevent the LO signal from leaking at the RF and IF ports. Isolation higher than 40dB is possible with double-balanced mixer topologies. Nevertheless, when all ports are differential, isolation worsens due to the presence of amplitude and phase imbalances of the differential input signals at each port. The maximum port-to-port isolation occurs when the LO and RF signals are truly differential.

The isolation is measured in terms of dB, comparing the signal entering one port, to the same signal level at the other port where it is not required. Generally, with increasing frequency, mixer isolation aggravates, due to the decreasing reactance of the stray capacitance and the more apparent circuit imbalances.

2.5.4 Noise figure

Noise and matching characteristics are crucial to achieving acceptable levels of performance in a receiver's mixer. Generally, noise figure is a specification mostly used to describe the down-converter mixer, in the receiver. It is a metric measuring the noise that is added only by the mixer in the signal, compared to the already existing noise in the signal. Noise is added from the active elements, like diodes and transistors, and from passive elements, like resistors parasitic or not.

It is more common to use the noise figure (factor) rather than the noise temperature but either way, there is a direct relationship between the noise factor at temperature T and the noise temperature Ta of a mixer.

Noise figure is described by the following equation:

$$NFdB = 10\log(SNRin / SNRout) \quad (2.25)$$

Where SNR is the signal to noise ratio and, thus NF, describes how SNR worsens by the noise added from the mixer when the signal is driven through it.

The noise figure is described in two ways for mixers, in contrast to other circuits, the single sideband (NFSSB) and the double sideband noise figure (NFDSB). The determination of the single-sided noise figure shall be made assuming that the desired frequency spectrum is on one side of the LO frequency, whereas the determination of the double-sided noise image shall be made when the spectrum of the input signal is on both sides of the LO frequency. If the gain conversion gain is the same for the RF signal and its image then it is shown that the following relationship:

$$NFSSB = NFDSB + 3dB \quad (2.26)$$

2.5.5 Stabilization

Unstable circuit configuration stimulates oscillations, which are highly undesirable for mixing operation. For that bias circuit, when used, should be stabilized at all operating frequencies of input and output ports, LO, IF and RF. Stability analysis can be done through Rollet's stability factor (K-factor). Where K is defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.27}$$

For unconditionally stable system K>1 and Δ<1. These two conditions are capable of and necessary for the unavoidable unconditional stability and can be easily assessed. Verification of unconditionally stability of the circuit, through Rollet’s factor, can be done using S parameter of the circuit, as the formula suggests.

2.6 Mixer Topologies [5]

There are many types of mixers with their practical use depended on the characteristics and performance they offer. One of the most significant classification is the one that separates mixers in active and passive.

- Passive mixers use passive electronic components, typically diodes. These components act as switching elements and, thus, this type of mixer does not provide gain, but instead losses. Still this type of mixers can offer the desired performance in many applications.
- Active mixers, on the other hand, contain active electronic components like BJTs, FETs, HBTs etc. They can provide gain, with the appropriate bias, exhibiting conversion gain.

Compared to active mixers, passive mixers have several advantages such as better linearity, wider dynamic range and therefore higher compression point, as well as zero requirements on
DC power consumption. However, passive mixers have a conversion gain of less than 0dB (essentially attenuating the input signal) or otherwise said to have a conversion loss of (Conversion Loss, CL) as opposed to active ones which usually exhibit Conversion Gain. In addition, they have a much larger image noise picture compared to active ones, as well as significantly higher LO power requirements (the power available to the mixer via the local oscillator). For these reasons, active mixers are in practice the preferred mixers in modern telecommunications systems.

Another classification of mixers depends on the number of ports the circuit contains, or, in other words, the number of terminals the non-linear device has. Depending on this criterion, the mixer can employ:

- One – port devices, such as diodes, with the combinations of filters (figure 2.17).
- Two – port devices, such as transistors, and filters (figure 2.18), or
- Three – port devices, using again devices such as transistors, but employing different device terminals for each signal. For this, differential or cascaded topologies can be used (figure 2.18).

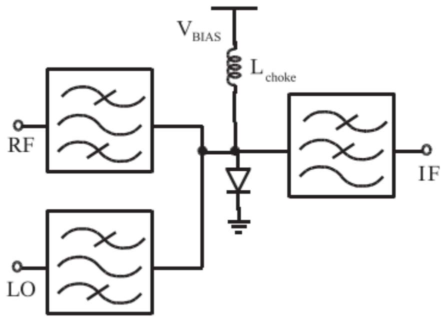


Figure 2. 17: Single diode mixer schematics with filters at the RF, LO and IF ports.

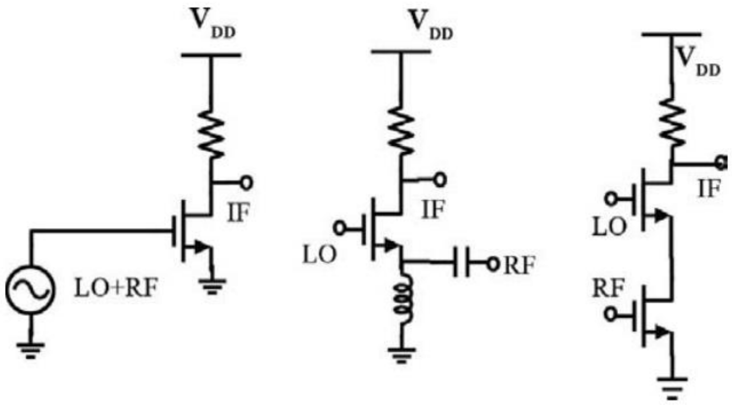


Figure 2. 18: CS, CG and cascode (or dual-gate FET) mixer topologies.

Generally, as it is shown in the above figures, filters or duplexers and an inductive choke (large inductor) are employed to provide isolation between the port signals and between the port signals and the power supply.

Mixers can also be categorized in balanced and unbalanced topologies.

Unbalanced (or single-ended) is a mixer that simply achieves the multiplication of two signals, but in the output co-exist significant levels of the input signals. It consists only of one mixing device (transistor or diode) and, also, a switch or diplexer to separate LO and IF signal. LO and IF inputs are followed by two bandpass filters, with LO and IF center frequency each, and both inputs are single ended, as the RF output too.

Examples of unbalanced mixers are topologies with single input ports and with no use of baluns or any other balancing circuit.

Single balanced mixers include a single balun at the LO port to provide isolation between the LO and the output port (RF for upconverters), figure 2.19(a). Thus, the LO input is differential, the RF output is also differential, but the IF input is single ended. Theoretically, single balanced mixers consist of the two single ended mixers. An important drawback of single-balanced mixers is the LO-IF feedthrough. The emitter coupled differential pair, for example, of figure 2.19(b), acts as an amplifier for the LO signal and, if the IF frequency is not much lower than the LO frequency, then LO may not be adequately suppressed by the lowpass filter at the IF output, without, also, attenuating the IF. As a result, the large LO content may desensitize the IF amplifier [17].

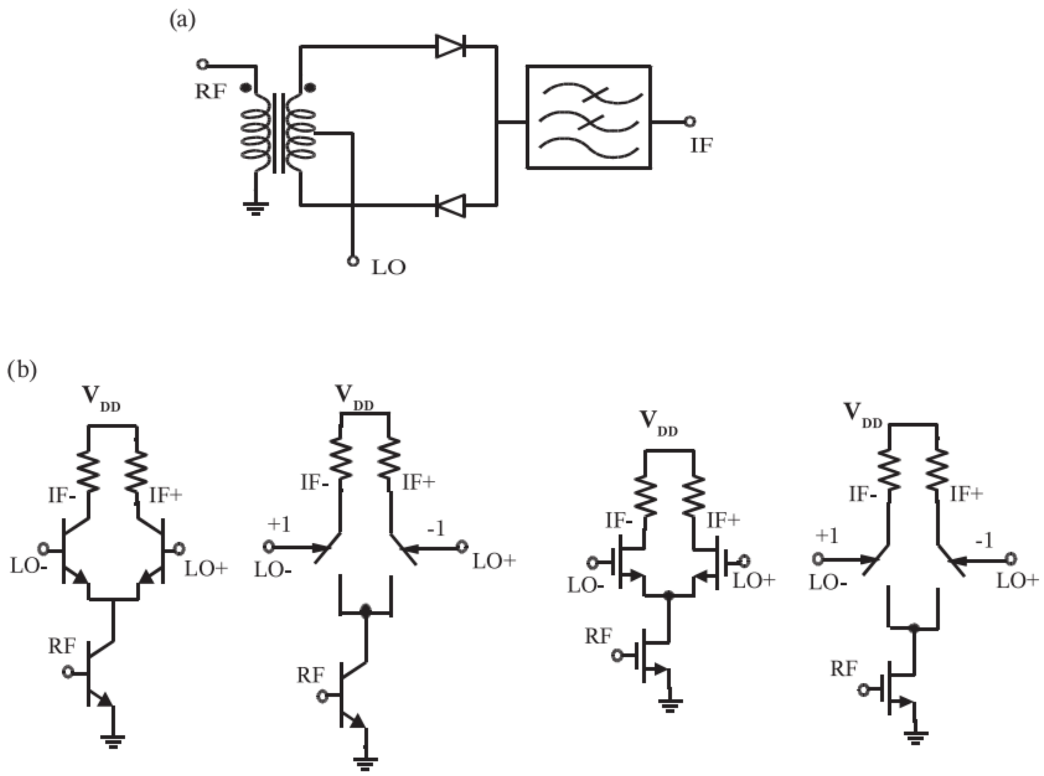


Figure 2. 19: (a) Single-balanced diode and (b) BJT/HBT and MOSFET mixer implementations and their conceptual equivalent circuit with anti-phase switches controlled by the LO signal.

Double balanced mixers provide high level of LO-RF isolation and LO-IF isolation and it provides a reasonable level of RF-IF isolation. The most traditional topology employs four Schottky diodes in a quad ring configuration (figure 2.20). Although single-balanced and double-balanced mixers were first implemented with diodes, the most common double-balanced topology today is the Gilbert cell.

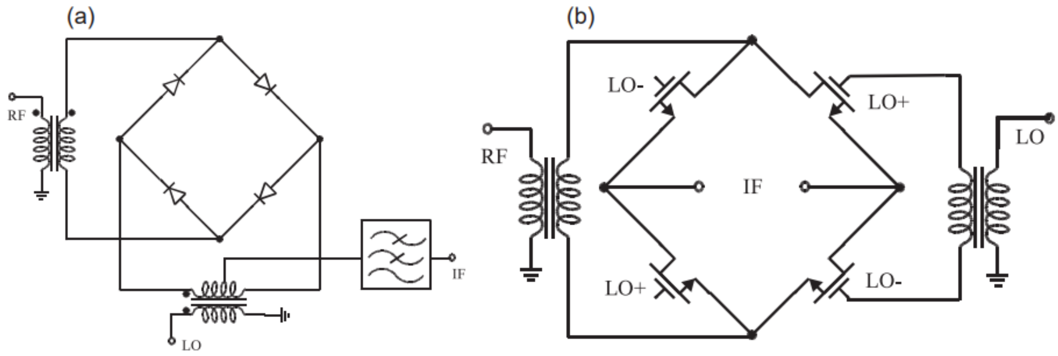


Figure 2. 20: Double-balanced (a) diode and (b) resistive FET mixer topologies

2.7 Gilbert cell

The gilbert cell mixer or multiplier is a very common topology in integrated circuits, first used by Barrie Gilbert. It is a double balanced mixer, which means, according to the previous paragraphs, that is able to remove unwanted LO and IF output signals from the RF output, due to the symmetrical topology it employs. The gilbert cell consists of a switching quad formed by two, cross-coupled differential transistor pairs preceded by a differential voltage-to-current converter (or transconductance) which also acts as gain stage. The above is illustrated in figure 2.21.

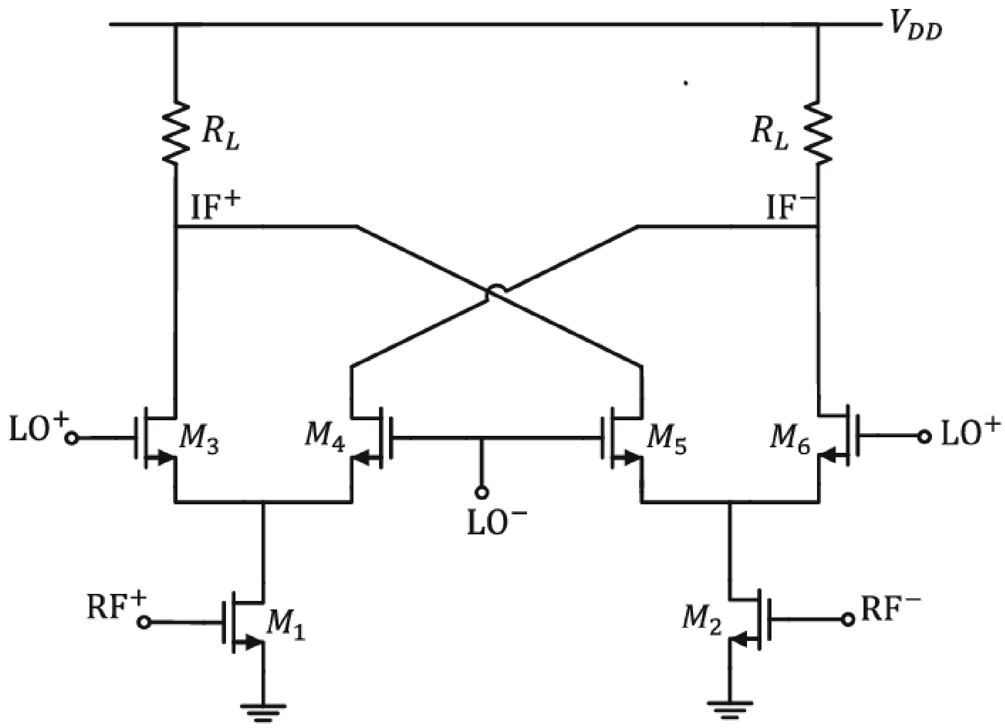


Figure 2. 21: Downconverter RF mixer in gilbert cell topology

M1 and M2 form the transconductance stage and M3-M6 the switching quad.

Typically, the input from the local oscillator has an amplitude greater than 4Vt ≈ 100 mV. With this large an input, the transistors M3-M6, in figure 2.21, quickly switch from their active to the off regions and vice versa, thus transistors act as fast switches. The amplitude of the lower stage M1-M2 can also be large, but proper operation of the mixer is also obtained for small amplitudes.

In essence, the transconductance stage converts RF input voltage signal to current signal. The current signal is then fed into the switch core of M3-M6 which turns ideally on and off at a frequency of LO drive, resulting in the desired IF current [18].

The gilbert cell theoretically consists of two single-balanced mixers or four single-ended mixers and is a fully balanced circuit that can be successfully used as a mixer of multiplier within RF integrated circuits.

Comparing to other mixing topologies, such as the diode ring, the gilbert cell-based mixer has the positive that requires lower LO-signal power and provides higher conversion gain [19]. Therefore, the proposed design is based on double-balanced Gilbert cell mixer [20].

2.8 Modulator and Image Rejection

As discussed in previous sections, modulators are commonly used to cancel out the unwanted mix products and more specifically, the image signal. To achieve this, the modulator utilizes phasing techniques, with the use of two balanced mixers and the quadrature (90°) hybrids as shown below.

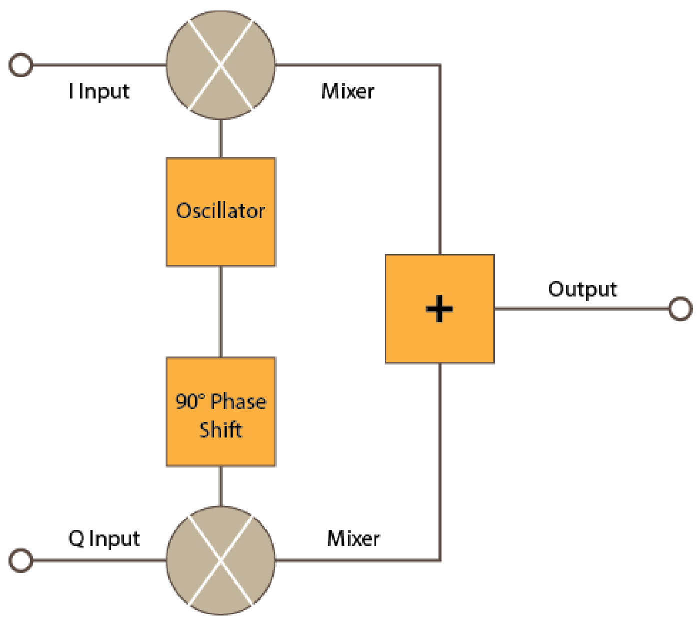


Figure 2.22: A modulator's representation consisting of two mixers in quadrature.

The two balanced mixers within the image reject mixer are driven in quadrature by the IF signal. The LO drive to each mixer is also 90 degrees shifted and the output is combined by the outputs of both mixers.

Perfect cancellation in practice is not possible as it requires identical mixers, perfect phase shift of the quadrature products and perfect amplitude balance.

However, modulators have some disadvantages, such as higher power consumption, due to two mixers employed, image rejection is frequency dependent and conversion gain is decreased comparing to a regular mixer, because the losses include the loss of the image too.

CHAPTER 3: B11HFC TECHNOLOGY [12], [15]

Infineon Technologies' B11HFC technology was used to build this modulator. It is a $400GHz/130nm$ SiGe BiCMOS technology with copper metallization for analog and mixed signal mmWave applications, which provides high performance and at the same time low power consumption. This SiGe BiCMOS technology combines the technologies of two different types of transistors, bipolar and CMOS, in the same integrated chip. HBTs offer high speeds and high gain, quantities very critical for analog components high frequency analog components, while CMOS technology, with its in turn, enables the implementation of low power logic gates. This unique combination offered by modern BiCMOS technologies opens up horizons for Si-based RF system-on-a-chip solutions.

The technology provides various devices and passive components such as npn transistors, metal-oxide-semiconductor (MOS) transistors, metal film resistors, metal insulator metal (MIM) capacitors, junction capacitors (metal film resistors), metal insulator metal (MIM) capacitors, junction capacitors, PIN diodes and microstrip transmission lines between the metal 6 and the metal 2 or metal 4. The vertical cross-section of the stack-up of the technology is shown in Figure 3.1.

As we can also see from the figure, technology provides us with six copper (Cu) layers, four thin (M1-M4) layers located at the bottom and two thick ones (M5-M6) located high up. In addition, above the six metal there is one layer (Alu) for the contact pads and for wiring.

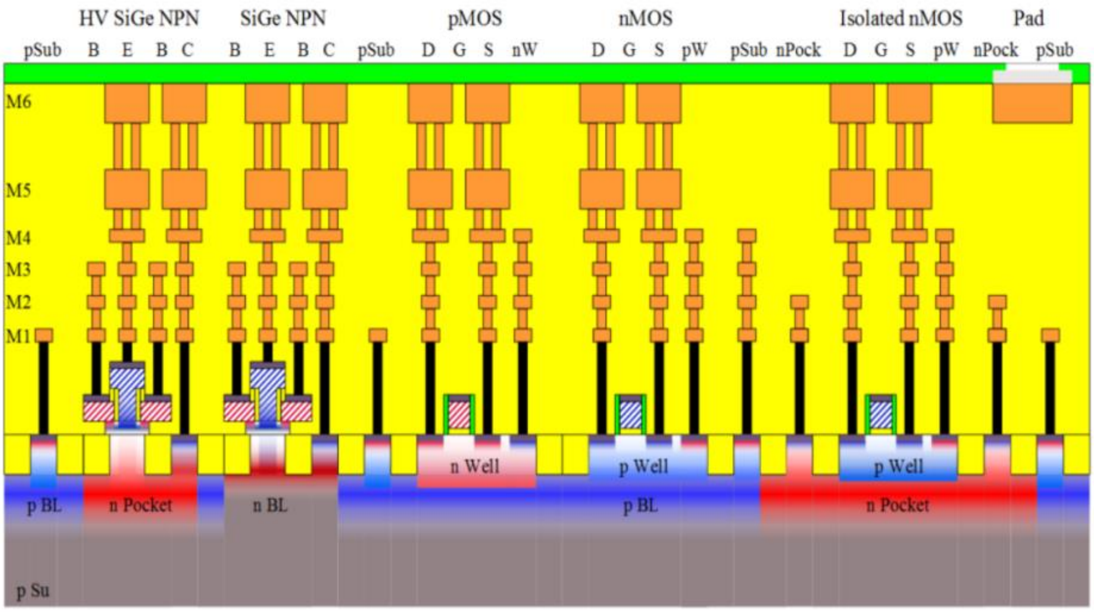


Figure 3. 1: 130nm SiGe BiCMOS B11HFC techology stack-up (Infineon Technologies)

3.1 High Speed HBT

For the mixer Heterojunction Bipolar Transistors (HBTs) were used as active, non-linear devices. FET and CMOS mixers are typically used in higher volume applications where cost is the main driver and performance is less important and as a result they were not used for this application.

Infineon Technologies AG's B11HFC technology provides a variety of npn SiGe Heterojunction Bipolar Transistors, which are the high speed npn, the medium speed npn and the high voltage npn. As the name suggests the high speed npn can reach much higher frequencies than the other two types. For example, the transit frequency f_T for the high speed npn is twice, or more, that of the others.

For this thesis, it is paramount to reach the higher possible frequencies, to achieve the 6G standard, thus only high speed npn transistors were used.

HBTs have two dimensions, the emitter length, which varies from 0,7 μm to 10 μm, and the emitter width, which varies from 0,22 μm to 0,34 μm. In order to find the real dimensions, the effective area A_{eff}, we subtract the mask area which adds 0,09 μm both lengthwise and widthwise.

In order to derive some basic characteristics of the high speed npn transistor of this technology, the following schematic was used figure 3.2.

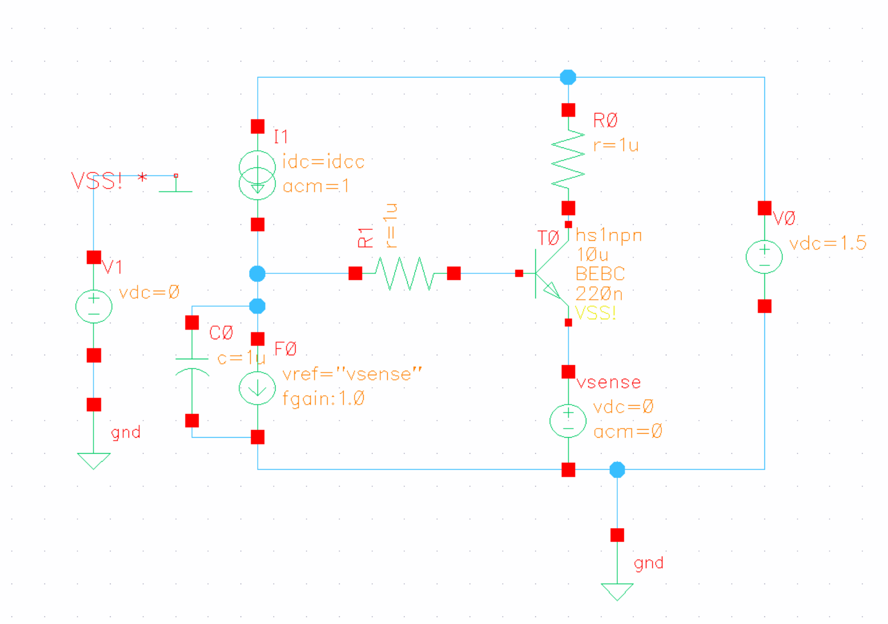


Figure 3. 2: Cadence schematic designed for hs HBT characterization.

For proper design it is advisable to have at our disposal, an estimate of the current density, for the optimal speed of the device. Figure 3.3 shows that, the highest unit frequency gain (transit frequency) f_T~280 GHz is obtained when the transistor collector is passed by a current density of about 14 mA/μm^2. It should be noted that transistor's models are frequently updated and, as a result, it is possible to have deviations from time to time.

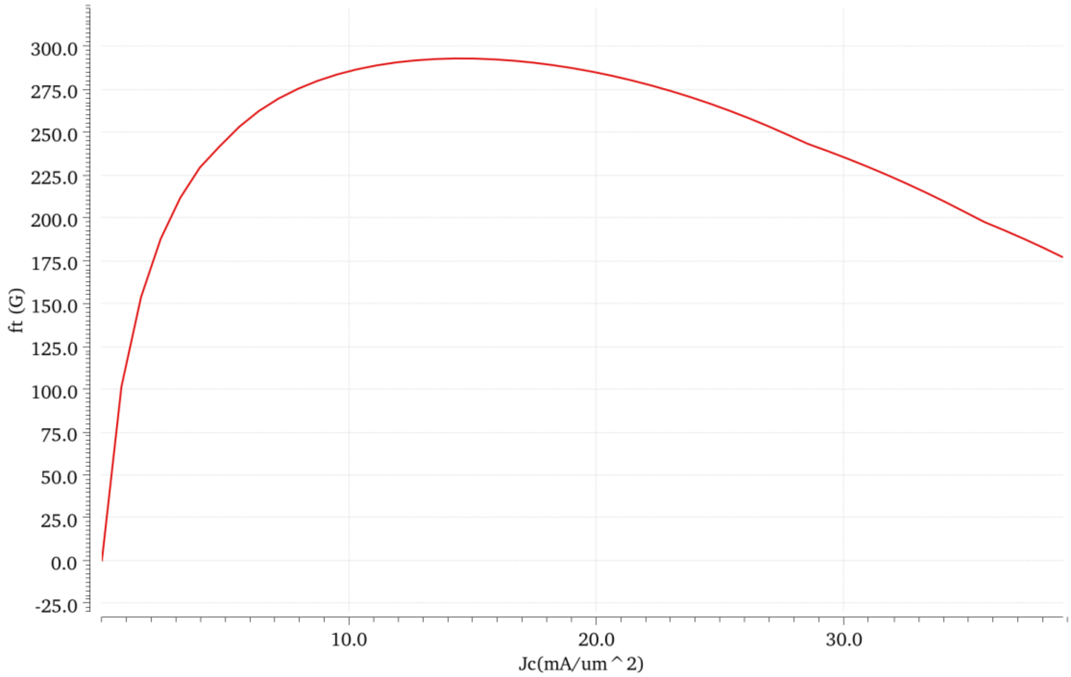


Figure 3. 3: F_T frequency versus collector's current plot for a high speed HBT of 0.22 x 10um^2 area.

Also, indicatively, the figure 3.4 of beta gain (β) versus frequency, was extracted.

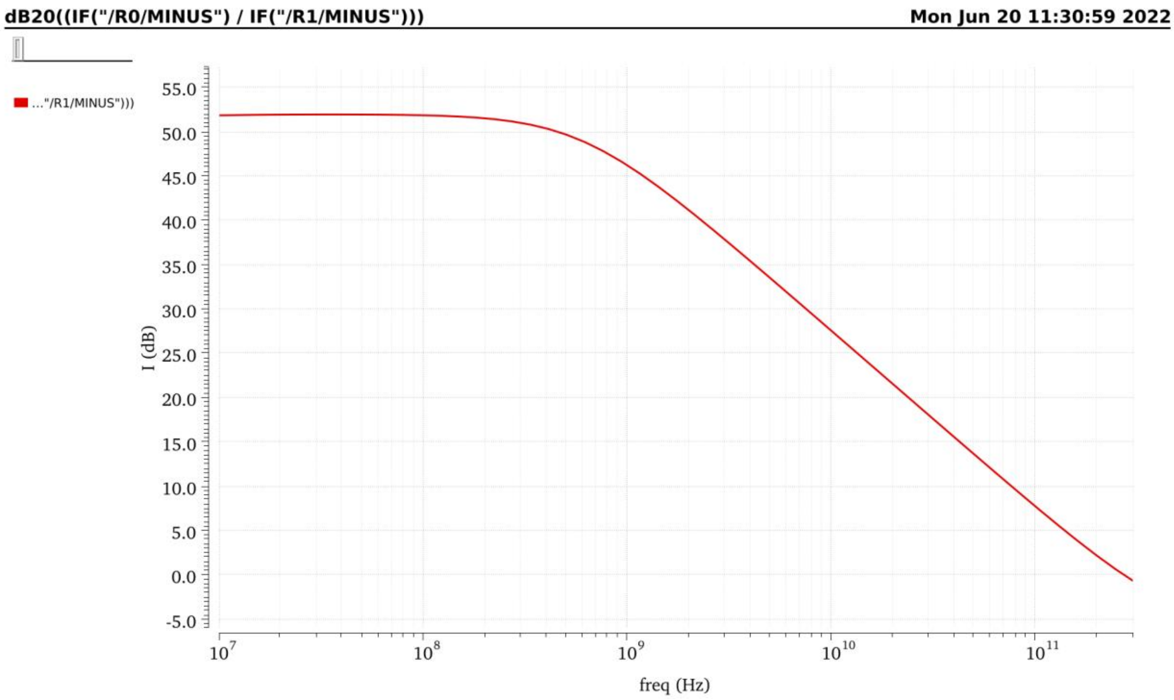


Figure 3. 4: Beta gain versus frequency plot for a high speed HBT of 0.22 x 10um^2 area.

Generally, the equation that connects the current density with the current at the collector of the HBT employs the effective area A_{eff} as seen below,

$$J_C = \frac{I_C}{A_{eff}}$$

3.2 MIM Capacitors

We randomly select a 100fF MIM capacitor from the library of and examine it for the dependence of its capacitance C and its quality factor Q versus frequency f. Figure 3.5 illustrates the Capacitance versus frequency plot, from which we can conclude that the capacitance of the MIM capacitor is inversely proportional to the frequency.

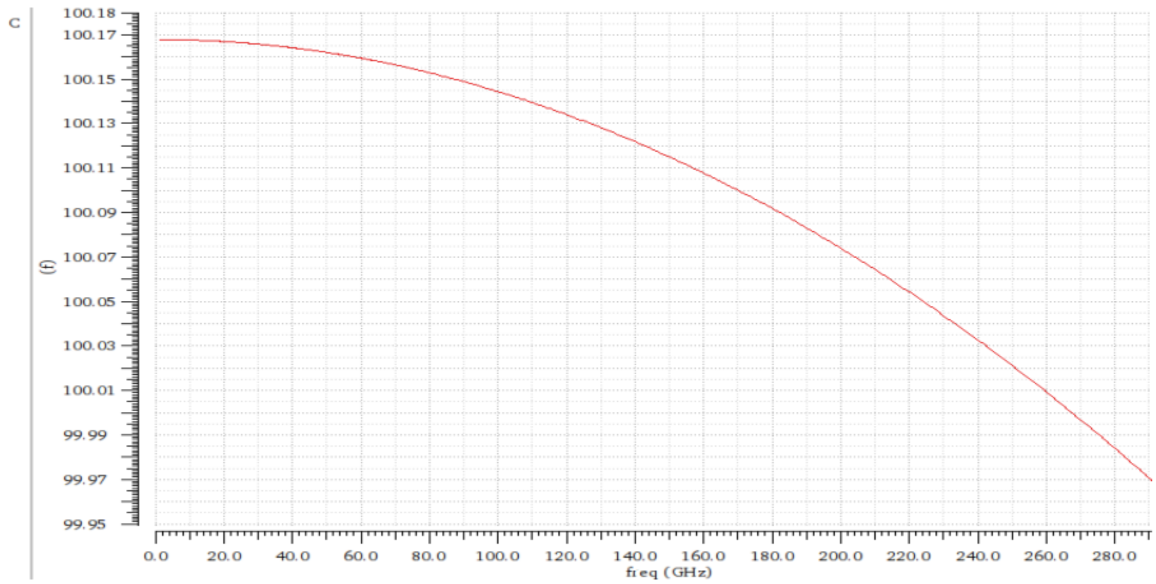


Figure 3. 5: Capacitance versus frequency of a MIM capacitor 100fF.

Figure 3.6 shows the Quality factor versus frequency plot, from which we can conclude that the quality factor of the MIM capacitor is inversely proportional to the frequency.

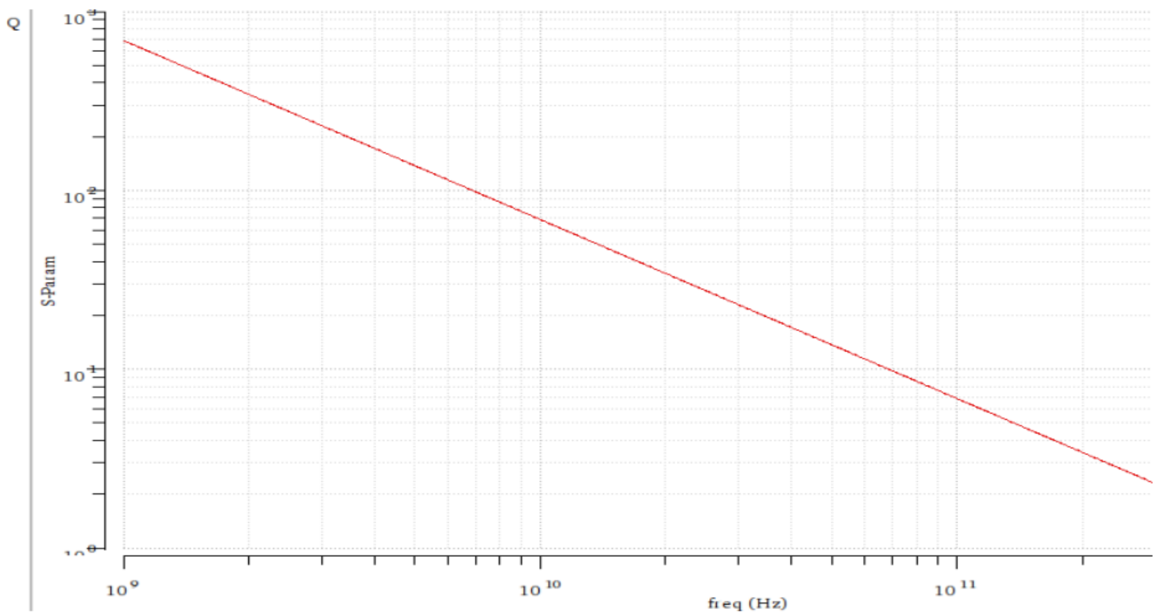


Figure 3. 6: Quality factor versus frequency of a MIM capacitor 100fF.

3.3 TaN Resistors

As shown in Figures 3.7 and 3.8 the TaN resistance models, like the MIM capacitor models, exhibit a frequency dependence. Their value versus frequency appears to change as if some parasitic capacitance is connected in parallel to the resistor. Furthermore, the performance of the resistors seems to depend on their dimensions, as resistors of larger dimensions seem to have a larger parasitic capacitance. Figure 3.7 shows the plot of the real part of a 200 Ω TaN resistor TaN versus frequency and Figure 3.8 shows the corresponding plot for the imaginary part of the resistor.

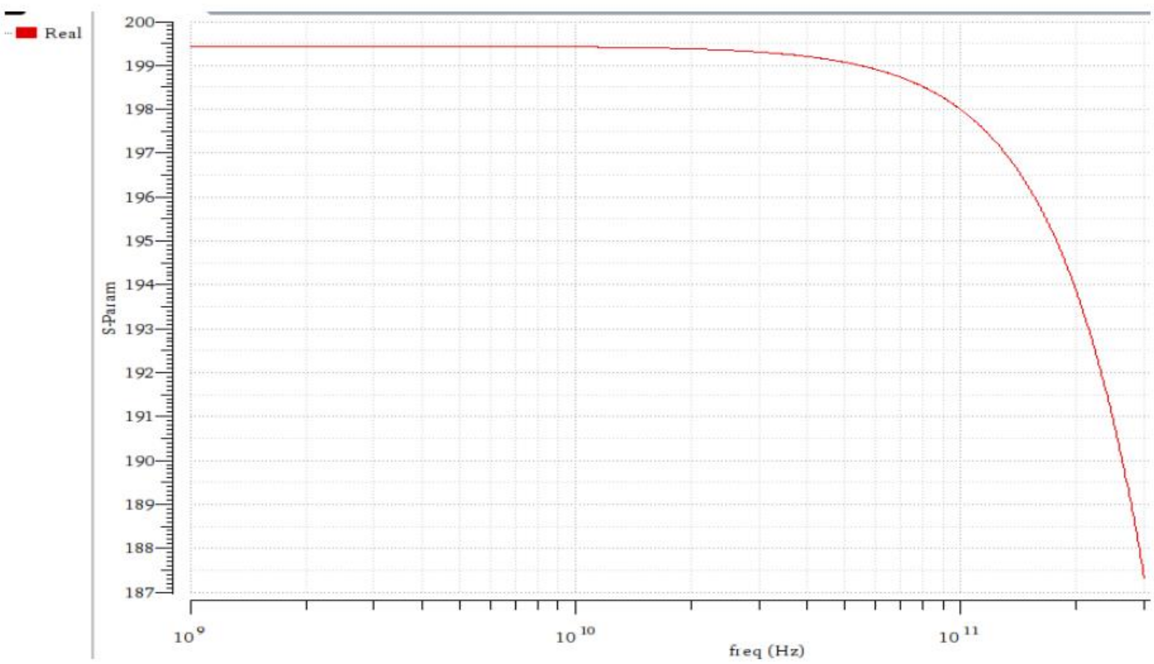


Figure 3. 7: Real part of a TaN resistor 200Ohm versus frequency plot.

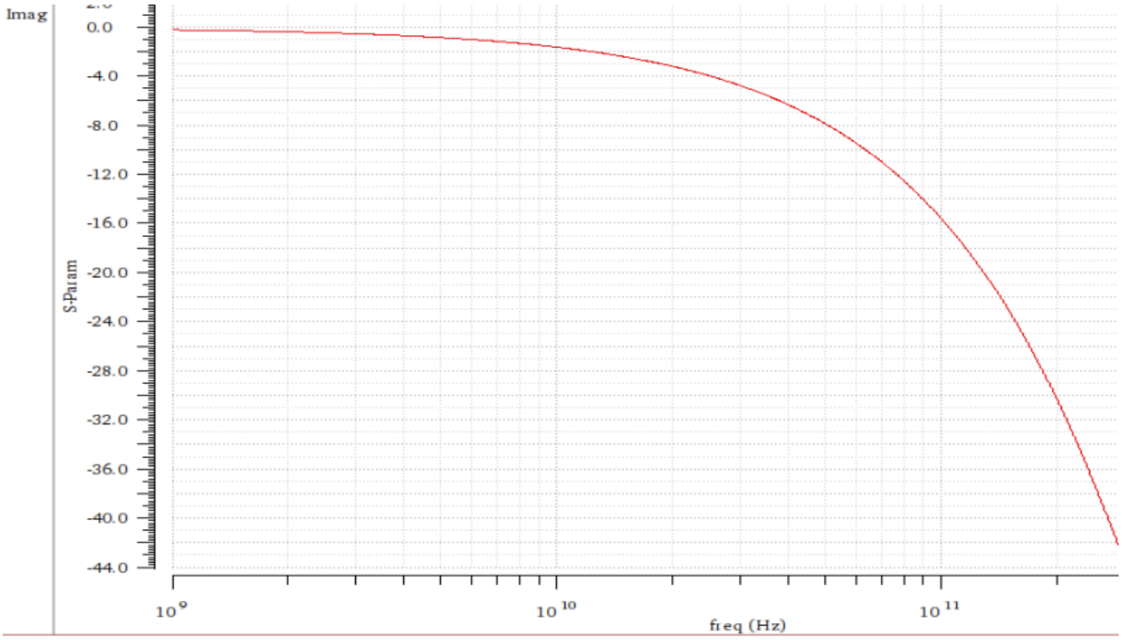


Figure 3. 8: Imaginary part of a TaN resistor 200Ohm versus frequency plot.

CHAPTER 4: SCHEMATIC DESIGN OF UP-CONVERSION MODULATOR

In this chapter the design of the up-conversion modulator, with 145GHz center frequency, is described. The design was carried out in the Virtuoso® environment of Cadence® while the mixer fabrication technology, is the B11HFC from Infineon Technologies. The specifications for this design, the design flow and an analysis of the technical obstacles encountered throughout the mixer synthesis process are attempted.

The design flow includes the following key points:

1. Establishing the specifications for the performance of the amplifier.

2. Selection of the transistors that characterize the active device of the mixer, based on the transistor models of the technology.

3. Design of the mixing circuit with ideal passive elements of the analog lib library and active HBTs of the technology.

4. Replacing the ideal passive elements with real models of the technology, designing input and output circuits and extracting graphical simulation results (Cadence Virtuoso® Spectre®).

5. Layout design, extraction of parasitic resistances, inductances, capacitances and mutual inductances in selected sections (RLCK extraction) and simulation of the layout in the electromagnetic simulation program ADS Momentum.

6. Extraction of graphical simulation results (Cadence spectre) of the EM simulated layout to characterize the performance and proper operation of the mixer.

7. DRC (Design-Rule Checker) and LVS (Layout versus Schematic) check.

The order of the above steps is not strictly the above but are iterated until the desired circuit operation is obtained.

4.1 Targets for mixer performance

For the mixer in this thesis, some operational limits were set for both to operate autonomously and to operate within the group project. These limits relate to the quantities that have been explained in detail in a previous chapter in terms of importance and functionality and are linearity, conversion gain, input/output matching, consumption and broadband. Nominally, these specifications are presented below.

- Key top-level specifications for the QDB Mixer:
  - IF Bandwidth: 1-20 GHz

- 3dB IF Signal Power dBm ~ -40 → -15 dBm
- LO Power ~ -5 dBm → 5 dBm
- 3dB RF Bandwidth: 30GHz (130GHz-160GHz)
- SSB Conversion Gain: 0 – 10 dB
- OP1dB > -18 dBm
- OIP3 > -7 dBm
- IRR > 20 dBc
- LO-to-RF isolation > 30 dBc
- Pdc < 100mW
- Terminations 100Ω

More specifically, in the context of the team project it was chosen that all port terminations be made at 50Ω and, therefore, differentially at 100Ω. Therefore, for all three input and output ports of the circuit, as differential, it was required to design matching networks at 100Ω, with extra caution to ensure LO to RF isolation higher than 30dB. Then, due to the requirements of this telecommunication application, the IF input signal bandwidth is from 1 to 20GHz, with signal power from -40dBm to -15dBm, and the LO bandwidth is required to be from 130GHz to 160GHz, with LO power from -5dBm to 5dBm. The above aim to achieve, approximately, an output RF bandwidth of 30GHz, from 130GHz to 160GHz. For the significant specification of conversion gain (CG) it is desired to achieve a value from 5 to 10 dB, and more strictly to be higher than 0dB. The 1dB compression point (output referred) needs to be higher that -18dBm, the 3rd order intercept point (output referred) higher than -7dBm and the image rejection ration (IRR) higher than 20dBc. Moreover, for the power consumption criterion, Pdc (mW), which, as is known, is required to be the minimum possible, an upper limit of 100mW was set.

The complete transmitter chain of the team project is presented below, in figure 4.1, with the mixing stage designed and implemented in the context of this thesis indicated by the red frame.

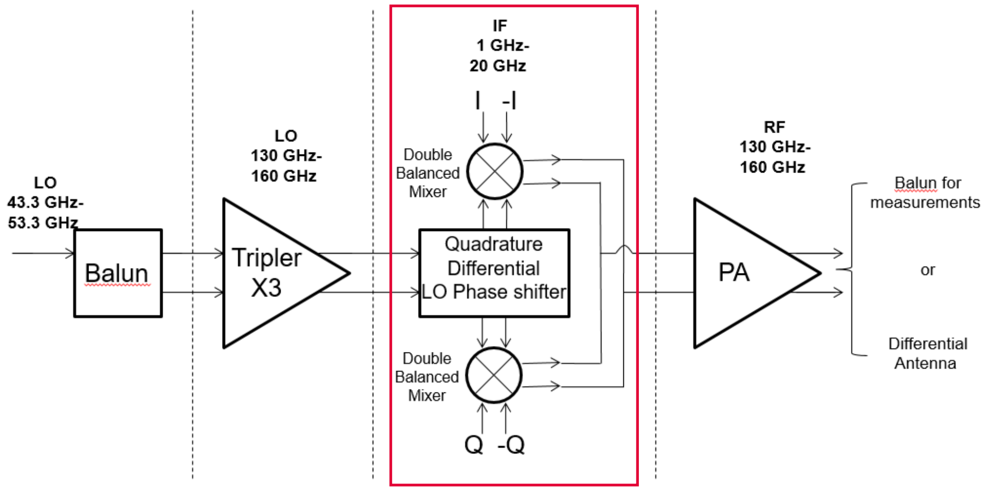


Figure 4. 1: Transmitter chain for short-medium range datalinks using PMF

4.2 Selection of the modulator core

In the following figure the gilbert cell mixer is presented in a simplified way.

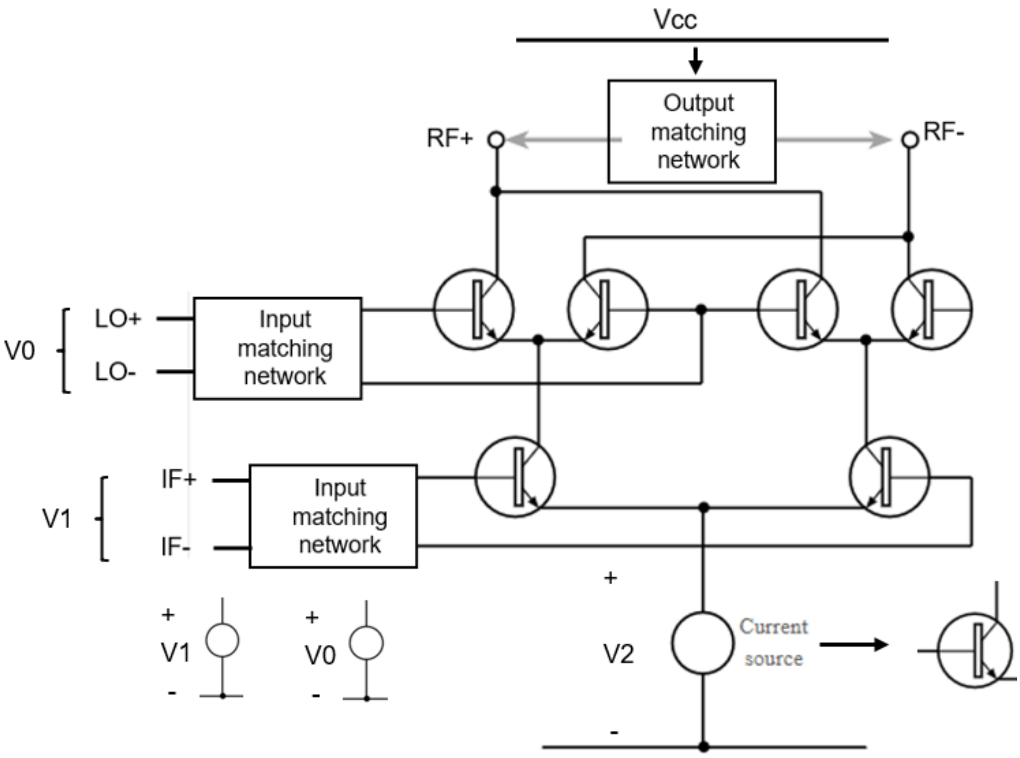


Figure 4. 2: Gilbert cell up-converting mixer.

First of all, the Vcc supply voltage is applied to the output matching network and the other dc voltage sources (V0, V1, V2) are applied at the base of the HBTs in order to properly bias the transistors. Secondly, the current source at the lower level of the circuit can be replaced by an HBT too, with proper dc voltage to its base. It does not receive an input signal at its base, as happens in the other stages, but this stage, the tail current stage, controls the flow of current to all branches.

In addition to the known gilbert cell, three matching networks are used, one for each port. It should be noted that all ports are differential, which is indicated by the plus (+) and minus (-) indexes in each port, LO, IF and RF.

4.3 Selection of the supply voltage

To begin with, the choice of the supply voltage level was decided based on the minimum required dc fluctuation, to ensure the proper biasing to all stages, but limited to not cross the power consumption specification. Due to the fact that the current of each branch is determined by the optimal current density J_{opt}, which implies the optimal performance of the HBT, power consumption can be mostly limited by the voltage level. However, this is not that a simple relationship, as dc level affects the quiescent current, which is proposed to have the J_{opt} optimal value. For the above reasons, the voltage level of 3.3V was chosen for supply voltage, suggested by b11hfc technology too, and with proper biasing adjustments, the optimal quiescent current can be achieved.

4.4 Selection of the active devices

As it was discussed earlier, in the previous chapter, the HBT that was used for this circuit was the high speed npn. Different emitter lengths were set for each stage, but the same emitter width, with the value of 0.22μm, was used.

According to figure 3.3 for the current density, it is suggested that for optimal operation the HBT should have a current density around 10 to 14 $mA/\mu m^2$.

However, not all stages have the same requirements. For the switching stage, as the name implies, transistors are biased near to pinch-off region to act as switches at LO frequency, from 130GHz to 160GHz. Thus, it is needed these transistors to have small dimensions and, of course, to use the high speed npn transistor model. Nevertheless, for the switching stage, it is suggested the transistors to be biased with current density that equals to $f_T/1.5$ at figure 3.3. In other words, not J_{opt}, but a smaller current density is desired.

Then, transconductance stage receives a slower input signal, the IF, from 1 to 20GHz and, also, this stage acts as current source for the switching stage, which means that the collector's current is split in two for the emitter coupled differential pair. As a result, these HBTs have bigger emitter length. For this stage the transistors are naturally biased for J_{opt}, that equals to f_T [2]. It should be noted that linearity is more important for the transconductance stage than for the switching stage because of the cascode structure [21] and, thus, larger dc currents are used to increase the current flow through this stage and the device operates in triode region.

4.5 Spectre simulations

In order to test the performance of the mixer, from the first to the last stage of design, a few analyses form the Virtuoso® Spectre® environment were chosen.

First of all, of course, the **DC analysis** was used, to provide information for the biasing of each stage, to check the quiescent currents, the region of operation and other metrics that describe the transistor's operation. The setup was simple and is presented below.

Secondly, in order to focus on the small signal analysis, the **harmonic balance (HB)** analysis was the most appropriate choice. It is a very efficient analysis for systems that have sinusoidal tones. However, as the tones become more non-linear, or real, the HB is getting slower because it enables more harmonics of each tone to describe the signals. The HB algorithm is flexible and calculates *the steady state solution* directly, by using the Fourier series. More specifically, as a frequency domain analysis, it first calculates the steady state of small signal frequency domain components and then on larger signals, which generate many new harmonic components.

Mixers are prime candidates for the use of harmonic balance analysis, among many others, that exploit non-linearities to achieve the desired performance.

The HB method is very efficient for simulating circuits such as low-noise amplifiers that have only low order harmonics. Mixers with a low moderate-tone power level can also be represented with low order harmonics. In general, problems related to multi-tone simulation in QPSS can be reduced in scope or even eliminated by using the HB method.

The set up used for the HB analysis is changed depending on the results that need to be extracted, enabling the sweep option for power sweeps of the IF (Piip3) and LO (P1) input power, figures 4.3 and 4.4.

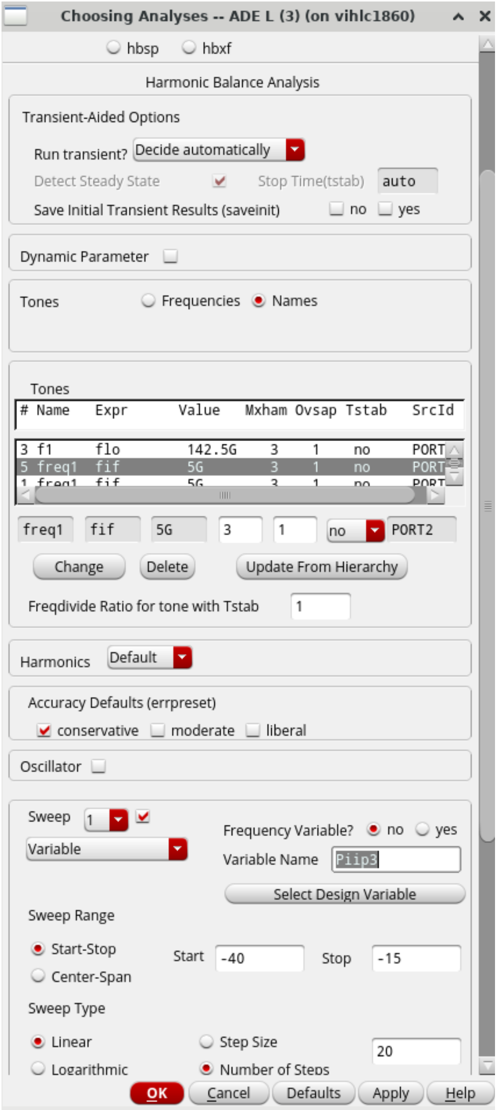


Figure 4. 3: HB setup with IF input power sweep on, for up-converting mixer.

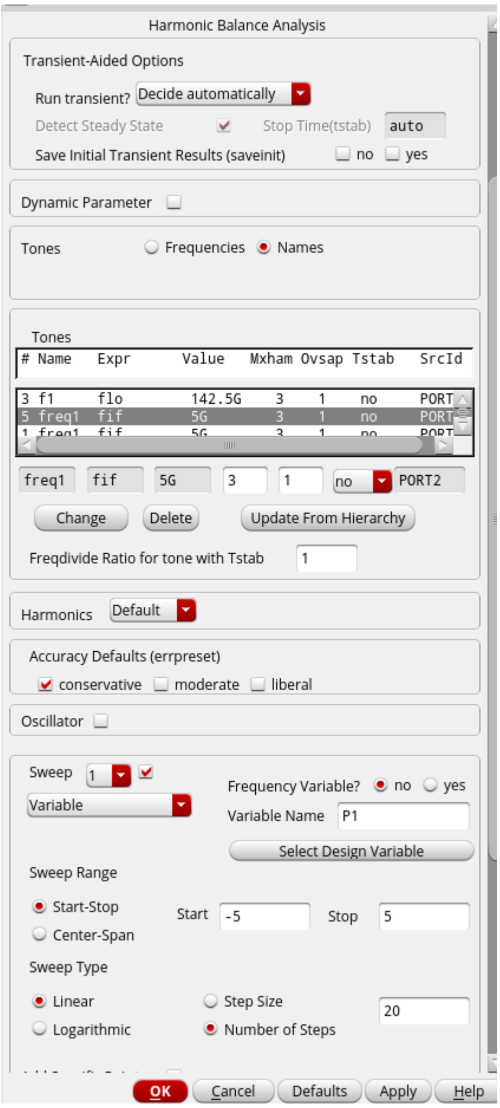


Figure 4. 4: HB setup with LO input power sweep on, for up-converting mixer.

Then, **transient** (tran) analysis was used to check the performance of the mixer on the time domain. More specifically, with tran both input signals are illustrated on time, to ensure that the desired waveform, amplitude and phase, is received by the HBTs' bases and, also, to check that the output waveform, amplitude and phase, is appropriate.

Finally, the **scattering parameters analysis** (sp) was significant in order to acquire the S-parameters that characterize our electrical network. Sp analysis was used, primarily, to design the input and output matching networks and extract the results of their final performance. In sp analysis the frequency range was set to 170GHz (from 1 to 170GHz).

4.6 Gilbert cell design

To begin with, a gilbert cell on b11 technology was designed, with ohmic load, of 500Ω, and without matching networks. For input and output ports we used ideal dc-feed inductors and dc-block capacitors from analoglib library. The schematic is illustrated below, figure 4.5.

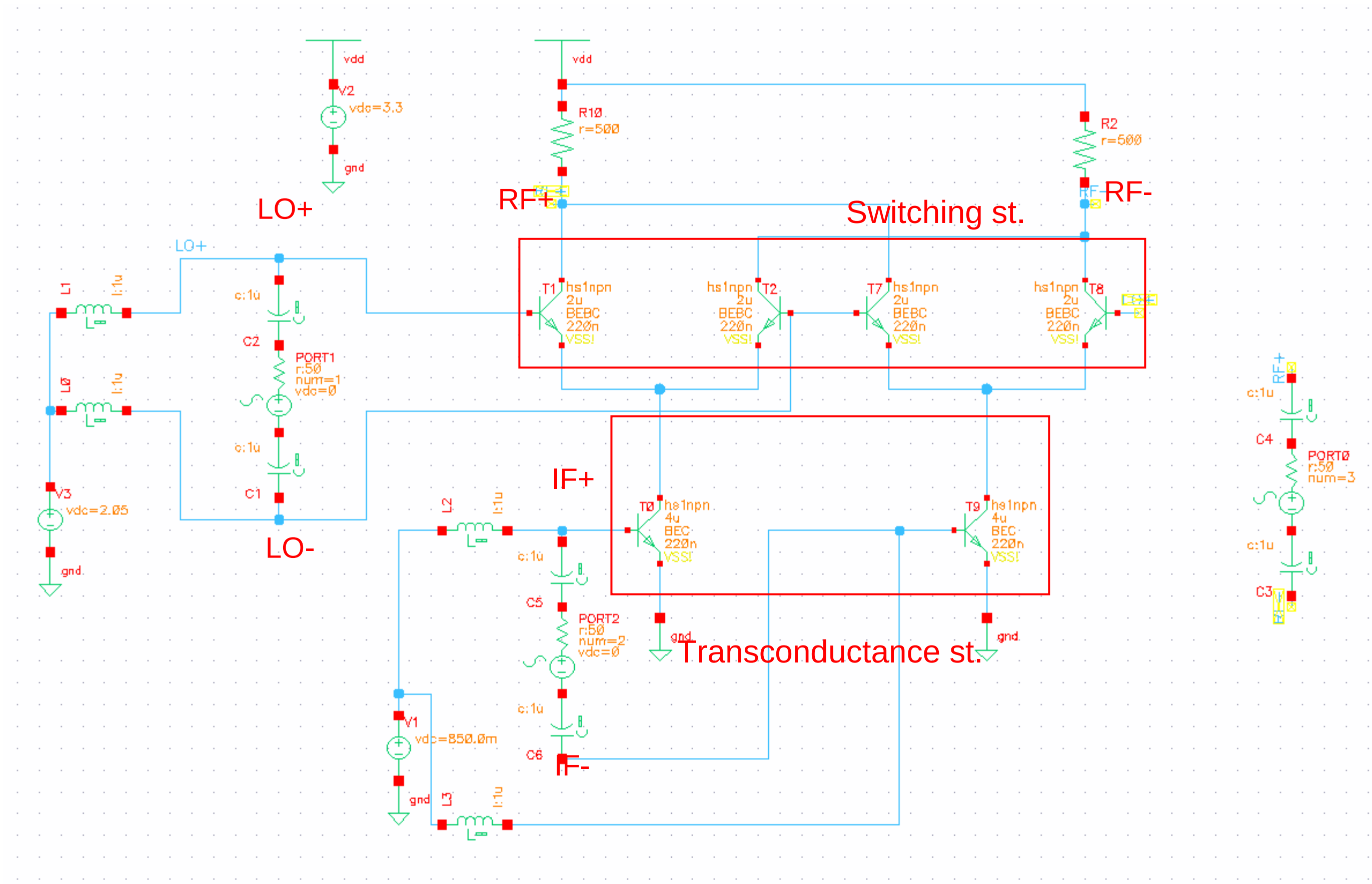


Figure 4. 5: Cadence schematic of an up-converting mixer, in gilbert topology, with ohmic load.

On this experimental design stage, the goal is to test this topology in combination with the capabilities of B11 technology. No significant conversion gain is expected, as this is a preliminary design without matching networks.

Indeed, with hb analysis the output spectrum shows that we have a conversion loss of 5dB, with -10dBm at the input and -15dBm at the output.

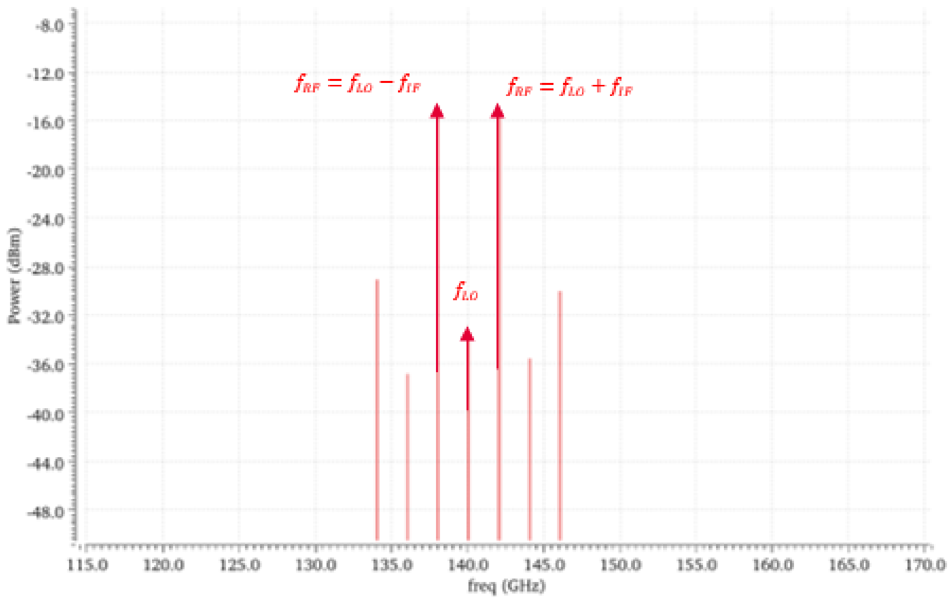


Figure 4. 6: Output RF spectrum for f_{IF} = 2GHz, P_{IF} = -10dBm, f_{LO} = 140GHz, P_{LO} = -5dBm

However, the above results indicate a proper function of the RF mixer, for example two output frequencies are generated, the $f_{RF} = f_{LO} - f_{IF}$ and $f_{RF} = f_{LO} + f_{IF}$, with the same level of amplitude. Many improvements should be made regarding the topology that will enhance the performance.

4.7 Mixer design

The next step is the following mixer in figure 4.7.

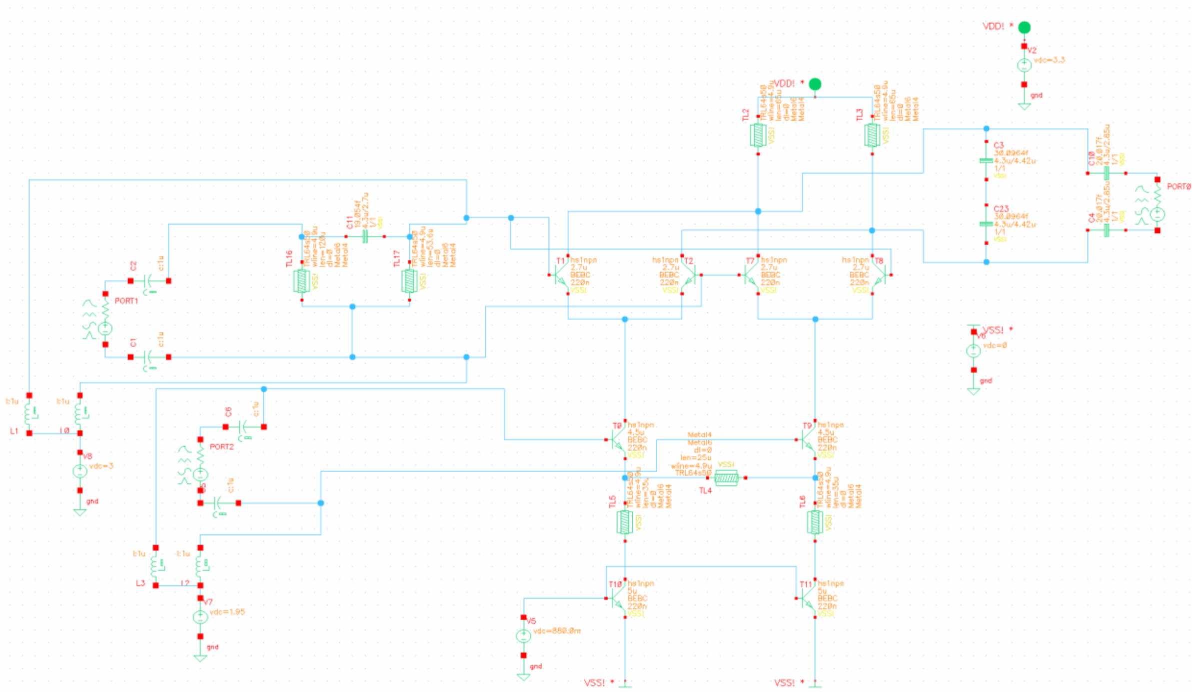


Figure 4. 7: Mixer schematic for sub-terahertz frequencies

In this schematic, a tail current was added, consisted of two HBTs with emitter length of 5um, or, alternatively, of one HBT with 10um emitter length, connected to both branches, to avoid mismatches.

The resistive load at the output is replaced with inductors, in order to amplify the achieved conversion gain [13], performing no significant dc voltage drop, that, also, increase power consumption. These inductors are part of the RF output matching network too, right up on the schematic. The LO input matching network is composed of an LC network, between the differential input. No baluns were needed for this design as all inputs and outputs are preferred to be differential.

For improved harmonic suppression and linearity, inductors in series and in parallel with the branches are added between the transconductance stage and the tail current.

Again, hb analysis was enabled for the graph generation, using the familiar setup. Figure 4.8 below show the spectrum of the RF output for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, P_{LO} = 0dBm.

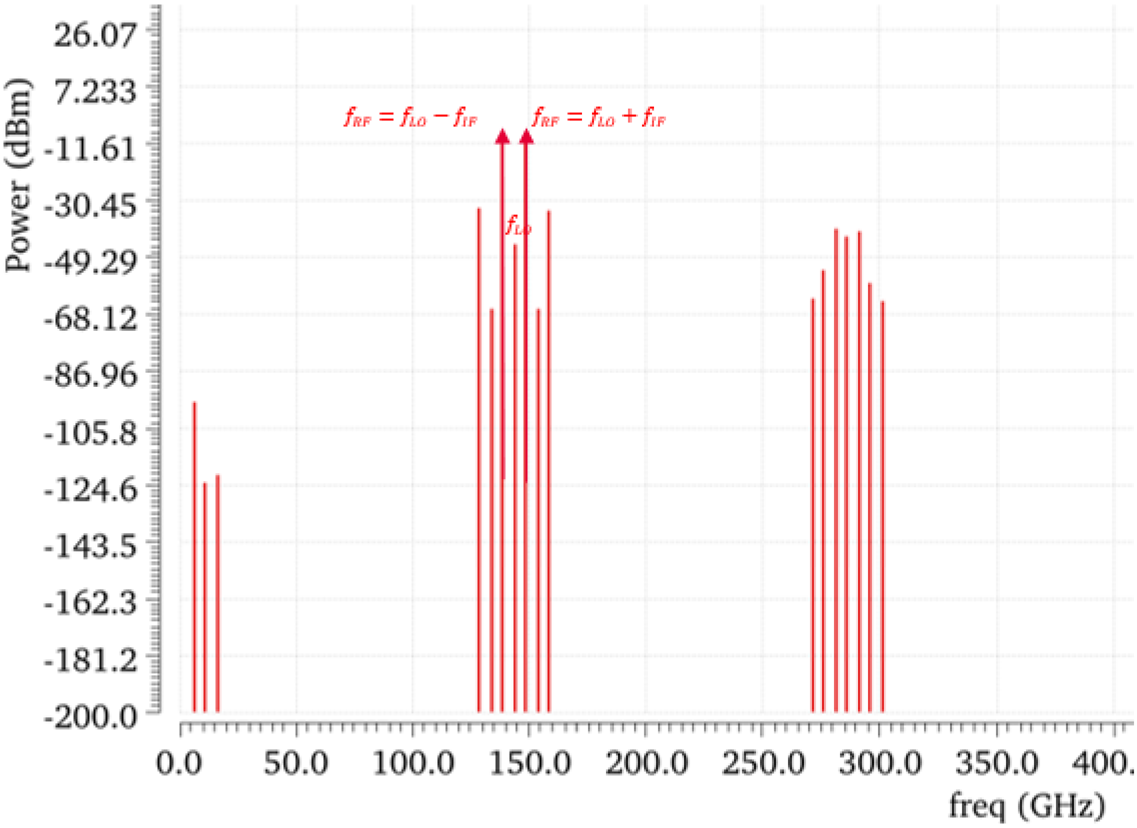


Figure 4. 8: RF Output spectrum for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, P_{LO} = 0dBm of the mixer

Then, we sweep the input IF power Piip3 from -40dBm to -10dBm and plot the output RF power versus input IF power, for LO power equal to 0dBm. The 1st order frequency at the output has to be chosen, which comes from the formula f_{LO} - f_{IF} = 137.5

GHz for lower sideband up conversion. This plot is presented below, in figure 4.9, notating the 1dB Compression Point too.

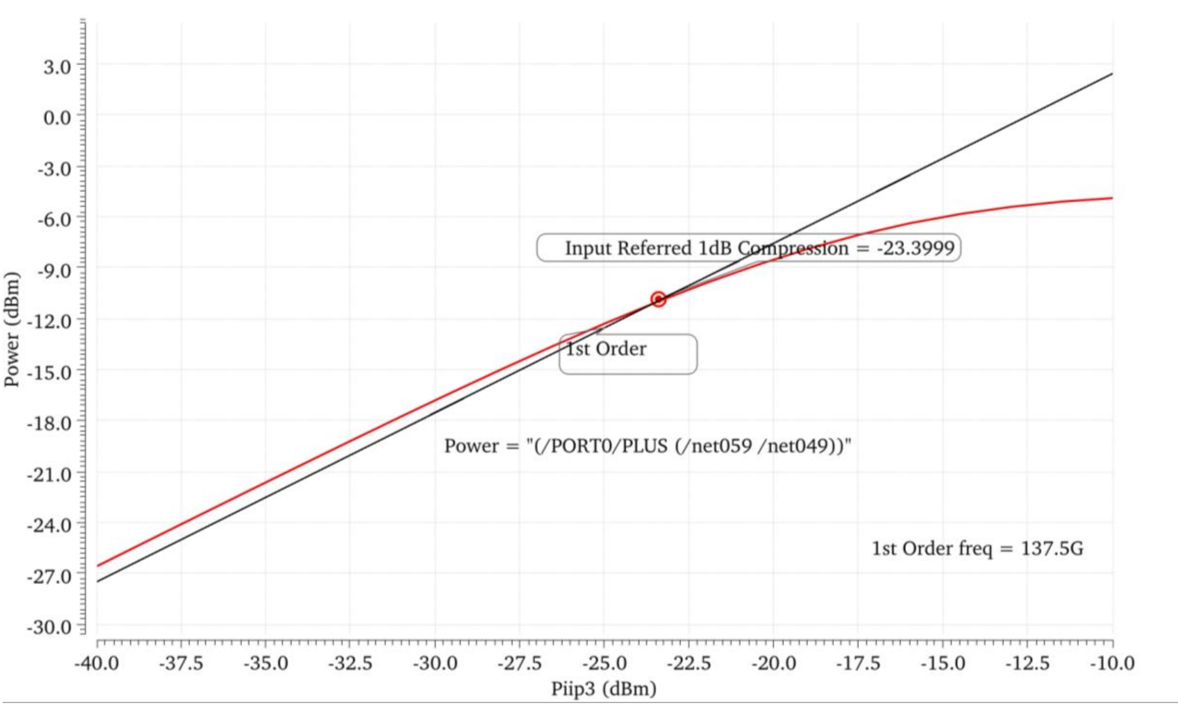


Figure 4. 9: Output RF power vs. Input IF Power with 1dB compression point equal to -23.4dBm, for f_{IF} = 5GHz, f_{LO} = 142.5GHz, P_{LO} = 0dBm of the mixer.

After the Compression Point curve, another simulation has to be run in order to plot the input referred 3rd order Intercept Point. In the IF setup another tone is added, with frequency very close to the first one, for example, f_{IFa} = 5GHz and f_{IFb} = 5.2GHz, with same power amplitude. The first tone will be set as large and the second as moderate at the HB menu. For this graph it is needed to specify the 1st and 3rd order frequency, which depends on the LO and IF frequencies.

The 1st order is coming from the relationship:

- $f_{LO} + f_{IFa}$ for upper sideband mixer and
- $f_{LO} - f_{IFa}$ for lower sideband mixer.

The 3rd order follows:

- $2^* (f_{LO} + f_{IFa}) – (f_{LO} + f_{IFb})$ for upper sideband mixer and
- $2^* (f_{LO} - f_{IFa}) – (f_{LO} - f_{IFb})$ for lower sideband mixer.

The result is the following figure 4.10.

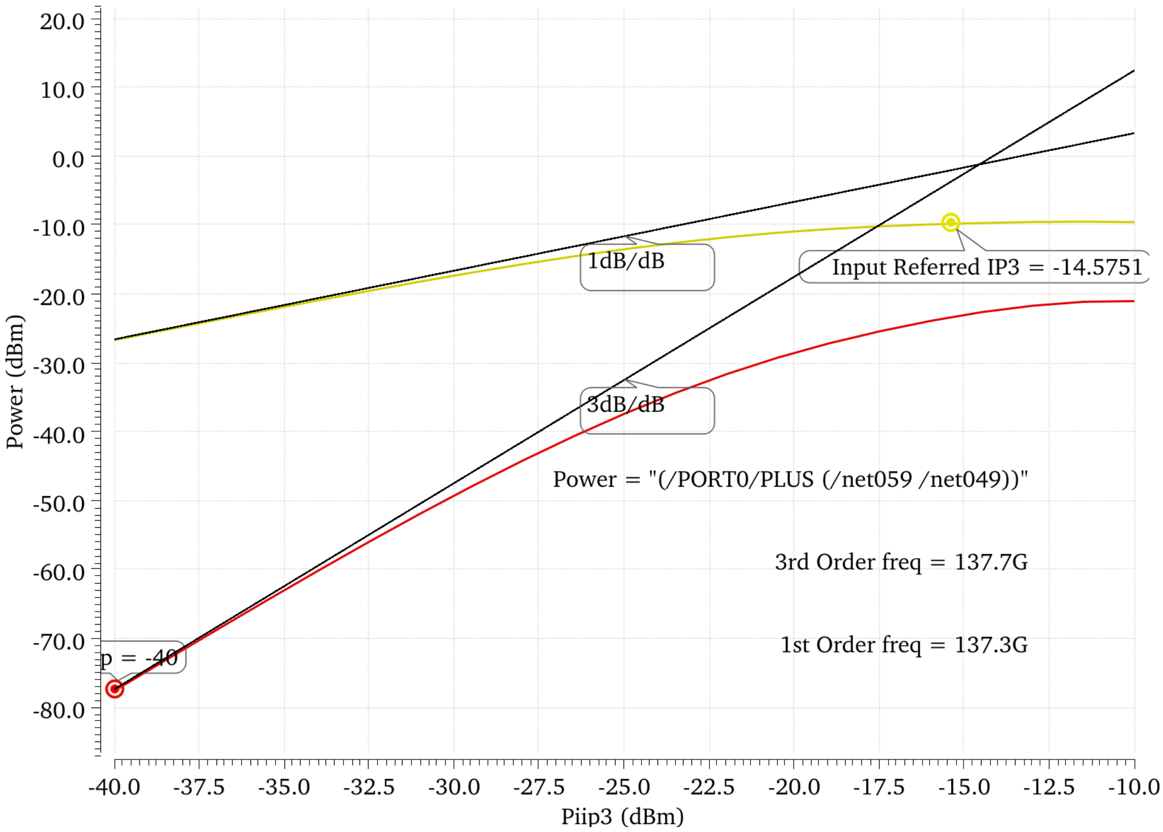


Figure 4. 10: RF output Power vs. IF input Power, IIP3 = -14.6dBm for the mixer.

4.8 Quadrature Double Balanced Mixer (QDB-Mixer)

The final up-converting topology is the modulator, consisted of two gilbert cell mixers, in quadrature operation, in figure 4.11.

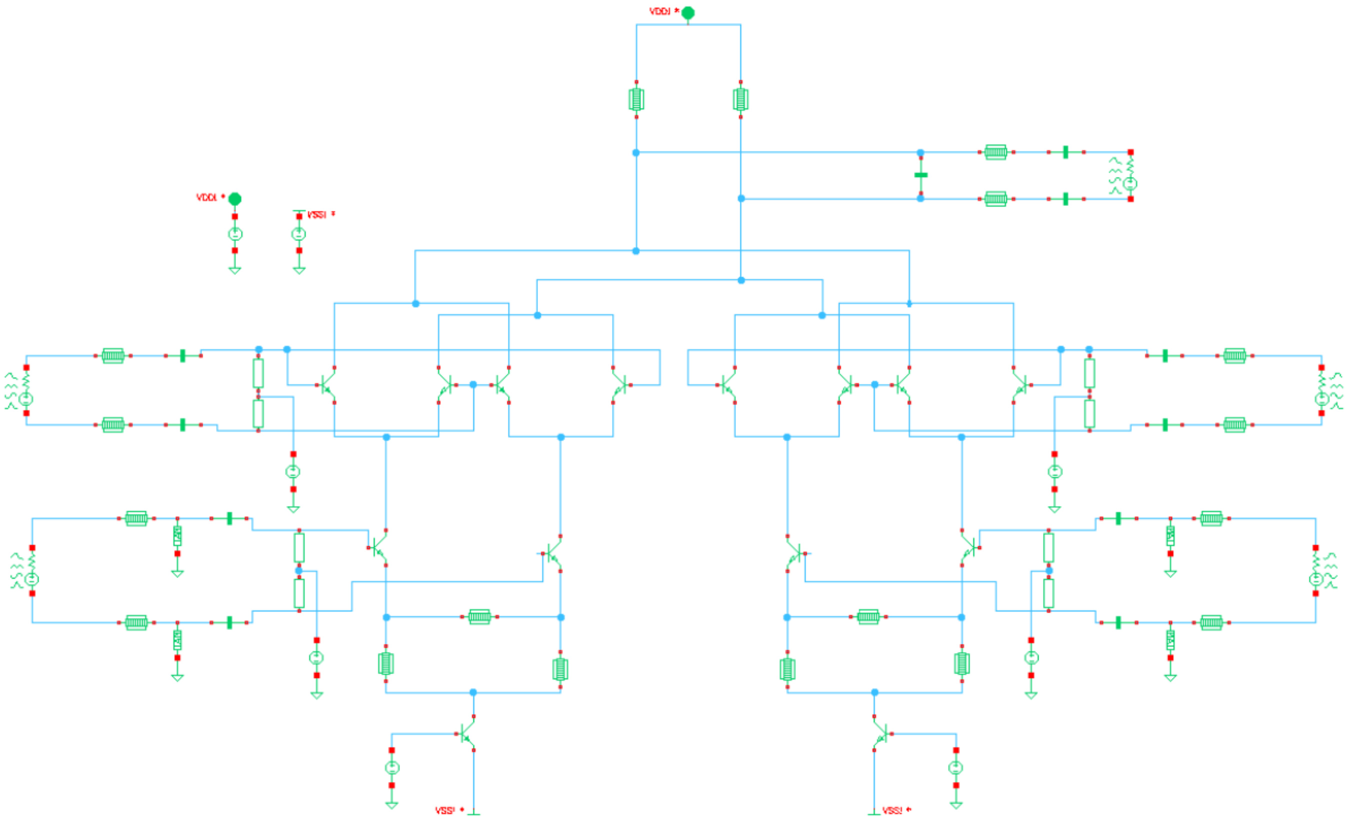


Figure 4. 11: Quadrature Double Balanced active Mixer based on gilbert cell topology

The two mixers operate in quadrature, modulating the differential I and Q signals with the differential LO_I (0^o phase) and LO_Q (90^o phase) signals respectively [22]. The topology of each mixer (I and Q), in quadrature, is the same with the mixer design described in the previous section. The switching stages consist of two emitter-coupled pairs [13] each with emitter mask lengths equal to 2.7um, the transconductance stage 4.5um and the tail current, consisting of one transistor, 10um. All transistors have the same emitter width of 0.22um. Vbias for switching stage is 2.9V, for transconductance stage 1.85V and for the tail current 0.88V resulting in a V_{BE} of around 0.88mV for the switching and transconductance stage, providing the 5.047mA and 10.12mA respectively. It is noteworthy to mention that the vbias of the tail current stage determines Vbe of all stages, through the quiescent current that is evolved. All voltage sources are chosen in a way to achieve optimum current densities, analyzed in section (selection of active devices).

For the modulator to operate properly and to ensure the image rejection [5], input signals have to be received in a specific way. If the upper sideband is the desired signal at the output, and assuming that I mixer has IF (0 degrees) and LO (0 degrees), differentially, then the Q mixer needs IF (90 degrees) and LO (270 degrees), or IF (270 degrees) and LO (90 degrees), differentially. If the lower sideband is needed, the Q mixer needs IF (90 degrees) and LO (90 degrees), figure 4.12. Generally, I stands for IF in 0 degrees and Q for IF in quadrature, 90 degrees. For the output, the positive output of the I mixer is connected to the positive output of the Q mixer and same for the negative output. As a result, the modulator has one differential RF output shared by the I and Q mixers.

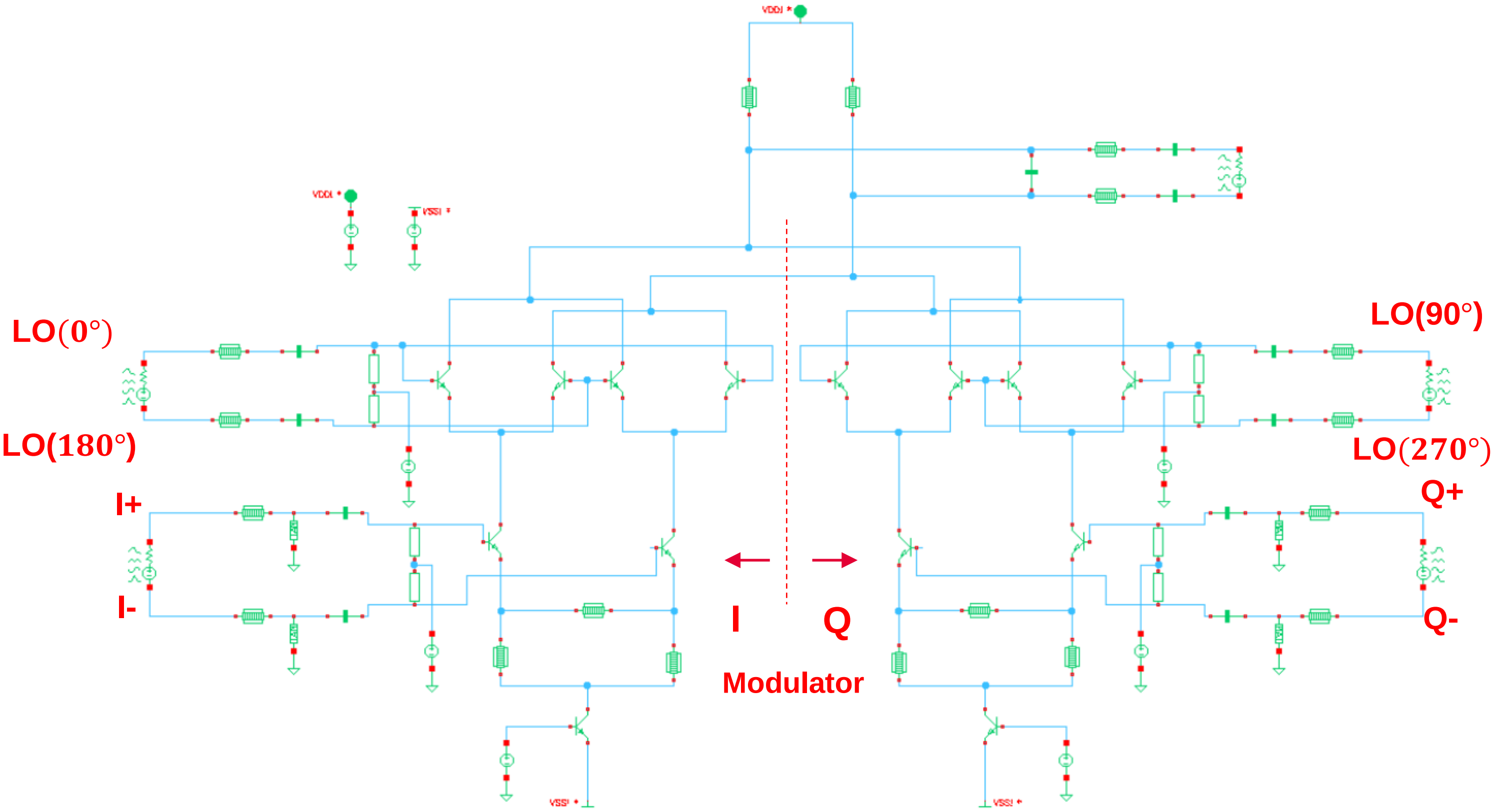


Figure 4. 12: Lower Sideband Up Conversion Modulator

4.9 Modulator Simulations

For all the following simulations, a temperature of $\mathbf{T = 45}$℃ was selected.

Using hb analysis the following plots were generated. Figure 4.13 below show the spectrum of the RF output for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, P_{LO} = 0dBm.

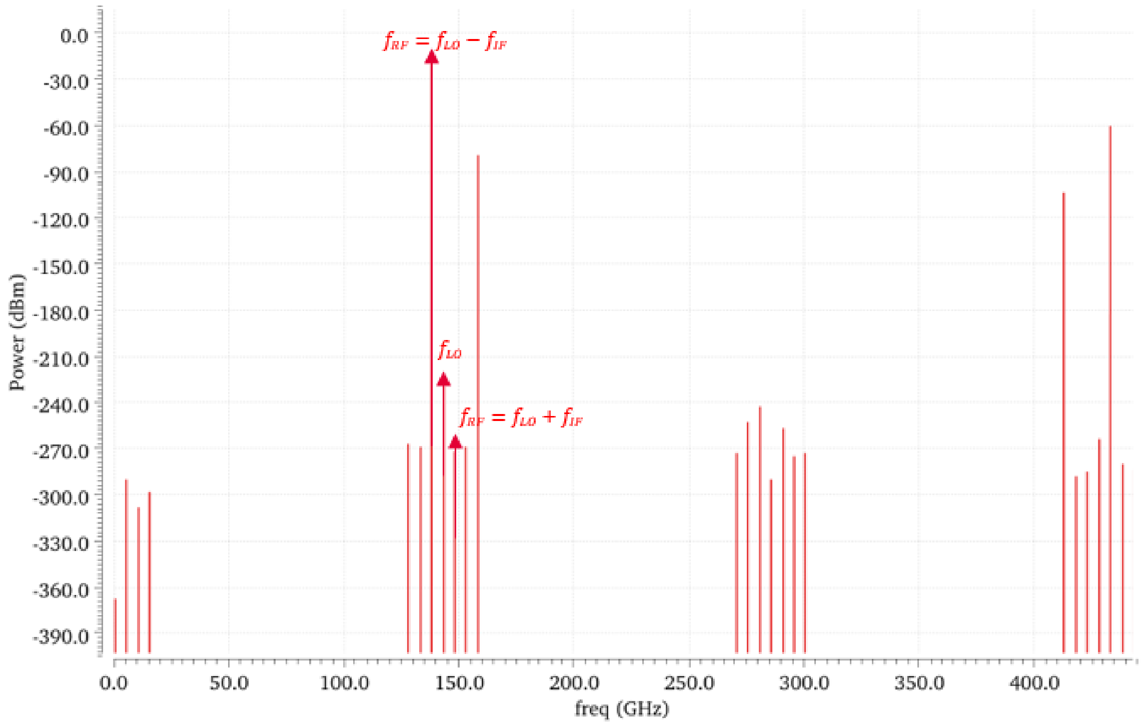


Figure 4. 13: RF Output spectrum for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, P_{LO} = 0dBm of the LSB modulator.

Then, we sweep the input IF power Piip3 from -40dBm to -10dBm and plot the output RF power versus input IF power, for LO power equal to 0dB, as shown in figure 4.14. The 1st order frequency at the output is set again at 137.5 GHz, as for the mixer. The input referred 1dB Compression Point has a value of – 14.2dBm approximately, accordingly to the specifications.

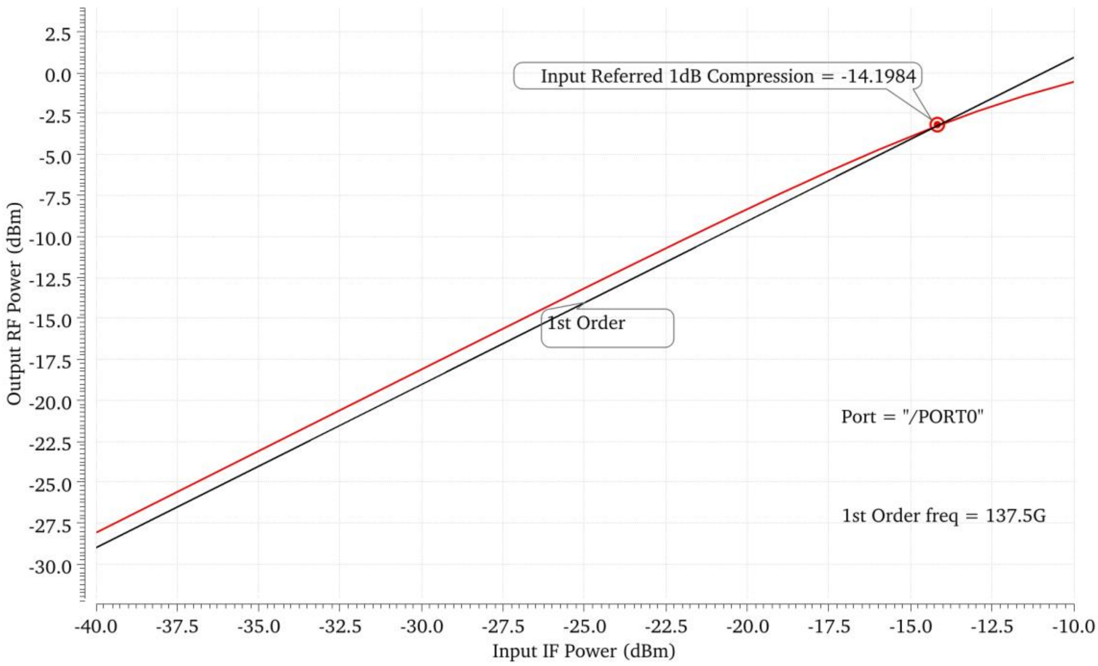


Figure 4. 14: Output RF power vs. Input IF Power with 1dB input referred compression point equal to -14.2dBm, for f_{IF} = 5GHz, f_{LO} = 142.5GHz, P_{LO} = 0dBm, of the LSB modulator.

Then, the conversion gain is plotted, setting the input IF frequency and the output frequency the modulated f_{LO} - f_{IF} = 137.5 GHz, for lower sideband up conversion.

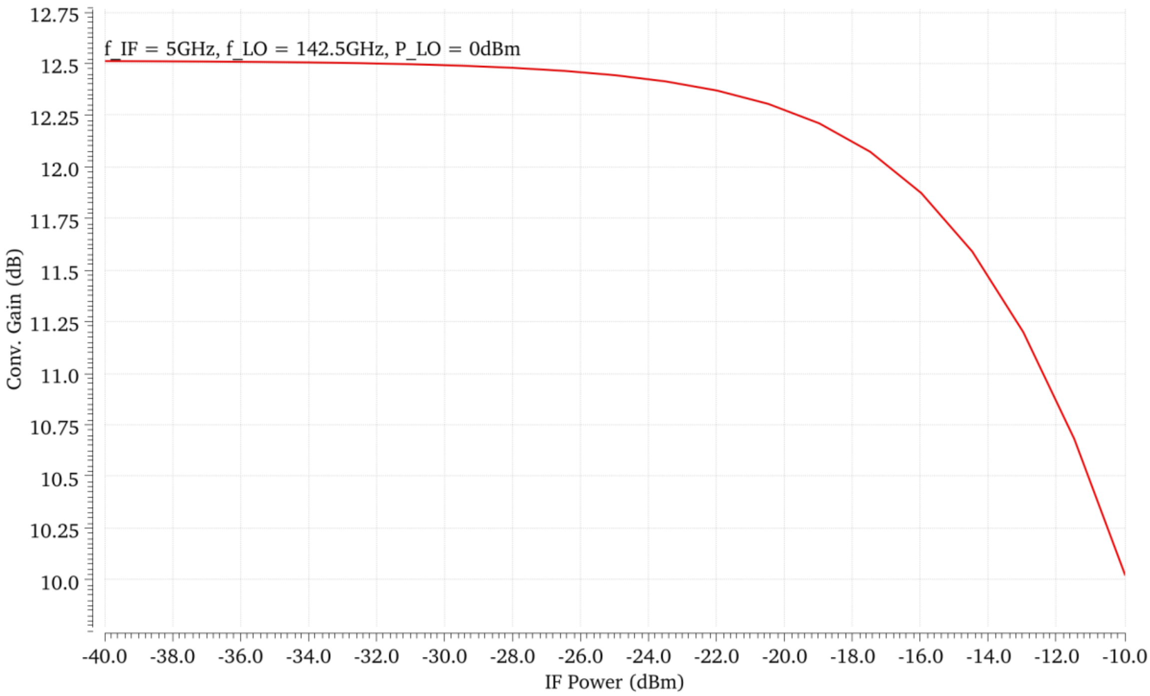


Figure 4. 15: Conversion Gain vs IF input Power for fIF = 5GHz, fLO = 142.5GHz, PLO = 0dBm, of the LSB modulator.

Same as previously, we sweep the input LO power P1 from -10dBm to 10dBm and plot the output RF power versus input LO power, for IF power equal to -30dBm.

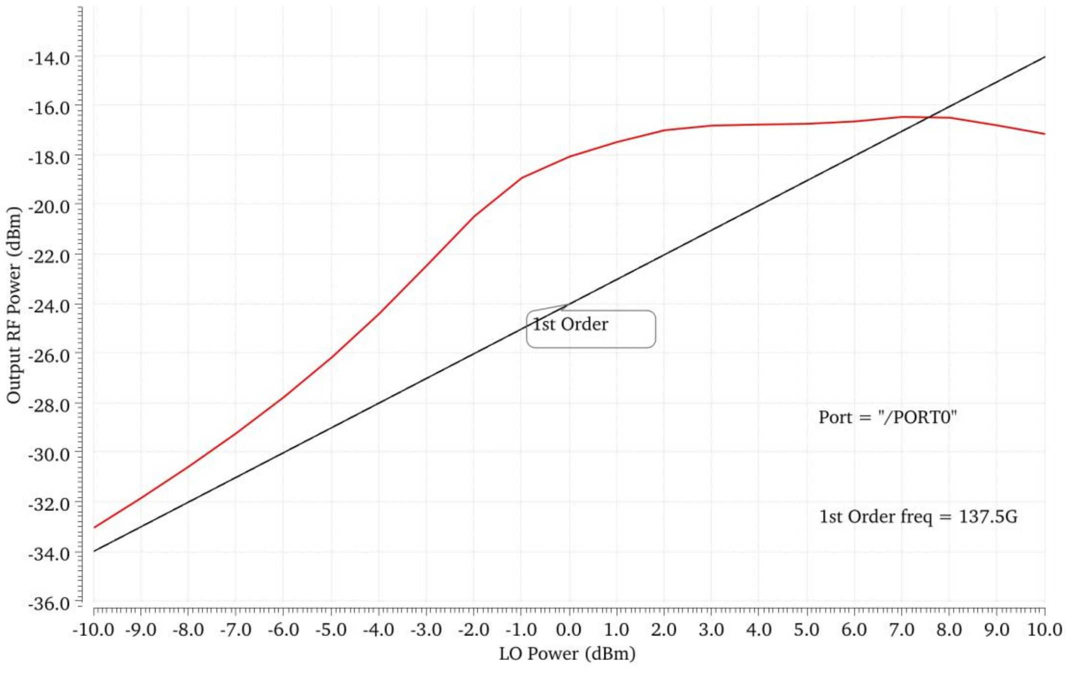


Figure 4. 16: Output RF power vs. Input LO Power with 1dB input referred compression point equal to -7.5dBm, for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, of the LSB modulator.

A summary of the conversion gain for different values of input IF and LO frequencies could be extracted by running multiple harmonic balance analysis, with an IF frequency parameter (fif) changed by the Parametric Analysis tool at Cadence. The fif sweeps at the Parametric analysis from 2 to 20 GHz, for a specific LO frequency. This procedure is repeated three times, each for a different value of the LO frequency. The result, is illustrated below, figure 4.17.

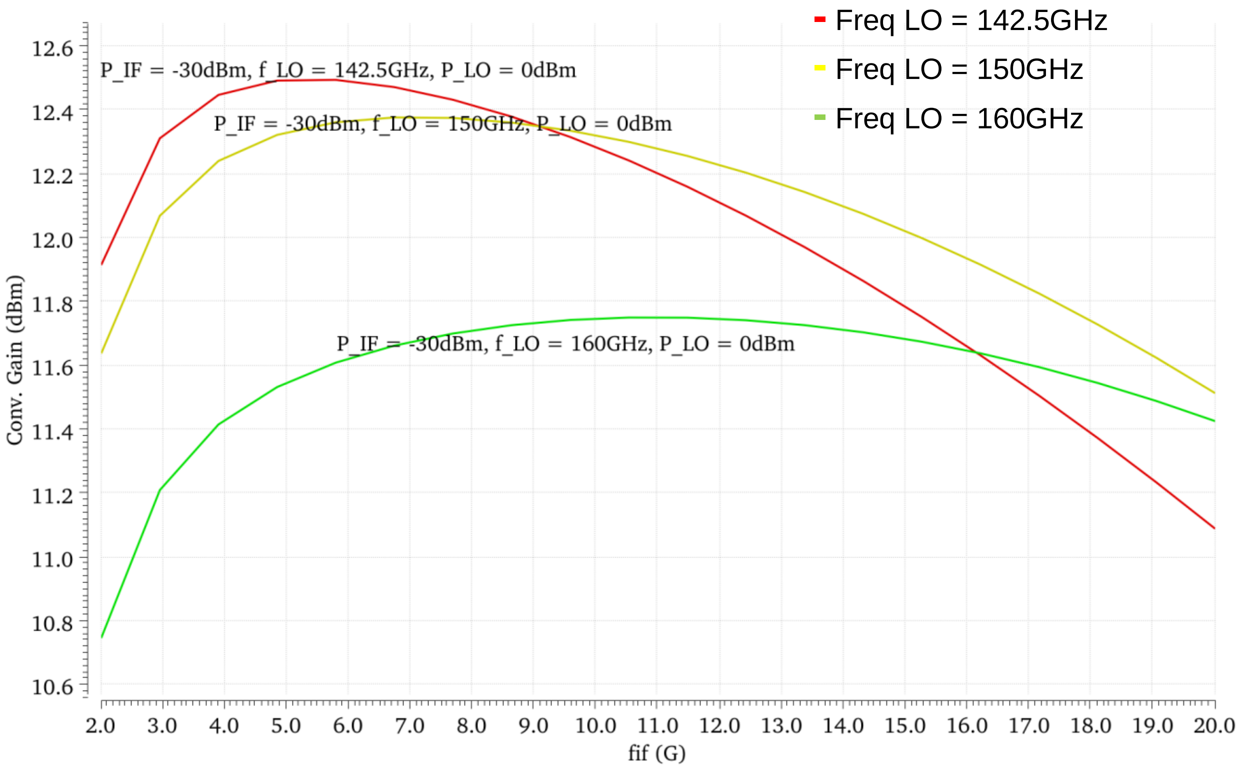


Figure 4. 17: Conversion Gain vs IF frequency for P_{IF} = -30dBm, P_{LO} = 0dBm, for different f_{LO} frequencies, of the LSB modulator.

Also, to ensure that the circuit has a proper behaviour, we run a transient analysis in the time domain. Indeed, the results in the time domain were expected and are presented in the plot below.

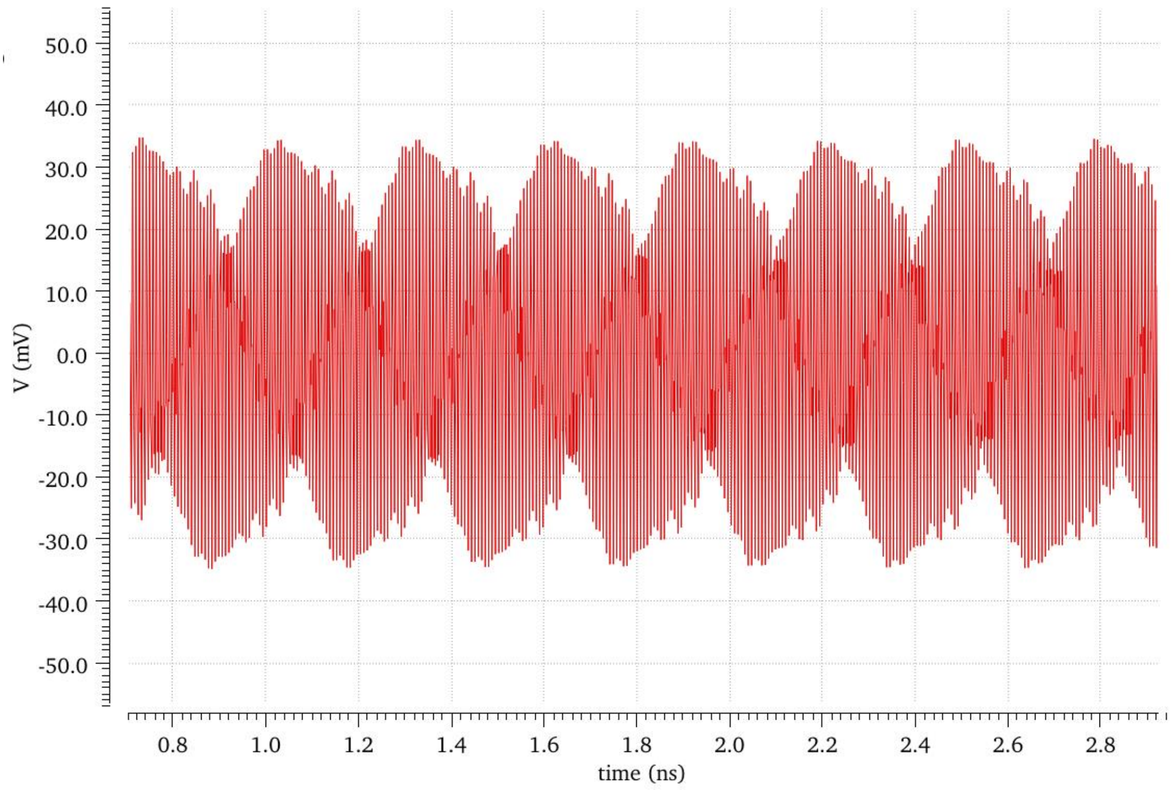


Figure 4. 18: Time domain results, for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GHz, P_{LO} = 0dBm, for the LSB modulator.

From all above graphs we observe a satisfying behaviour of the mixer for the selected operation range. Some fluctuations are expected, but still, for all values the mixer meets the expectations.

4.9.1 Matching Networks Simulation

The matching networks that are designed for each input port are same for the two mixers (in quadrature), for example for the IF inputs, I input has the same matching network with Q input. The LO matching network consists of a tline in series with a mimcap and the IF same, but between these two elements a restan is connected in parallel to the ground. This resistor is significant for the matching, because it achieves the matching at the lower frequencies of IF, but, also, provokes losses, due to its ohmic behavior. The RF matching network for both mixers is shared, as the RF output is shared. All above presented at the modulator schematic, figure 4.11.

With S-param analysis we extract the scattering parameters for all ports. To LO port was given the number 1, to IF port number 2 and to output RF port, number 3.

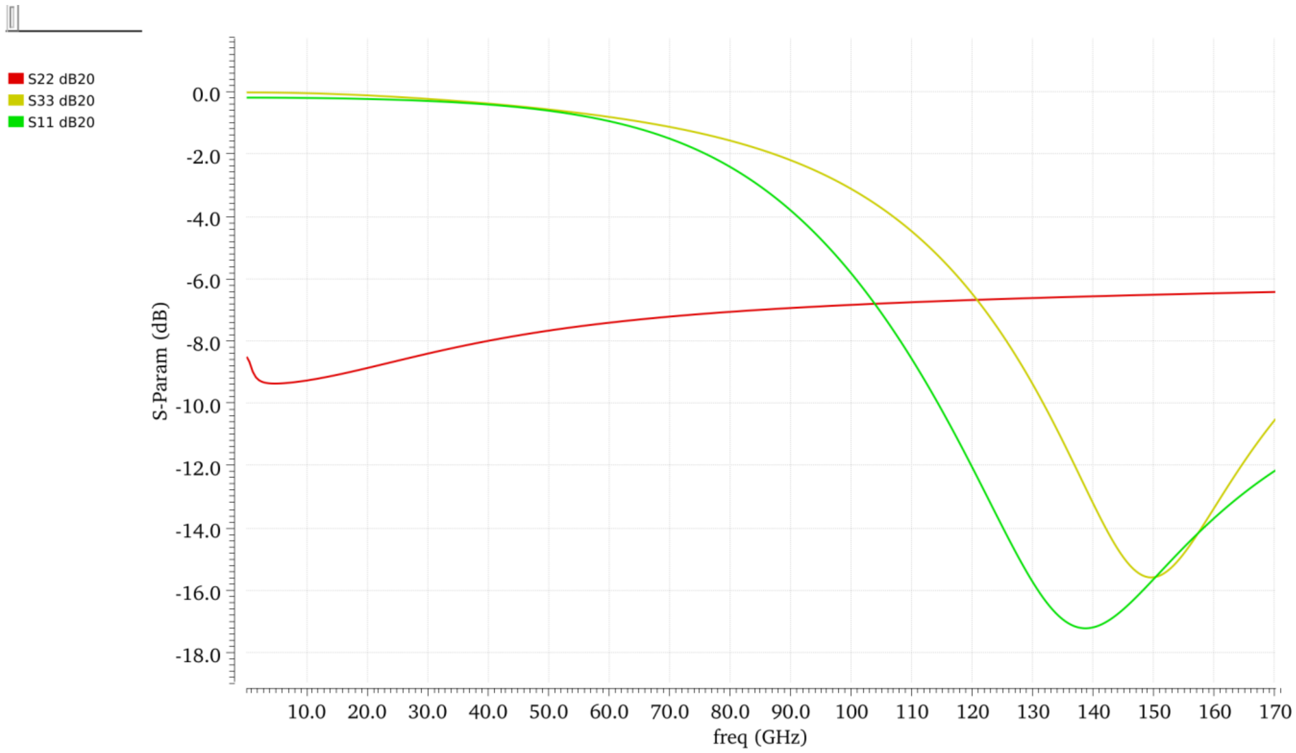


Figure 4. 19: Reflection coefficients for all ports, from SP Analysis 0-170GHz, of modulator.

The proper matching is achieved for the desired frequencies, 0 to 20GHz for the IF (red color), 130 to 160 GHz for LO (green color) and RF (yellow color).

Also, other coefficients, that prove the ports isolations, are presented below, figure 4.20.

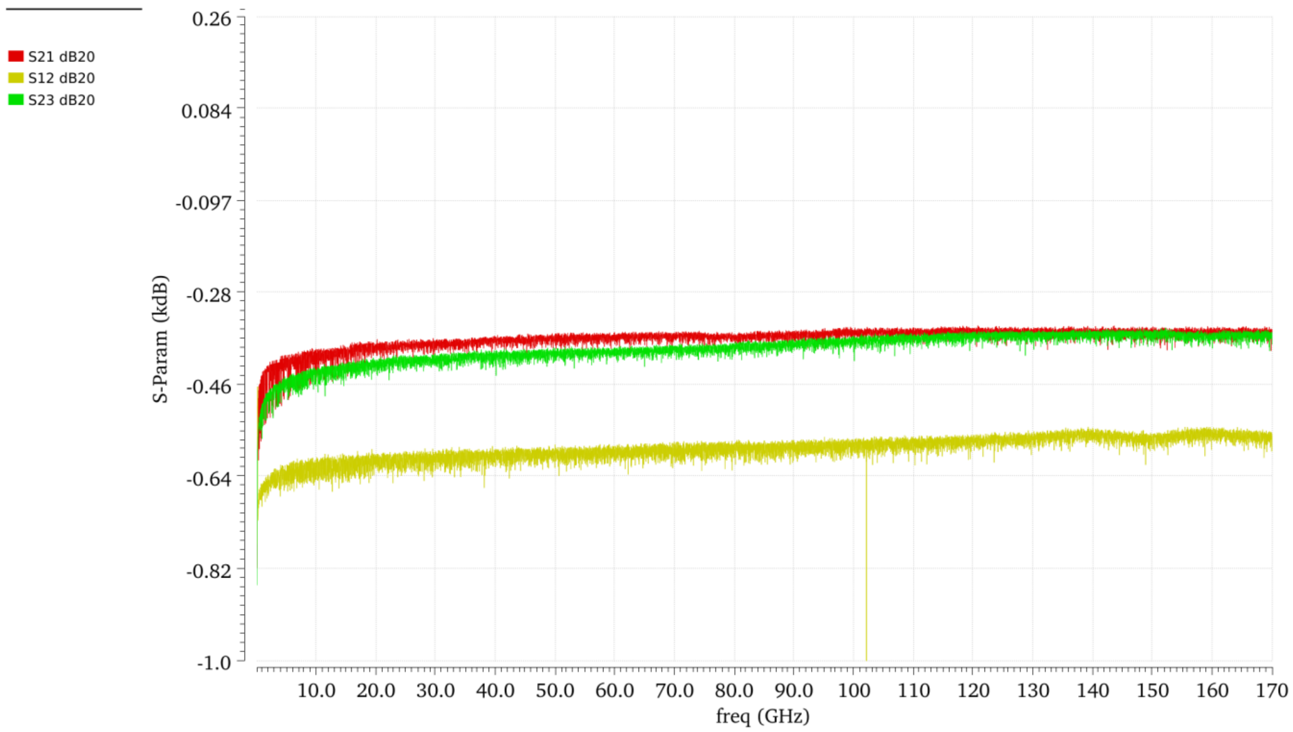


Figure 4. 20: Scattering coefficients for port isolation, from SP Analysis 0-170GHz, of modulator.

4.9.2 Temperature Simulation

In this part, it is important to test the mixer's performance, not only for 45°C, but for a wider and realistic temperature range. For this purpose, running again HB analysis and using the parametric analysis tool, we sweep the temperature from -10 to 100 º C and we calculate the output RF power for each temperature value, which are presented in figure 4.21.

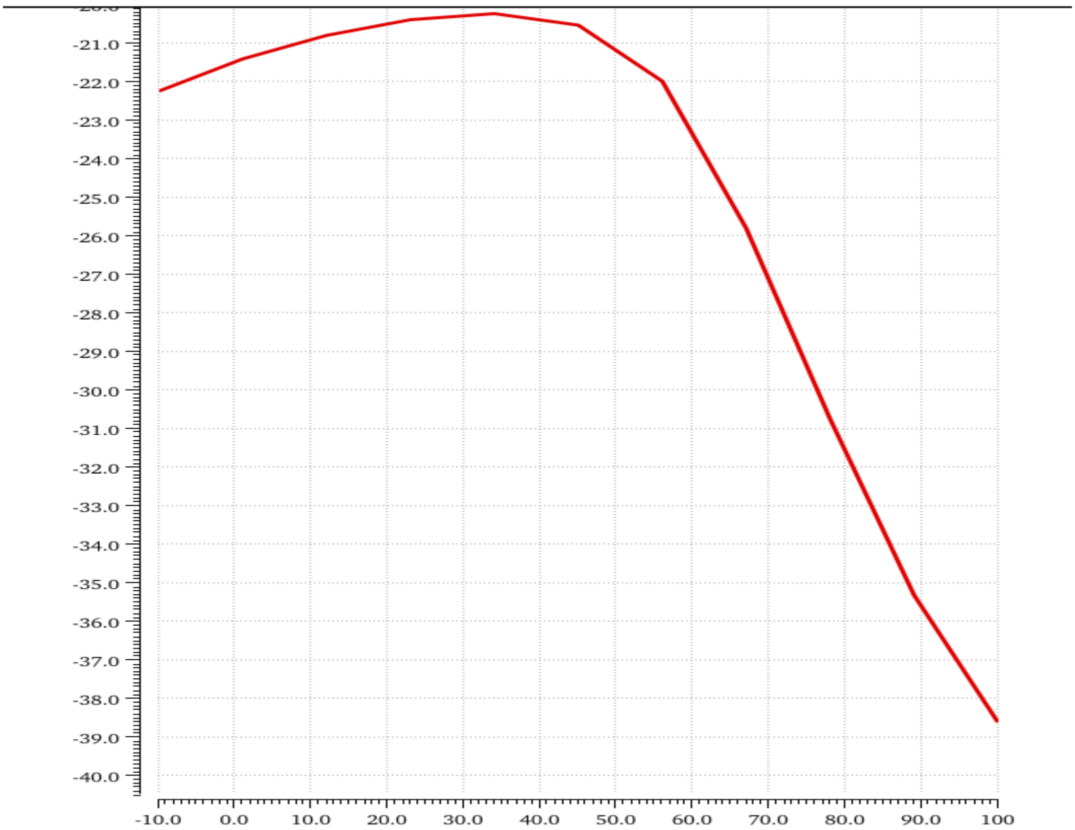


Figure 4. 21: Output RF power (dBm) vs. temperature (º C) for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GH, P_{LO} = 0dBm, of the LSB modulator.

4.9.3 Voltage Supply Simulation

Moreover, the voltage supply levels are crucial to be tested to define the acceptable limits. However, usually a fluctuation of around ±10% of the nominal value, 3.3V for this project, should be tolerated by the circuit, which represents realistic scenarios. Again, the same procedure is followed, as for the temperature test, but, now, the supply voltage, Vcc, sweeps from 2.9V to 3.7V. The output RF power is plotted below, in figure 4.22, where a proper operation is verified for this voltage range.

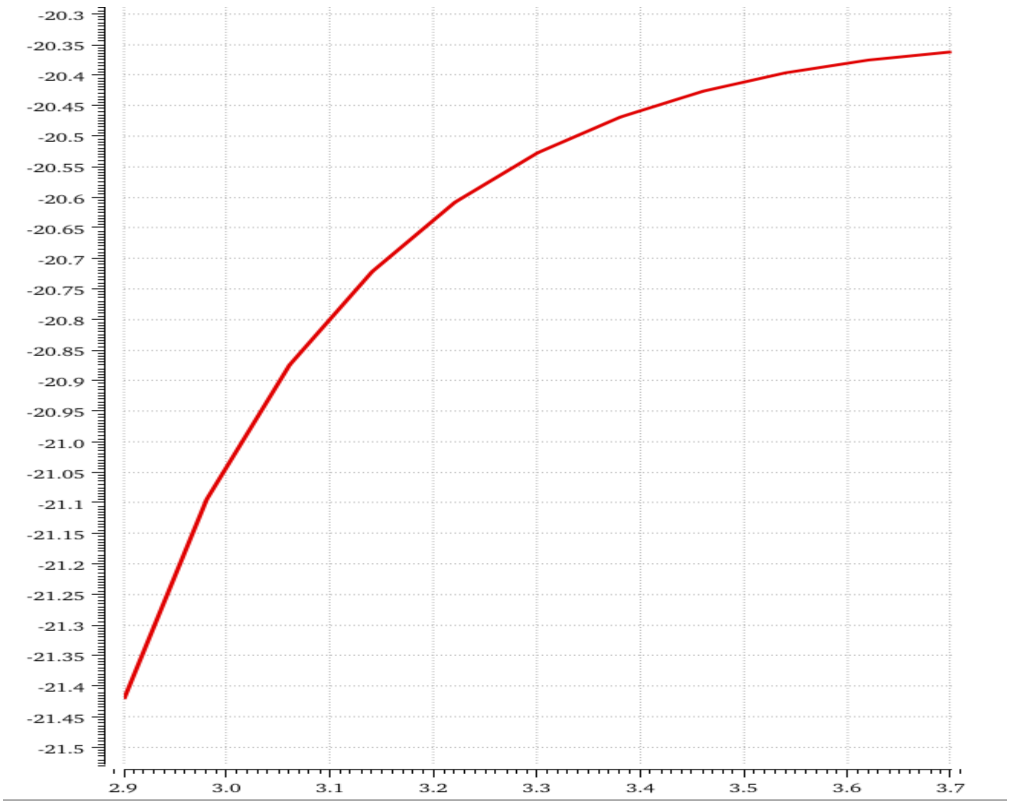


Figure 4. 22: Output RF power (dBm) vs. Vcc (V) for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GH, P_{LO} = 0dBm, of the LSB modulator.

4.9.4 Monte Carlo and Corner Analysis

In addition, Corner and Monte Carlo analysis are essential for a deeper insight into the circuit. With these analyses many other uncertain scenarios regarding fabrication mismatches can affect the electrical behavior of the circuit. Also, again, environmental changed in supply voltage and temperature are tested.

Firstly, for Monte Carlo analysis, we open ADE XL and we enable the setup, figure 4.23.

Corners	☐ Nominal	☑ Example_Corners	☐ Example_MC@nom	☐ Example_MCxCorners
Temperature		45	-40 27 150	-40 27 150
Design Variables				
x		3.3	2.9,3.7	
Click to add				
Parameters				
Click to add				
Model Files				
include.scs		☑ nom sf slow_low_gain fs fast slow hicum_nom hicum_sf hicum_slow_low_gain hicum_fs hicum_fast hicum_slow	☑ mc	☑ mc
ifxbasic.scs		☑ nom	☑ mc	☑ mc
include-all-soac.scs		☑ ...hecks_and_passives	☐ <section>	☑ ...hecks_and_passives
Click to add				
Model Group(s)		<modelgroup>	<modelgroup>	<modelgroup>
Click to add				
Tests				
☑ ...pt_double09:1	☑	☑	☑	☑
...mber of Corners	1	48	6	12

Figure 4. 23: Examples of Corners' setups

For this analysis, all model libraries run simultaneously, not only the hicum_nom, that was chosen until now, to consider all possible transistor's behaviors. The analysis runs for Vcc = 3.3V and T = 45º C.

The output RF power versus the input IF power, for all model libraries, is shown in figure 4.24.

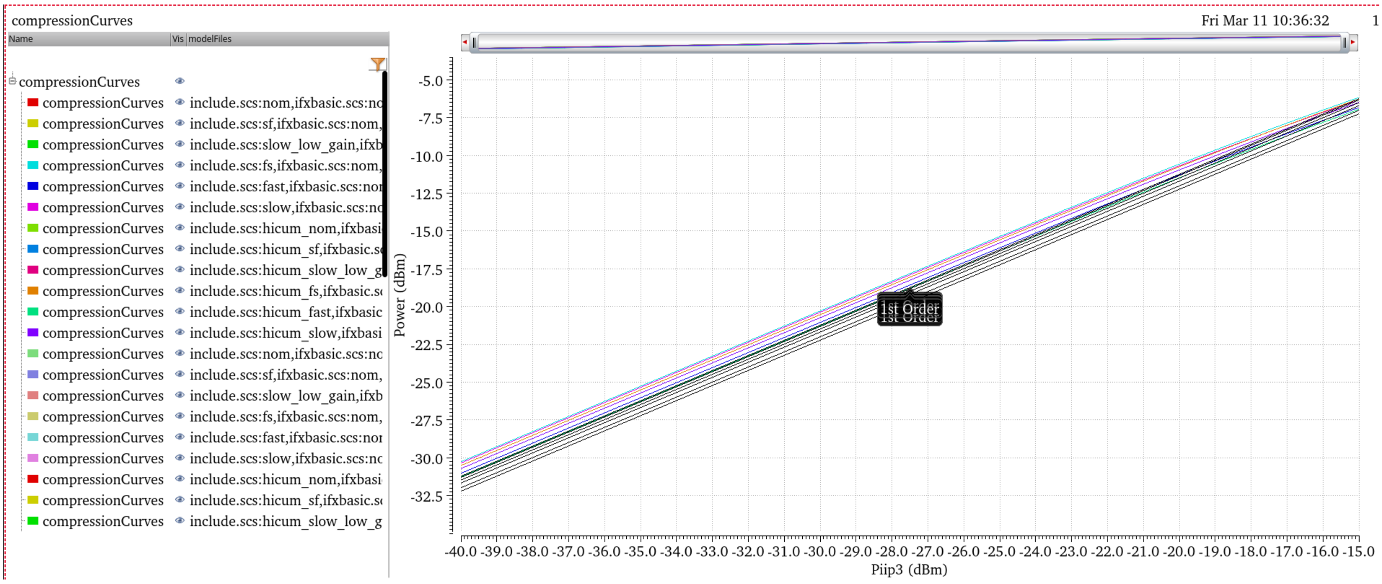


Figure 4. 24: Output RF power vs input IF power, for all model libraries.

Same for the output RF power spectrum, figure 4.25.

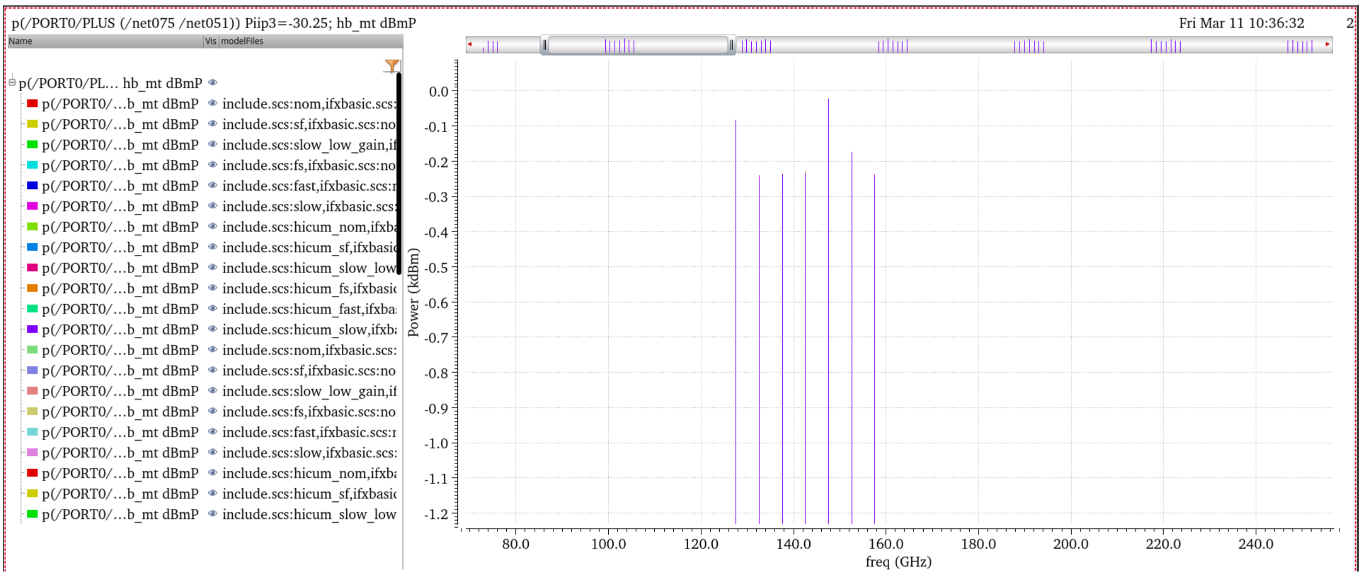
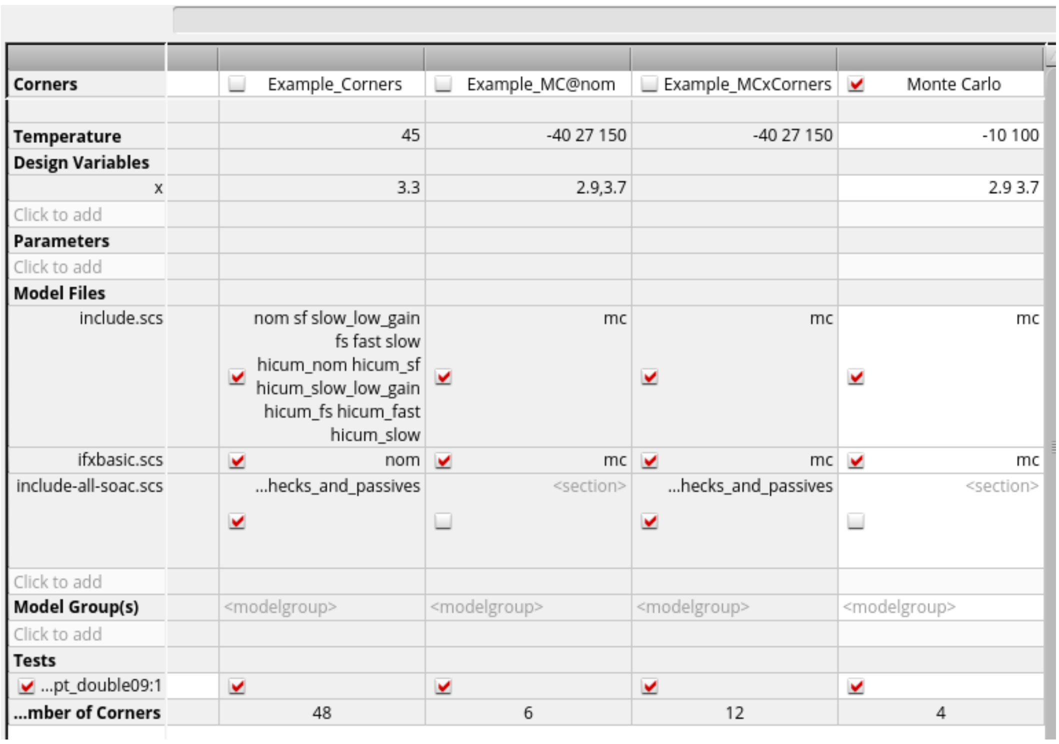


Figure 4. 25: Output RF power spectrum for f_{IF} = 5GHz, P_{IF} = -30dBm, f_{LO} = 142.5GH, P_{LO} = 0dBm, of the LSB modulator, for all model libraries.

It is clear that small fluctuations are observed for different model libraries, concluding that the modulator can tolerate extreme manufacturing variations.

Finally, we perform Monte Carlo analysis, setting the setup below, figure 4.26 and 4.27.



Corners	Example_Corners	Example_MC@nom	Example_MCxCorners	✓ Monte Carlo
Temperature	45	-40 27 150	-40 27 150	-10 100
Design Variables				
x	3.3	2.9,3.7		2.9 3.7
Click to add				
Parameters				
Click to add				
Model Files				
include.scs	✓ nom sf slow_low_gain fs fast slow hicum_nom hicum_sf hicum_slow_low_gain hicum_fs hicum_fast hicum_slow	✓ mc	✓ mc	✓ mc
ifxbasic.scs	✓ nom	✓ mc	✓ mc	✓ mc
include-all-soac.scs	✓ ...hecks_and_passives	☐ <section>	✓ ...hecks_and_passives	☐ <section>
Click to add				
Model Group(s)	<modelgroup>	<modelgroup>	<modelgroup>	<modelgroup>
Click to add				
Tests				
✓ ...pt_double09:1	✓	✓	✓	✓
...mber of Corners	48	6	12	4

Figure 4. 26: Monte Carlo setup for variable temperature and supply voltage

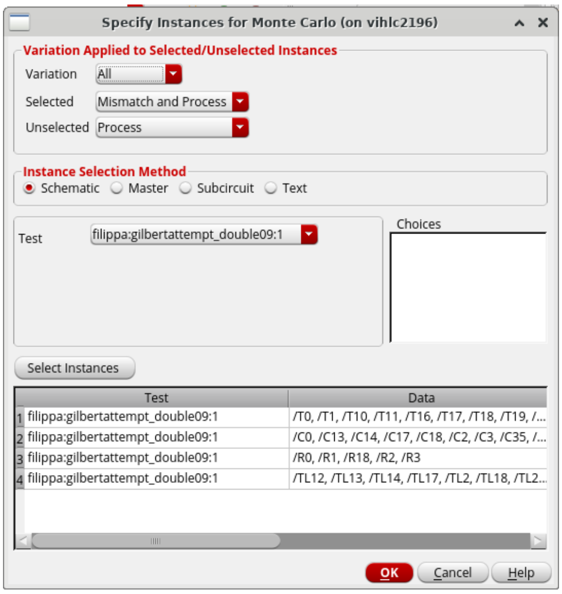


Figure 4. 27: Specification of instances for Monte Carlo Analysis

For Monte Carlo two extreme values are selected for temperature, -10ºC and 100ºC, and voltage supply, 2.9V and 3.7V. All transistors, tlines, resistors and mimcaps from the schematic are selected for Mismatch and Process for Monte Carlo Analysis.

The Monte Carlo cases with the simulation results are shown below, figures 4.28 and 4.29.

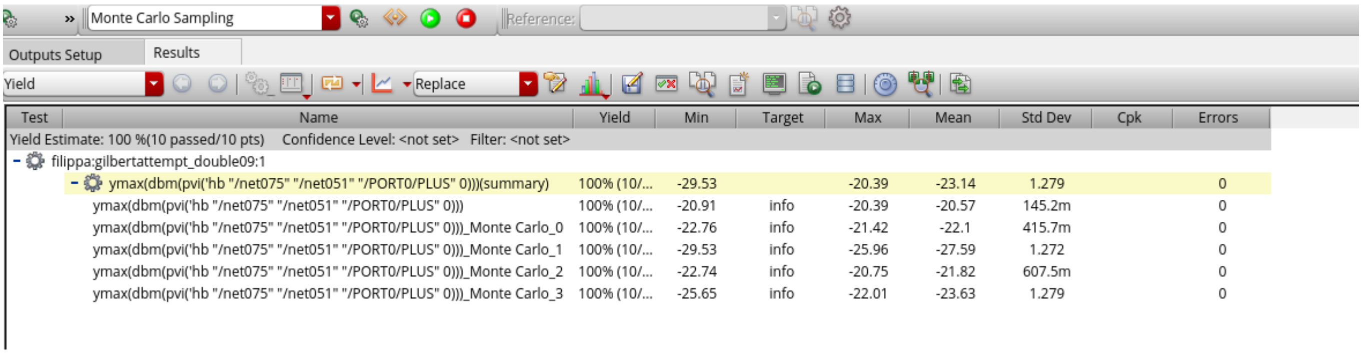


Figure 4. 28: Results for Monte Carlo cases

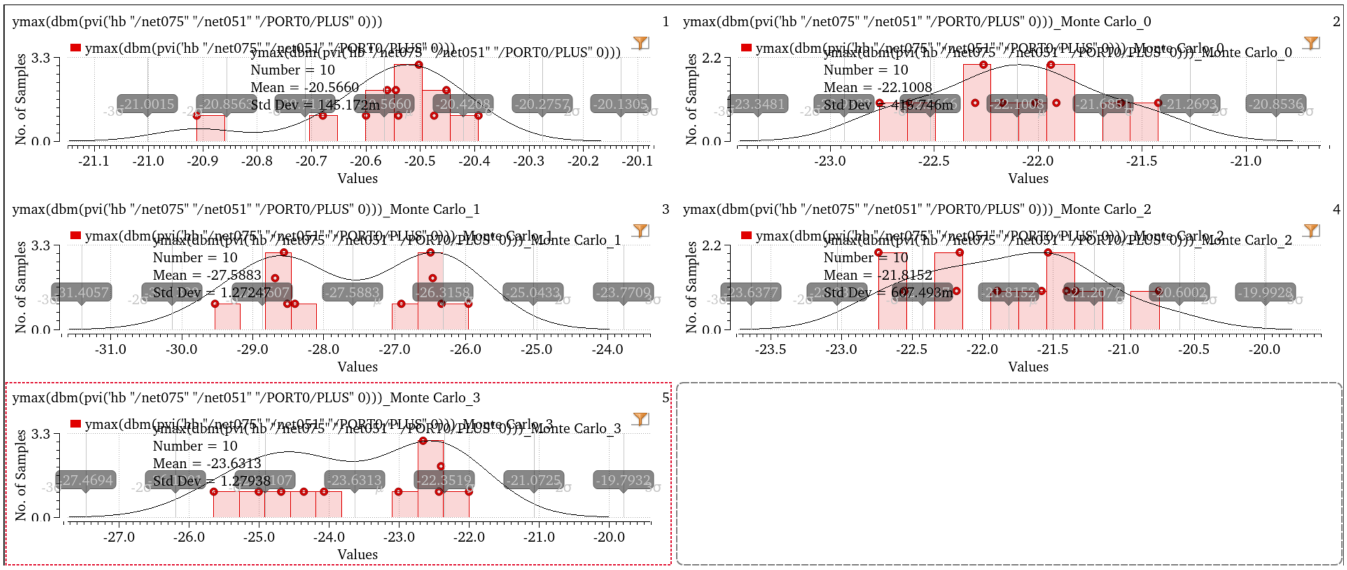


Figure 4. 29: RF output, power of 1st harmonic, for Monte Carlo simulated cases.

CHAPTER 5: LAYOUT DESIGN OF THE UP-CONVERSION MODULATOR

This chapter describes the whole process of designing the modulator at the layout level. It presents the techniques and problems that encountered by the passage of the design from ideal-schematic level to Layout. Each part of the up-converter mixer at the Layout level and the different ways of simulation for deriving the parasitic elements of all passive networks are demonstrated.

At the end of the chapter, the final design is presented with all the necessary additions at the layout level, which was handed over for fabrication to Infineon Technologies AG.

5.1 Active devices and interconnections

The I/Q modulator is implemented in a 130 nm SiGe BiCMOS process with a transit frequency f_T of $250\ GHz$ and an oscillation frequency f_{max} of $370\ GHz$. As previously mentioned in the previous chapter, the selected area of each bipolar transistor of the active device topology is $0.22 \times 2.7\ \mu m^2$, $0.22 \times 4.5\ \mu m^2$ and $0.22 \times 5\ \mu m^2$, accordingly, for each stage, while each transistor consists of one block and has a double base ($BEBC$). The technology features 6 copper layers and a top aluminum metal layer. MIM capacitors, polysilicon and TaN resistors are also available.

The intermediate Metal 4 is used as reference ground, while Metal 3 is used as a power supply plane. Lower metals 1, 2 are mostly used for dc interconnects. Low loss thick top metals 5 and 6 realize all the RF structures offering reduced capacitive coupling to the ground. Particular attention was paid to the interconnections in order to meet the current limits requirements for the metal widths and, thus, secure the metal connection from high current values. Also, the parasitic capacitance and inductance, that all metal interconnections add, were controlled by adjusting the length, width and metal layer, to not exceed an acceptable value.

For the power supply, measurement acquisition and even packaging of an implemented integrated circuit, it is necessary to introduce contact pads to all the inputs and outputs of the circuit, whether we refer to the dc power supply or to the input and output of RF signals. The Contact Pads used in the implementation of the power amplifier in this thesis are Aluminum Pads. More specifically, all the contacts of the circuit consist of a stack of shorted metals the highest of which is aluminum [15].

In order to provide the proper LO phases at the bases of the HBTs of the switching stage, a well-defined differential LO coupler is inserted between the LO generation circuitry and modulator. The layout was implemented with the Cadence Layout tool and the final design is illustrated in figure 5.1. Also, the complete design of the transmitter, which was sent for the tape out, is presented in figure 5.2., where the mixer of this thesis is presented inside the red frame.

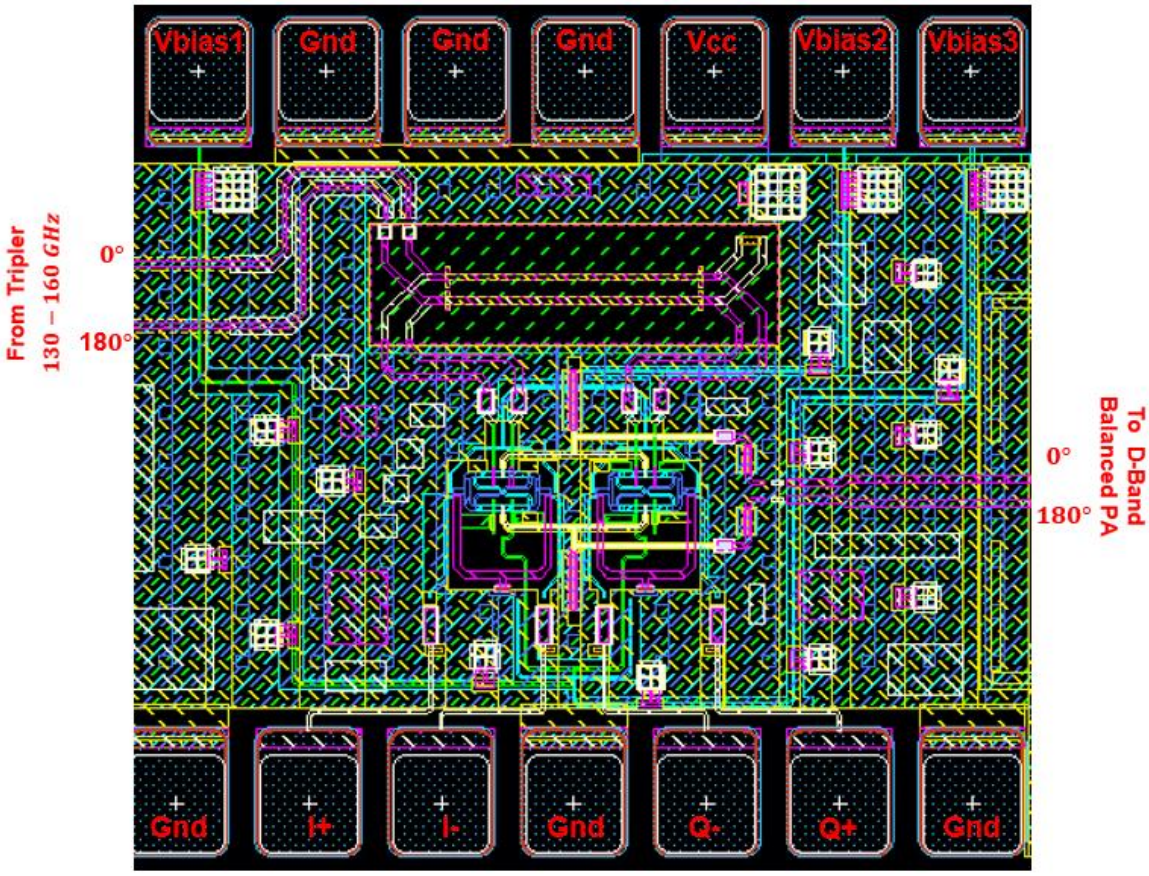


Figure 5. 1: Final layout of the proposed I/Q Modulator.

Figure 5. 2: Final layout of the PMFTX.

A version of the I/Q Modulator layout, removing the ground and supply plane, is shown below in figure 5.3. The total area of the integrated designed is 0.455mm^2.

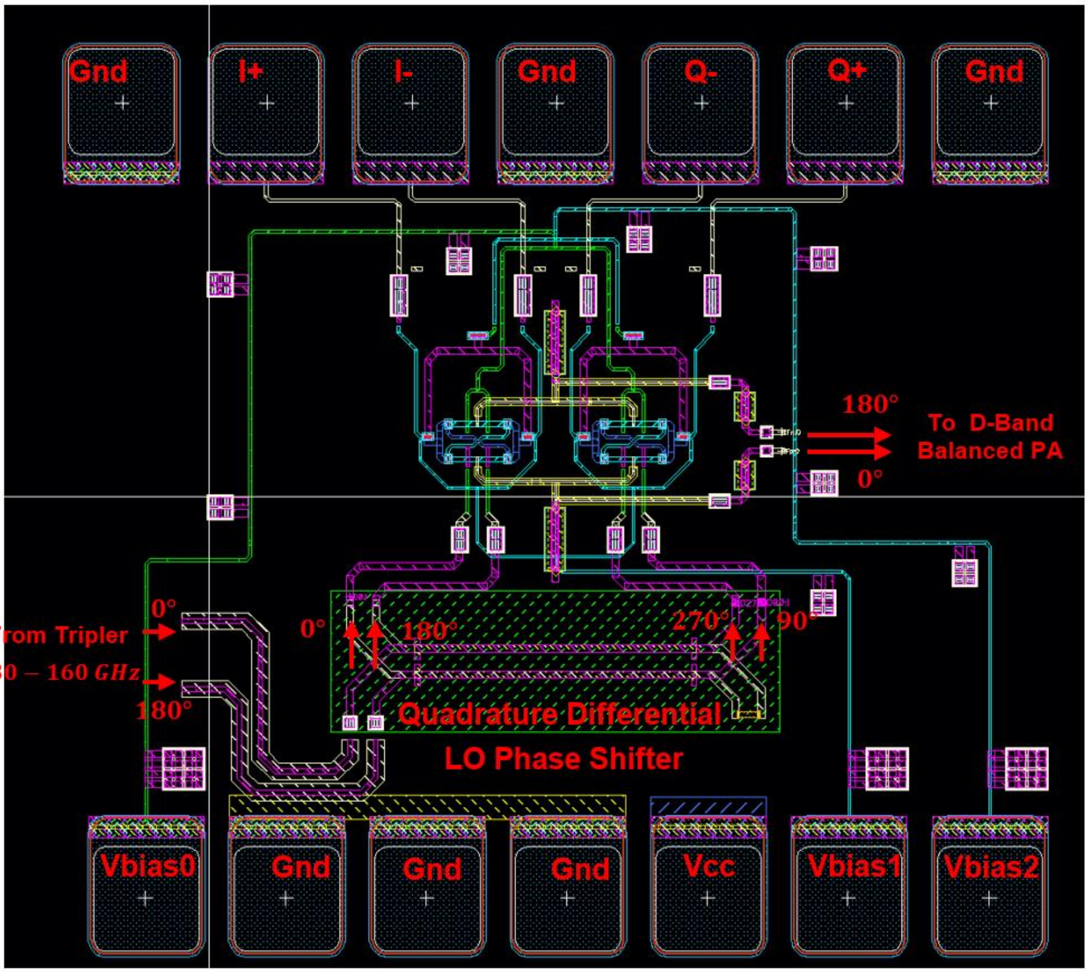


Figure 5. 3: Final layout of the proposed I/Q Modulator, without ground and supply plane.

The high frequency operation of the proposed I/Q modulator requires an accurate modeling of transistors' metal interconnects. To test the performance of the up-converting mixer, we used *RC parasitic extraction* (Cadence tool) for the HBTs up to metal 4 and, then, the *ADS Momentum* tool was used up to metal 6 for the HBTs as well as for all circuit elements and interconnections, to run electromagnetic (EM) simulation. The extracted S-parameter data were imported in Cadence and the following results were extracted, running harmonic balance analysis.

The metal stack used in the given 130nm technology is shown in figure 5.4.

Figure 5. 4.: Metal stack.

5.2 Modulator design

The significant specification of LO leakage was highly affected by the layout structure and especially by the mixer core's structure. At such high frequencies the layout design is challenging because the inductive and capacitive phenomena between different metal planes are more pronounced. Therefore, particular attention was paid to the overlaps and distances between the interconnect metals and to the choice of metals in terms of their dimensions and level. Noteworthy is the fact that different metal levels imply different values of equivalent inductance and capacitance with the ground plane. More specifically, lower metals (metal 1 to 4) exhibit lower inductance than higher metals (metal 5 and metal 6), which are thicker and, thus, have higher current tolerance. In addition, for the same metal level, the use of a ground plane can change the behavior of the metal, for sub-Terahertz frequencies.

For example, we EM simulated, in Momentum, a single metal2, of 30um length, assuming that its ground plane is implicit, or equivalently the substrate. The resulting S-parameter data of the EM simulation are then imported to the schematic cell of figure 5.5.

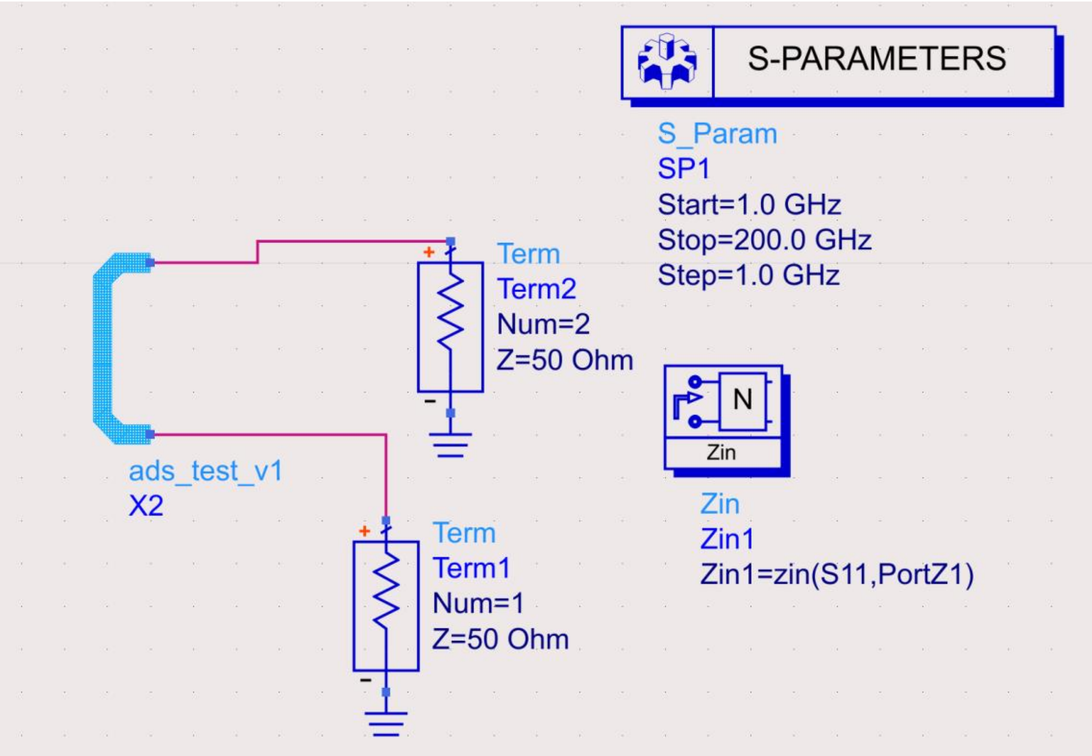


Figure 5. 5: ADS schematic cell for characterization of a single metal2 line.

Both ends of the metal are terminated in a 50Ohm port and this schematic is simulated again, running an S-parameter analysis. From this simulation, we get the following results, in figures 5.6, 5.7, 5.8.

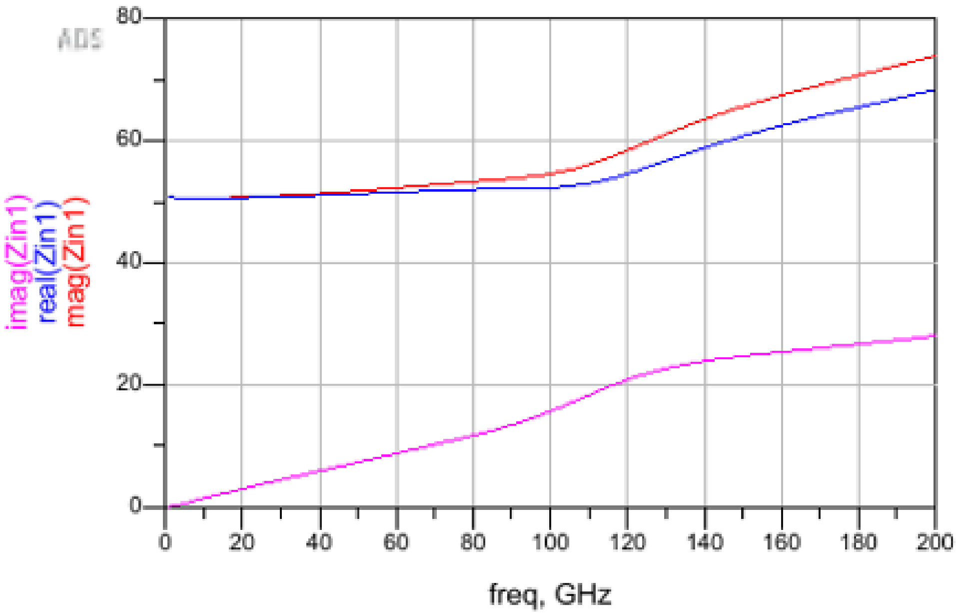


Figure 5. 6: Magnitude, real and imaginary part of input resistance for metal2.

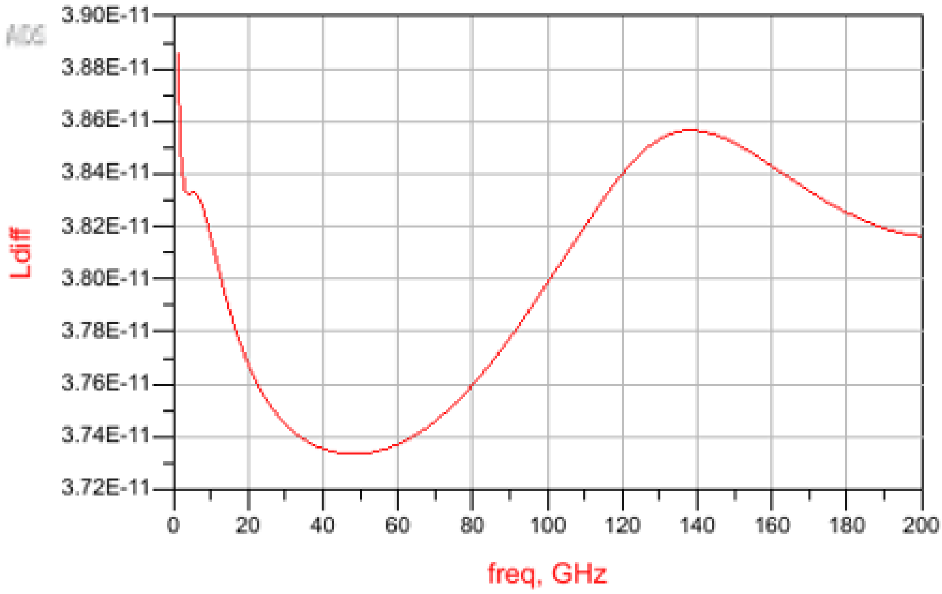


Figure 5. 7:Parasitic inductance of the input resistance for metal2.

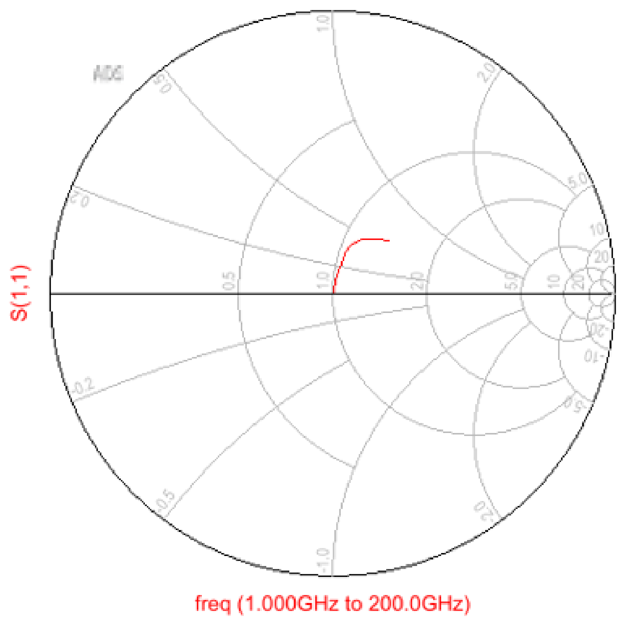


Figure 5. 8: Smith Chart of the input resistance for metal2.

The figures above indicate an inductive equivalent behavior, which is more pronounced at higher frequencies. Figure 5.6 and figure 5.8 show that metal2 presents a positive real part in the input resistance, thus inductive, and in figure 5.7 we calculate that this parasitic inductor is around 38.5pH for the frequencies of interest (130GHz to 160GHz).

Now we repeat the same procedure, with the same metal but we used for ground plane a metal1 plane, which is closer, than the implicit ground, to metal2. Again, the resulting S-parameter data of the EM simulation are imported to the same schematic topology of figure 5.9.

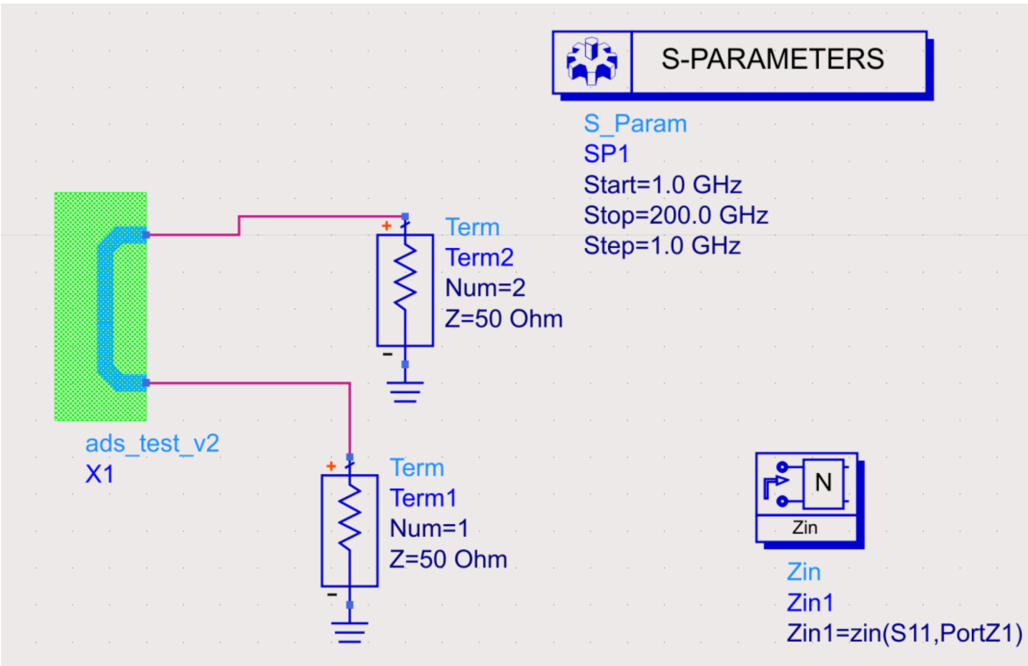


Figure 5. 9: ADS schematic cell for characterization of a single metal2 line with metal1 ground plane.

The results from this simulation are presented in figures 5.10, 5.11.

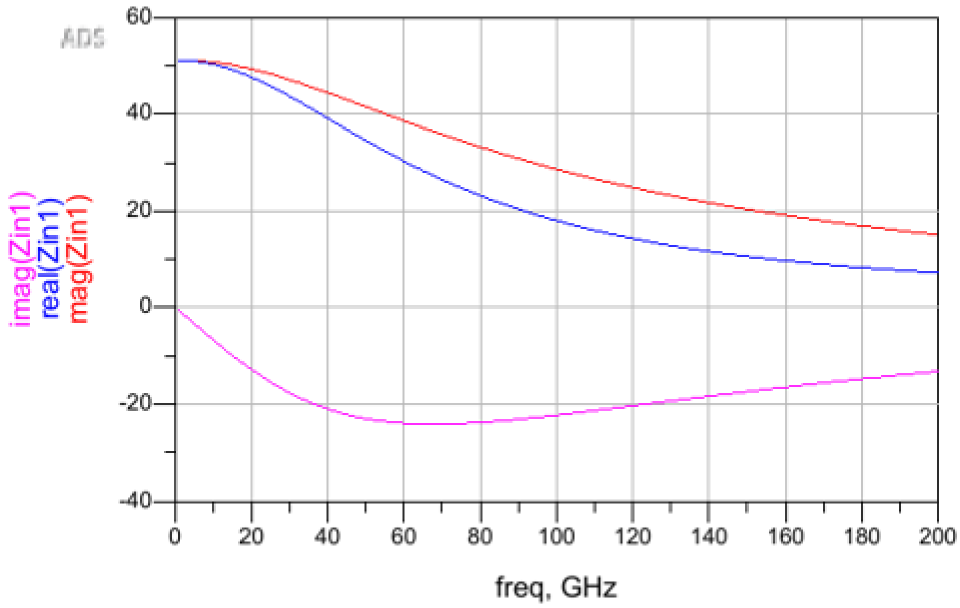


Figure 5. 10: Magnitude, real and imaginary part of input resistance for metal2 with metal1 ground plane.

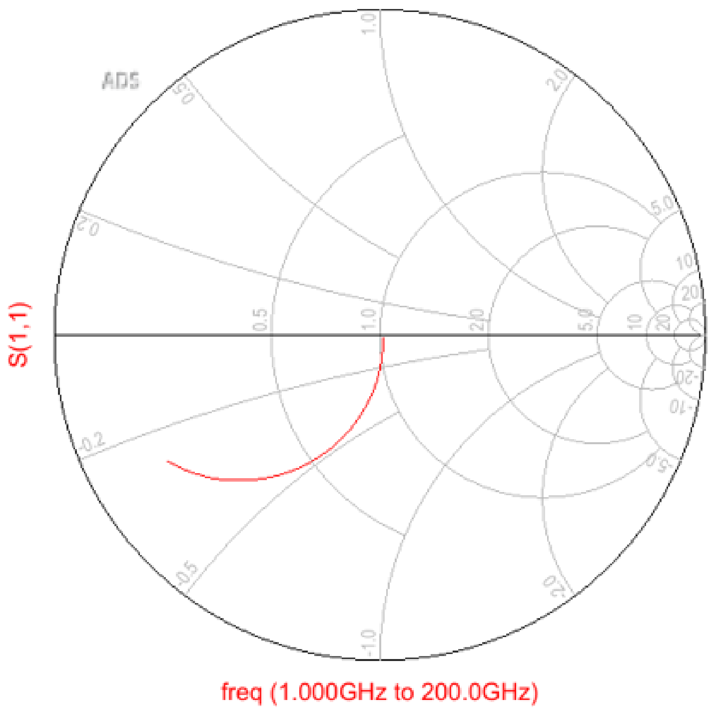


Figure 5. 11: Smith Chart of the input resistance for metal2 with metal1 ground plane.

The addition of a ground plane approximately 0.341um from metal2, which is the distance between the two metals, is changing the behavior of metal2 significantly.

Figures 5.10 and 5.11 show a negative imaginary part of the input resistance, or in other words a parasitic capacitance formed between the two metals.

The above results underline that parasitic phenomena are highly observed at these frequencies, but also that we should carefully use the ground plane to not have undesirable parasitic behavior. As a result, for the switching and transconductance stages the implicit ground plane was used and no other metal plane was added, in order to avoid this undesirable distributed capacitance in the signal path.

Another key factor that determines the layout design is the symmetry in the signal path. Any asymmetry inserted in the signal path can cause imbalances and thus deteriorations, as the fully balanced gilbert cell topology gradually loosens. Also, of high importance was the placement of the rpoly resistors that provide the dc biasing to the switching stage. In particular, the closer rpoly resistors are to the HBT's base the better.

For the layout schematic, the first step was to design the structure of the switching stage, the mixer core, which is the most challenging due to the number of interconnections and signals it contains.

A first attempt was the following, in figure 5.12, presenting only the LO input and RF output paths for the switching stage. In this case, asymmetry in the metal length exists in the input LO signal path (metal 6). Additionally, LO input and RF output paths are significantly overlapping. These characteristics can cause enough deterioration to the mixer performance, in terms of the LO leakage, exceeding the acceptable level.

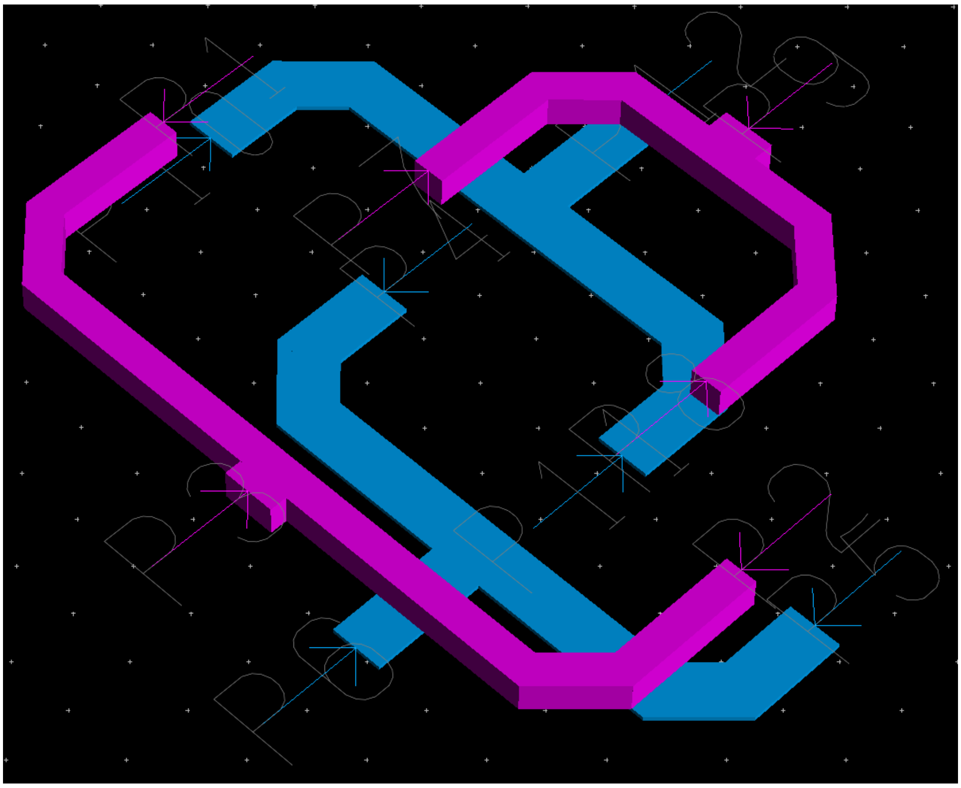


Figure 5. 12: Mixer core draft1 for the I/Q Modulator.

Another proposal for the mixer core that was tested is the following, in figure 5.13, with its 3D representation, in figure 5.14.

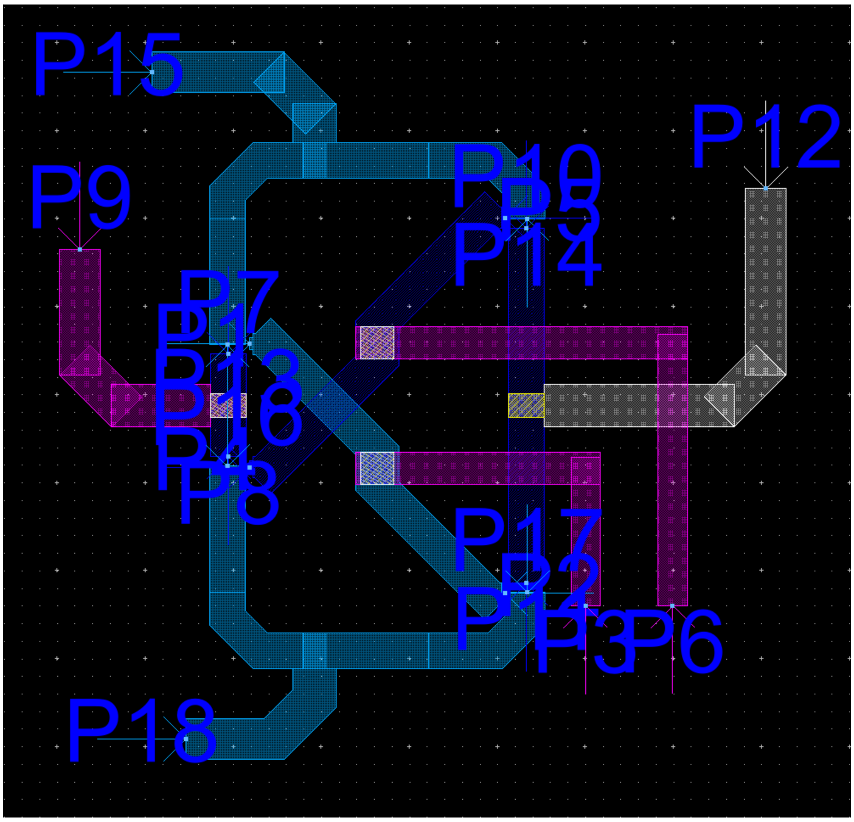


Figure 5. 13: Mixer core draft2 for the I/Q Modulator.

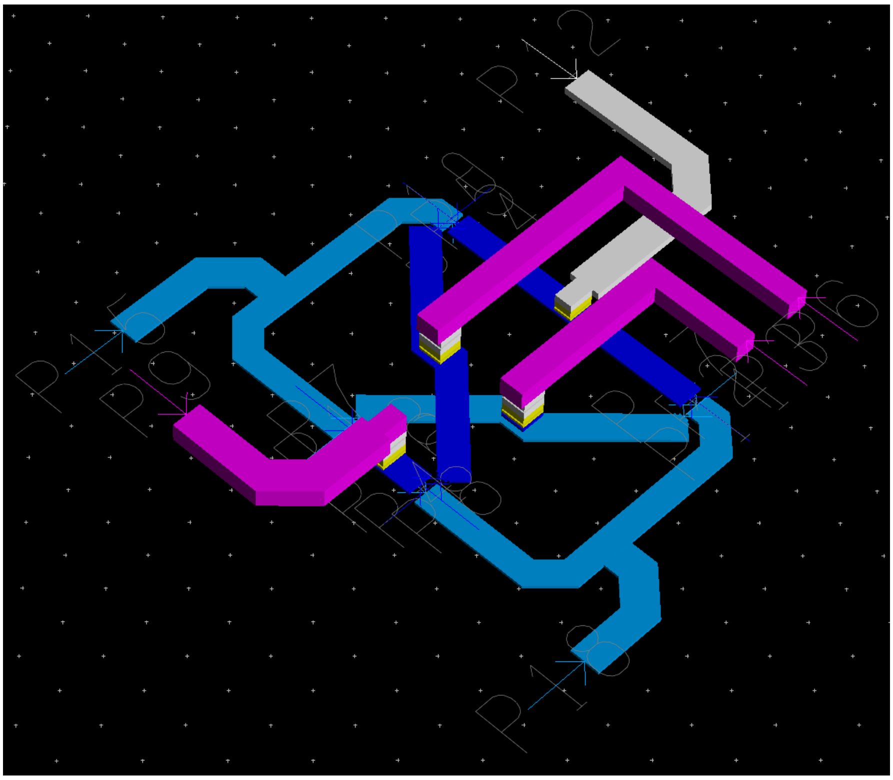


Figure 5. 14: 3D illustration of the mixer core draft2.

For this mixer core implementation, the asymmetry was transferred to the output RF signal path (metal 3). Nevertheless, the specification of the LO leakage was slightly improved, due to the fact that no overlap exists between the input LO signal path and the output RF signal path. However, still the results of LO leakage were not enough satisfying, needing an improved approach.

From the above observations, the optimum performance was achieved with the following structure for the mixer core, in figure 5.15. In this layout the majority of the input and output paths are symmetrical for the differential signals and, also, the metal overlaps between the paths are minimized.

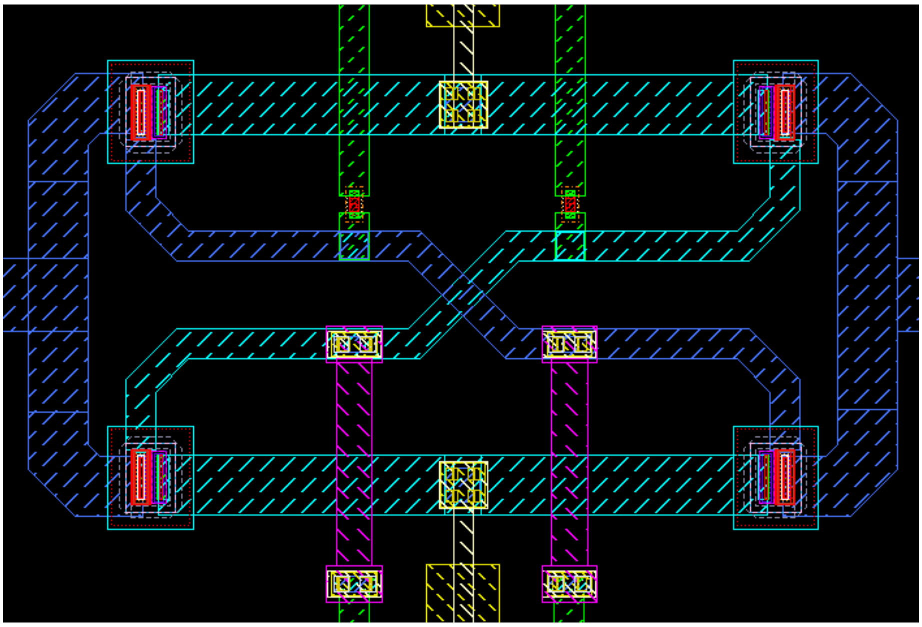


Figure 5. 15: Mixer core layout of the proposed I/Q Modulator.

The mixer core layout above is 3D illustrated in figure 5.16.

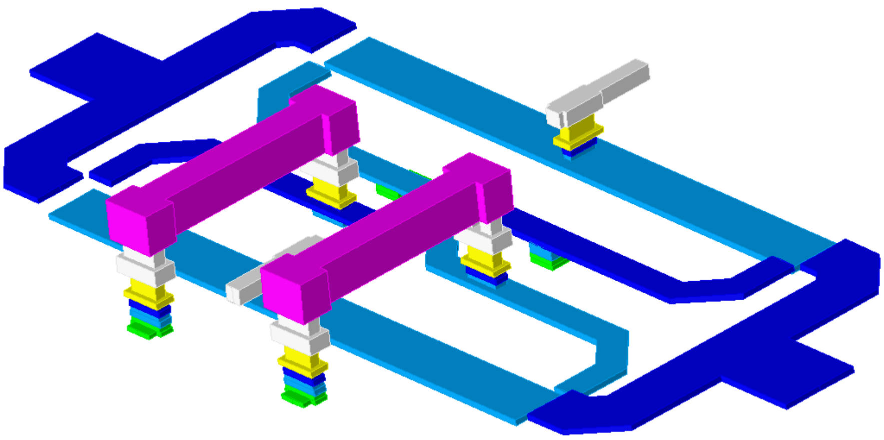


Figure 5. 16: Mixer core layout of the proposed I/Q Modulator, 3D illustration.

Simulating, exclusively, the mixer core in the environment of Momentum and importing the S-parameters to Cadence, we perform a harmonic balance analysis on the initial schematic. The performance of the mixer is presented in the figure 5.17, where a leakage level of 50 dBc is observed.

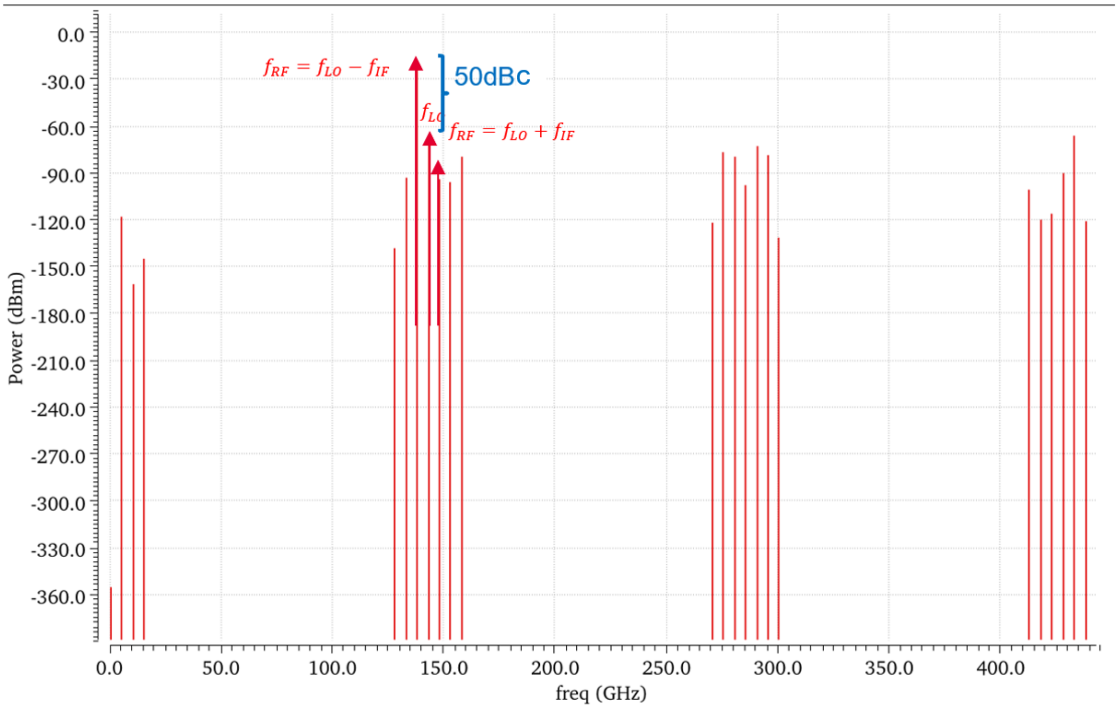


Figure 5. 17: Output spectrum for f_{LO} = 142.5 GHz, P_{LO} = 0 dBm, f_{IF} = 5 GHz, P_{IF} = -30 dBm of LSB Up-Conversion Modulator, replacing the mixer core EM results.

A simple test to verify the results for the LO leakage is to compare the S-parameter data of the first and the final mixer-core structure. For the first case of figure 5.12, presented also in figure 5.18, the S-parameters that describe the signal crossing at the LO+ and the LO- path and the signal cross from the LO path to the RF path, are shown in figures 5.19, 5.20 and 5.21.

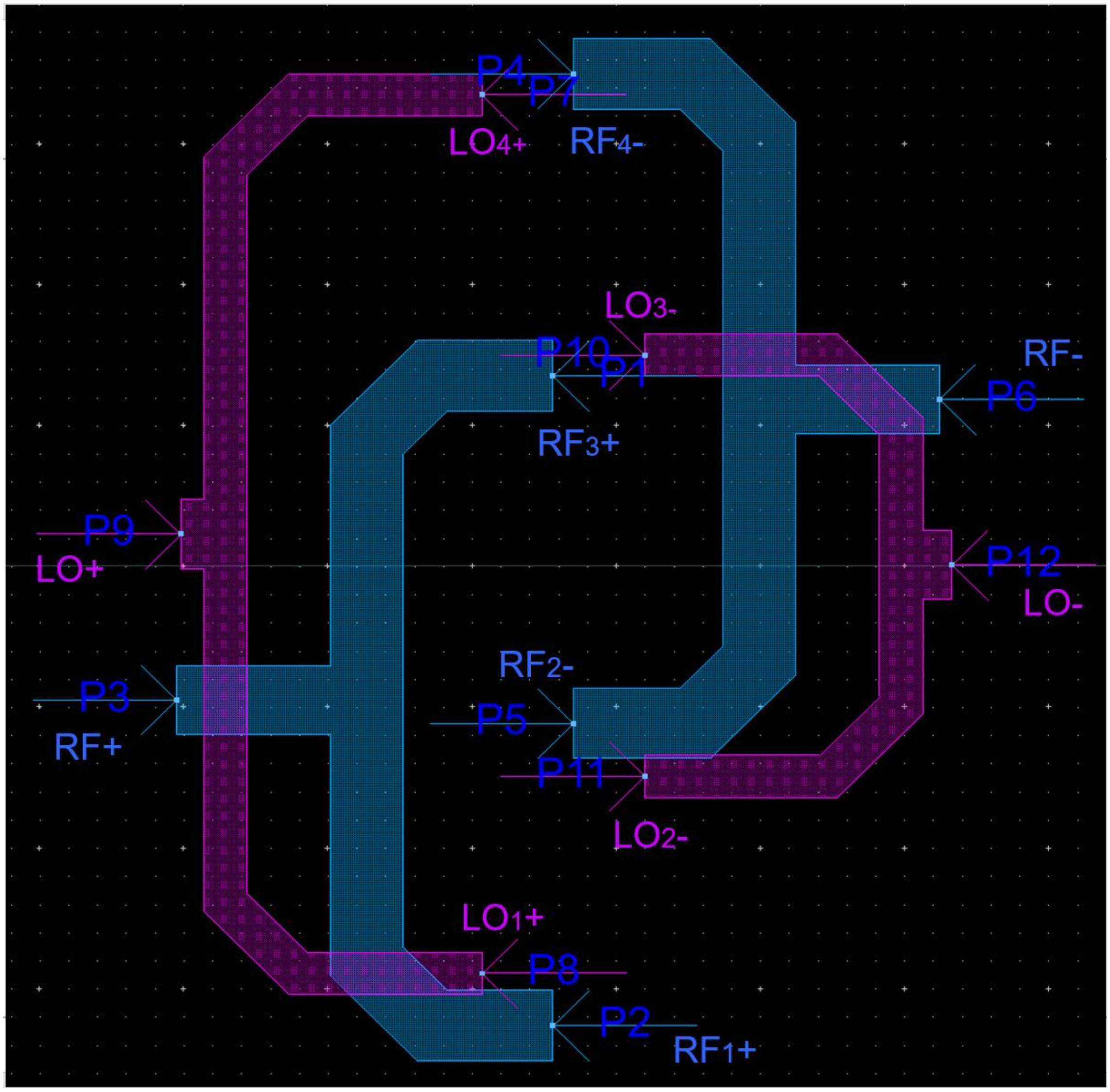


Figure 5. 18: Mixer core draft1 for the I/Q Modulator with highlighted port numbers.

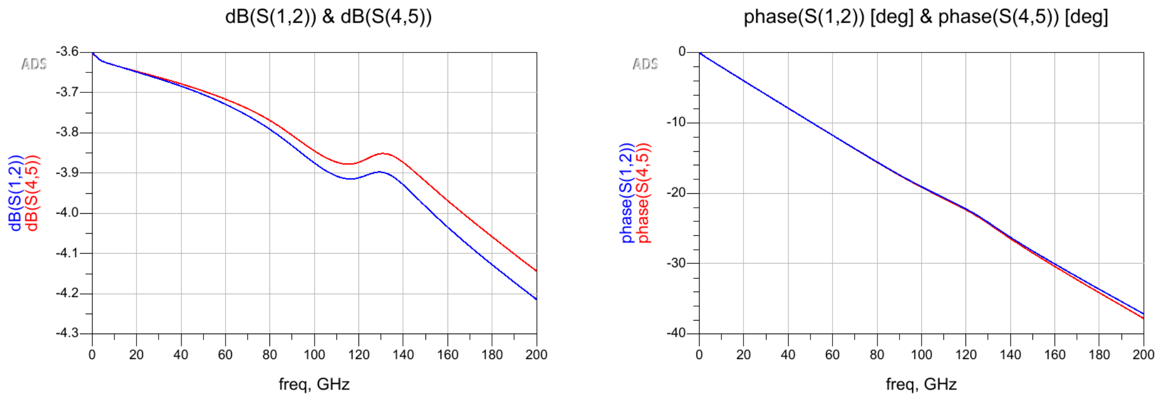


Figure 5. 19: S-parameter S12 and S45 coefficients for the LO+ and LO- signal path, for the mixer core draft1.

In figure 5.19, the comparison between the LO+ and the LO- signal paths is realized. The seemingly identical paths give different S-parameter results, therefore they are expected to cause imbalances at the signal flow. Also, in figure 5.20 we observe for the LO path a transit coefficient of around -3.67dB, for the frequency band of interest, and in figure 5.21 the rejection of LO signal at the RF output port is around -22dB for the same frequencies.

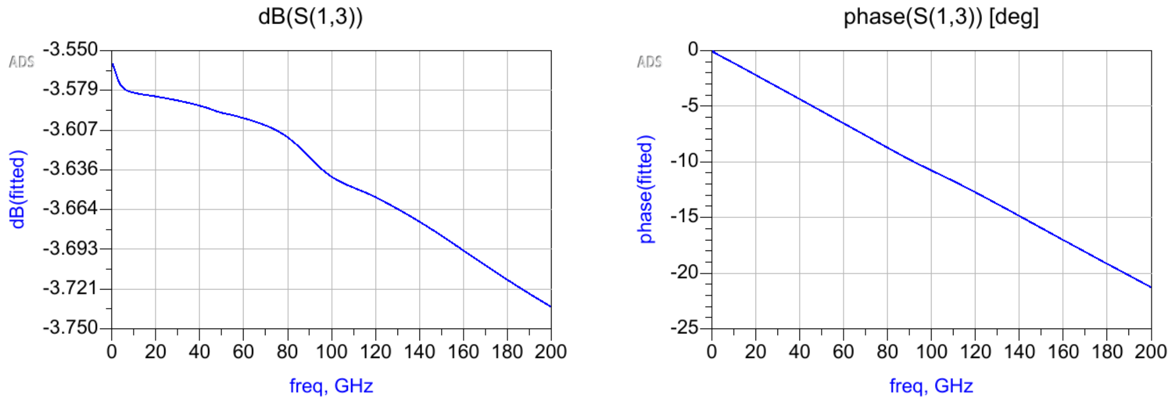


Figure 5. 20: S-parameter S13 coefficient for LO signal path, from the input pin to the HBTs' base, for the mixer core draft1.

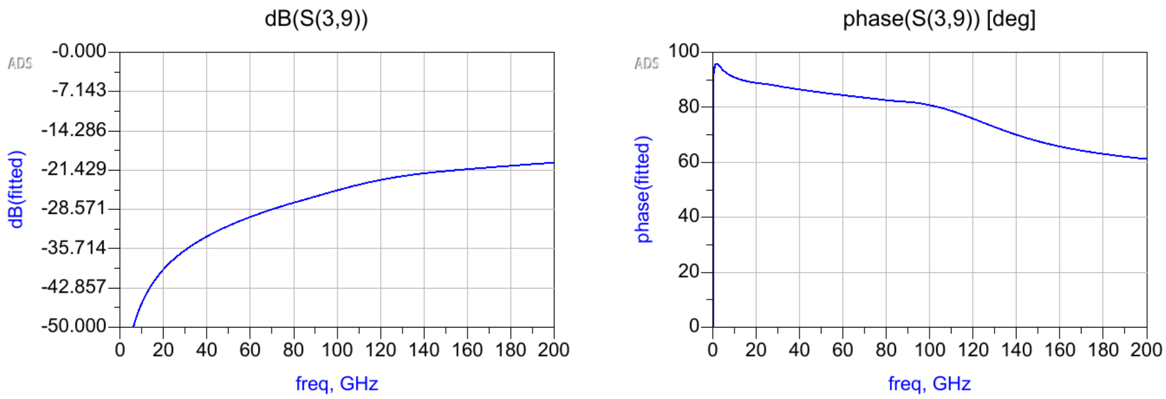


Figure 5. 21: S-parameter S39 coefficient for signal cross from the LO input to the LO output, for the mixer core draft1.

On the other hand, for the final mixer-core, in figure 5.22, following the same steps, we extract, correspondingly, the S-parameter results for the LO+ and – signal path and the LO rejection at the RF output, in figures 5.23, 5.24 and 5.25.

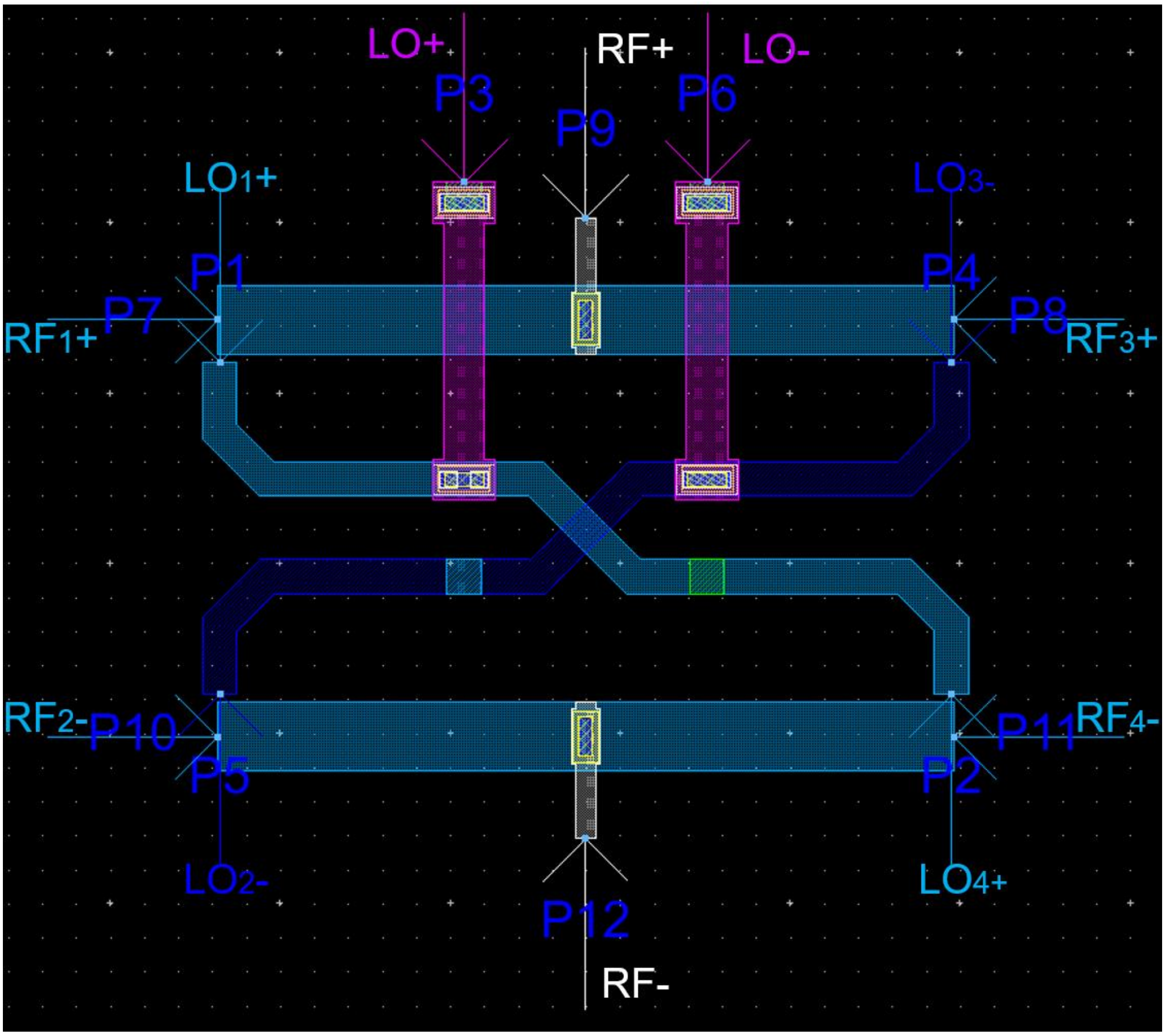


Figure 5. 22: Mixer core layout of the proposed I/Q Modulator, with highlighted port numbers.

For the frequency band of interest (130 to 160 GHz) we get very similar S-parameter values for the LO+ and LO- paths, in figure 5.23, which result in minimum imbalances, in contrary to the previous structure in figure 5.18.

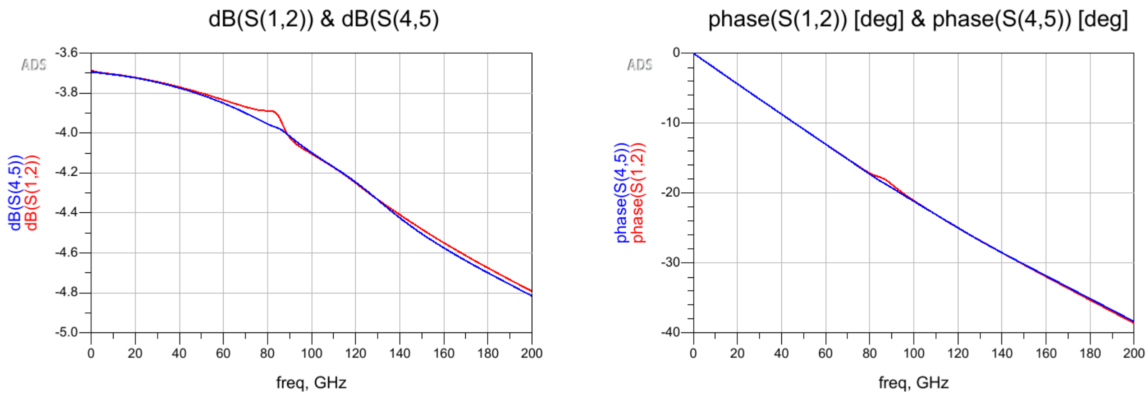


Figure 5. 23: S-parameter S12 and S45 coefficients for the LO+ and LO- signal path, for the mixer core.

Additionally, in figure 5.24 we observe for the LO path a transit coefficient of around -3.3dB for the frequency band of interest and in figure 5.25 the rejection of LO signal at the RF output port is around -28dB for the same frequencies. These values show an improvement for the performance of the mixer core compared to the previous structure. This improvement is expressed in lower imbalances and, as a result, in optimized LO leakage level.

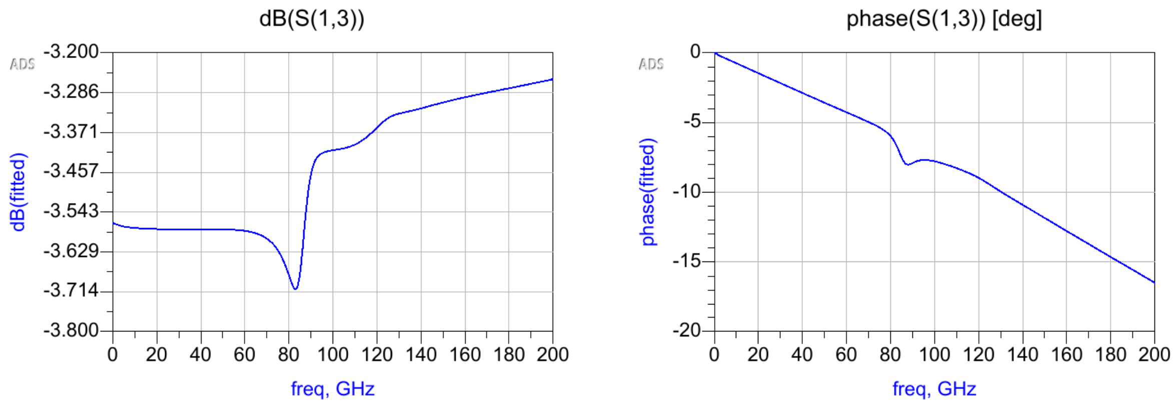


Figure 5. 24: S-parameter S13 coefficient for LO signal path, from the input pin to the HBTs' base, for the mixer core.

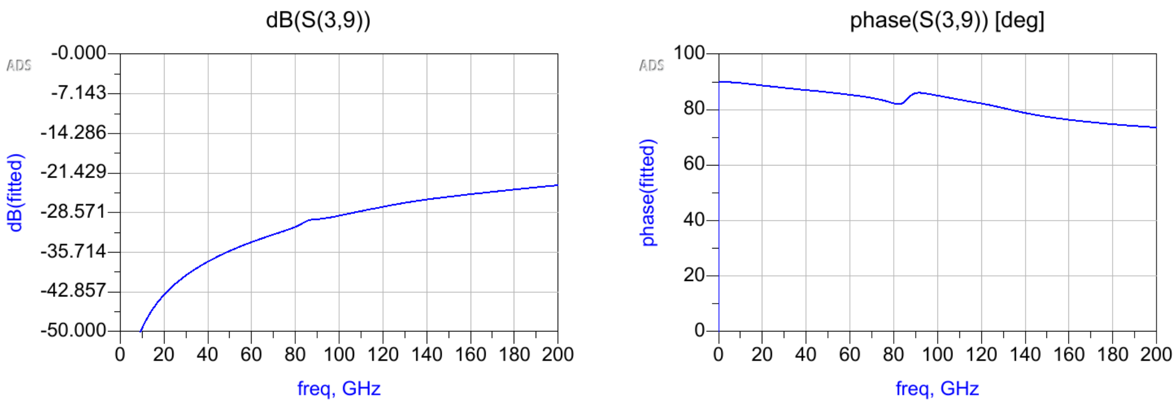


Figure 5. 25: S-parameter S39 coefficient for signal cross from the LO input to the LO output, for the mixer core.

The above tests lead to the conclusion that the proposed mixer-core, in figure 5.15 was more suitable for our layout, than the mixer-core draft1 in figure 5.12.

The next step was to EM simulate the transconductance stage, and the LO and IF inputs and RF output metal connections.

For the proposed mixer core, the following structure, in figure 5.26, was proposed for the transconductance and output RF signal paths. However, the asymmetries in the RF output path (metal 5, with metal 4 ground for return path) cause additional deteriorations, exceeding the design specifications.

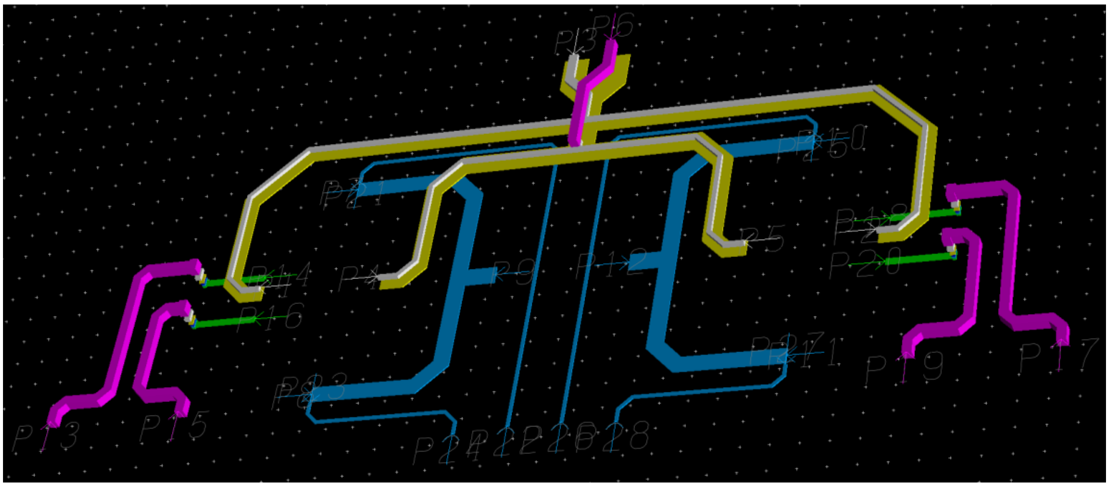


Figure 5. 26: Transconductance stage and connections draft layout of the I/Q Modulator.

As a result, aiming at the symmetry of the output signal path, the following structure was designed, in figure 5.27, and simulated to Momentum.

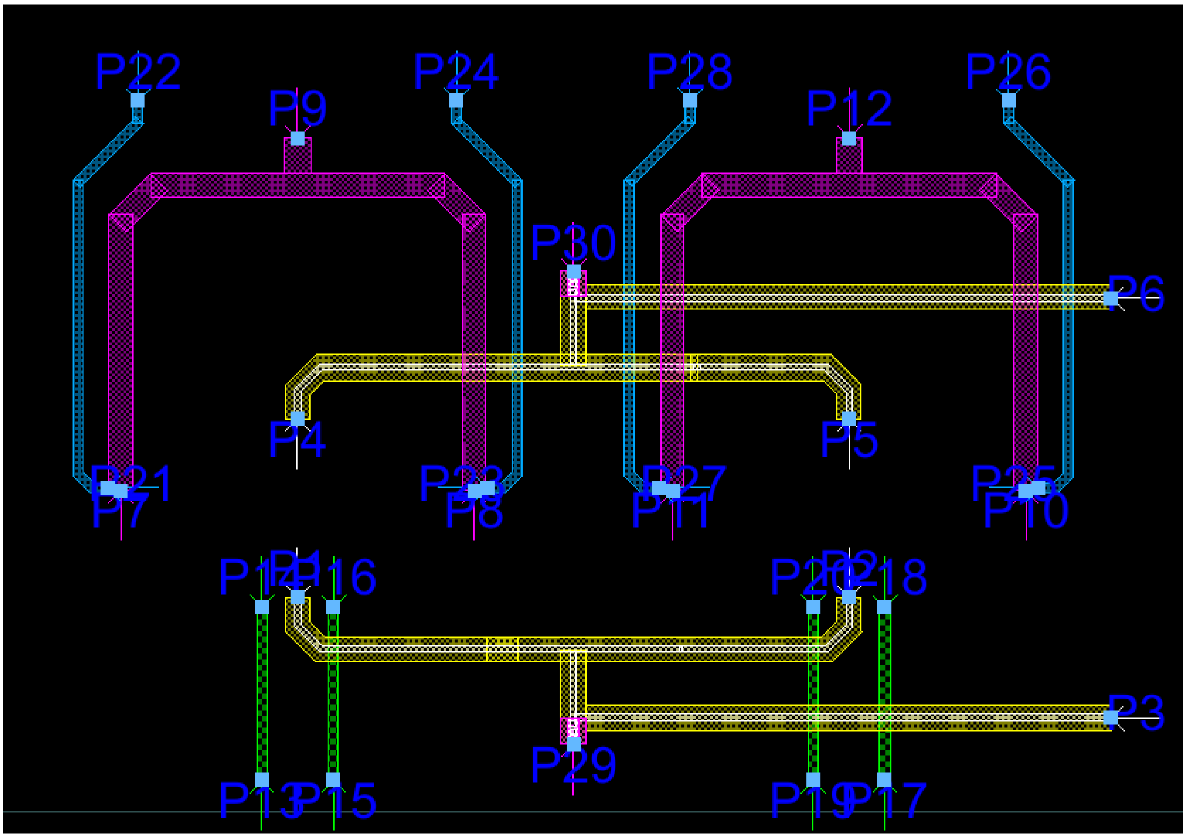


Figure 5. 27: Transconductance stage and connections layout of the proposed I/Q Modulator.

The layout above is 3D illustrated in figure 5.28.

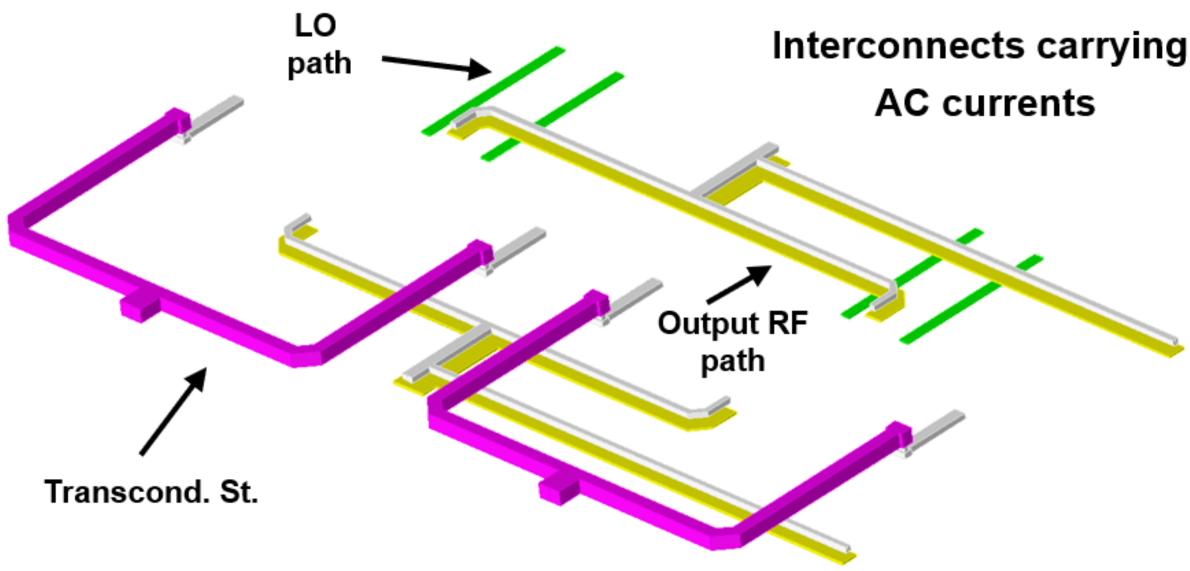


Figure 5. 28: Transconductance stage and connections layout of the proposed I/Q Modulator, 3D illustration.

Again, running the EM simulations for the above parts of the layout, the S-parameter results are imported to Cadence, including the mixer core S-parameter results, and we perform a harmonic balance analysis to the modulator design. In figure 5.29 a deterioration at the LO leakage is notable, with a LO leakage value of 35 dBc.

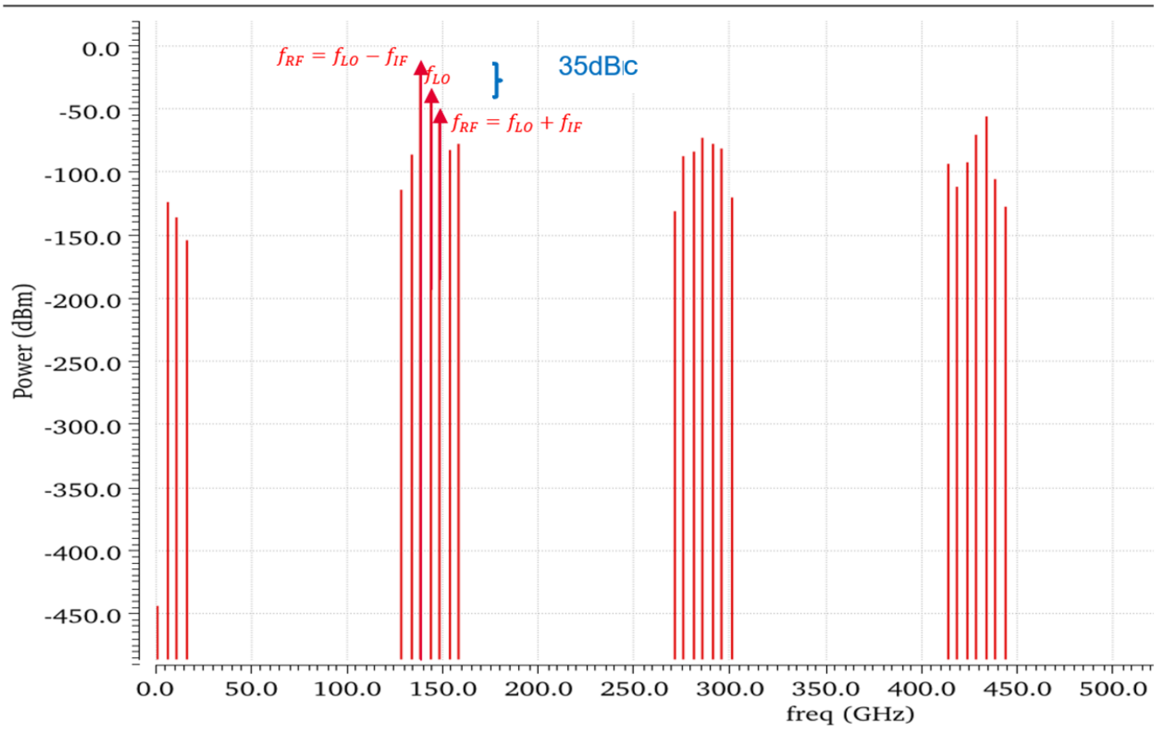


Figure 5. 29: Output spectrum for f_{LO} = 142.5 GHz, P_{LO} = 0 dBm, f_{IF} = 5 GHz, P_{IF} = -30 dBm of LSB Up-Conversion Modulator, replacing the mixer EM results.

Finally, the LO, IF and RF matching networks were designed, in figure 5.30, 5.31 and 5.32, respectively, and simulated in Momentum.

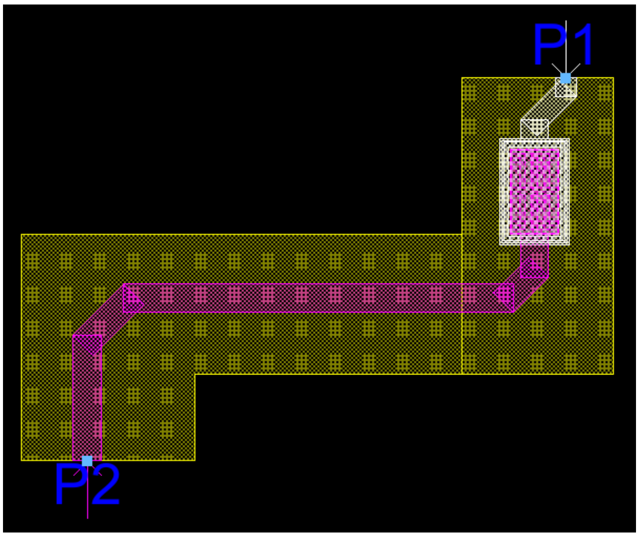


Figure 5. 30: Layout of LO input matching network

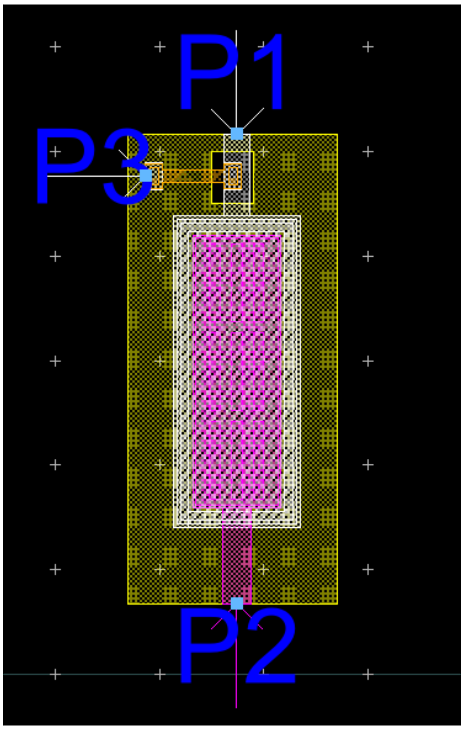


Figure 5. 31: Layout of IF input matching network

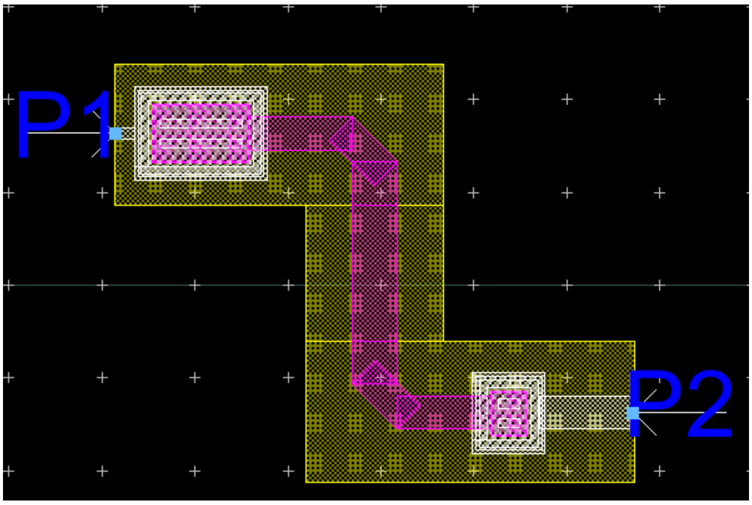


Figure 5. 32: Layout of RF output matching network

5.3 DRC Rules

After the completion of the physical design, as well as the interconnection of the individual parts, an automatic program will check each polygonal element in the drawing according to certain rules and report any violations. This process is called Design Rule Checking (DRC).

The design rules are a set of parameters provided by the semiconductor manufacturers, i.e. by each different technology, that allow the designer to verify the correctness of a mask set. The design rules are specific to a particular semiconductor manufacturing process. A set of design rules specify certain geometric constraints and connectivity constraints to ensure sufficient margins to obtain account for the variability of semiconductor manufacturing processes. This will ensure that all parts function correctly [14]. The basic types of rules are presented in figure 5.33.

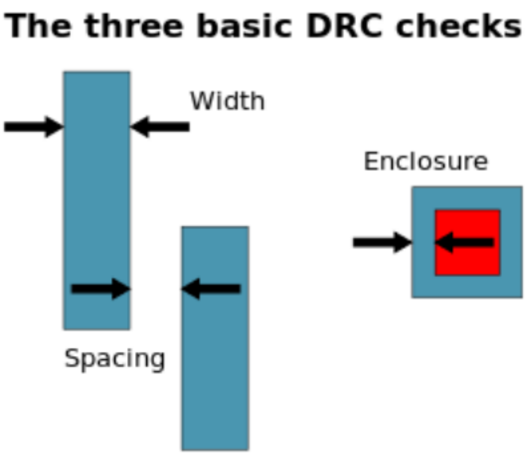


Figure 5. 33: Basic Design Rules

The DRC run was performed in the mixer layout with no errors, as shown in figure 5.34.

Figure 5. 34: DRC-clean.

5.4 LVS Simulation

A successful design rule check (DRC) ensures that the layout conforms to the rules designed/required for the correct construction of the integrated. However, it does not guarantee whether it actually represents the circuit we want to build. This role is performed by the LVS checker. LVS, which stands for Layout versus Schematic is performing a comparison between the layout and schematic that exist in the same cell. The LVS control software recognizes the intended layout patterns representing the electrical components of the circuit, as well as the connections between them. This netlist is compared by the "LVS" software against a similar schematic layout or circuit diagram.

The LVS check includes the following three steps [14]:

- Extraction: The software program takes a database file containing all the layers drawn to represent the circuit in the layout. It then runs the database through several area-based logical operations to determine the semiconductor components represented in the design by their fabrication layers.

- Reduction: The software combines the extracted components in serial and parallel combinations, if possible, and creates a netlist representation of the layout database.

- Comparison: The exported netlist layout is compared to the netlist obtained from the schematic circuit. If the two netlists match, then the circuit passes the LVS check.

It is crucial that the simulation be successful, which was achieved for out layout, as shown in figure 5.35.

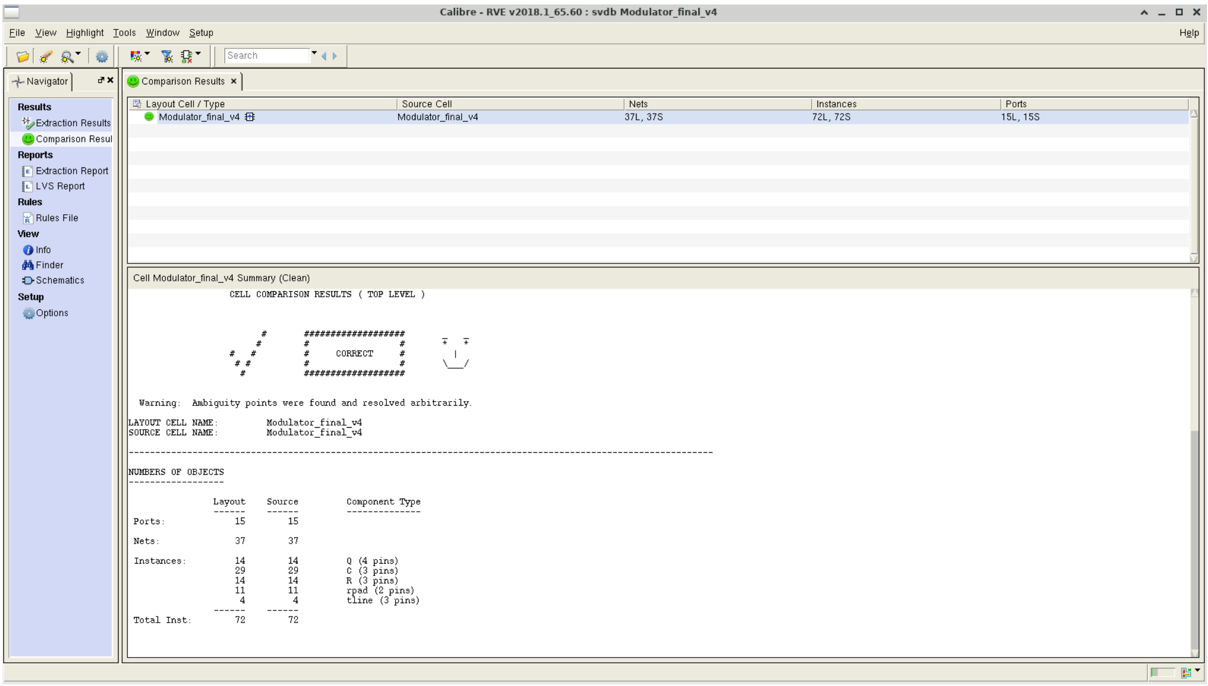


Figure 5. 35: LVS-clean.

5.5 LSB Modulator Performance

A final harmonic balance analysis was carried out on the schematic of the LSB Modulator containing all the elements and interconnections simulated in the Momentum environment. This final schematic simulated in Cadence is presented in figure 5.36 and it consists of n-ports, that represent the S-parameter data, exported form ADS, for all interconnections and elements used in the final layout.

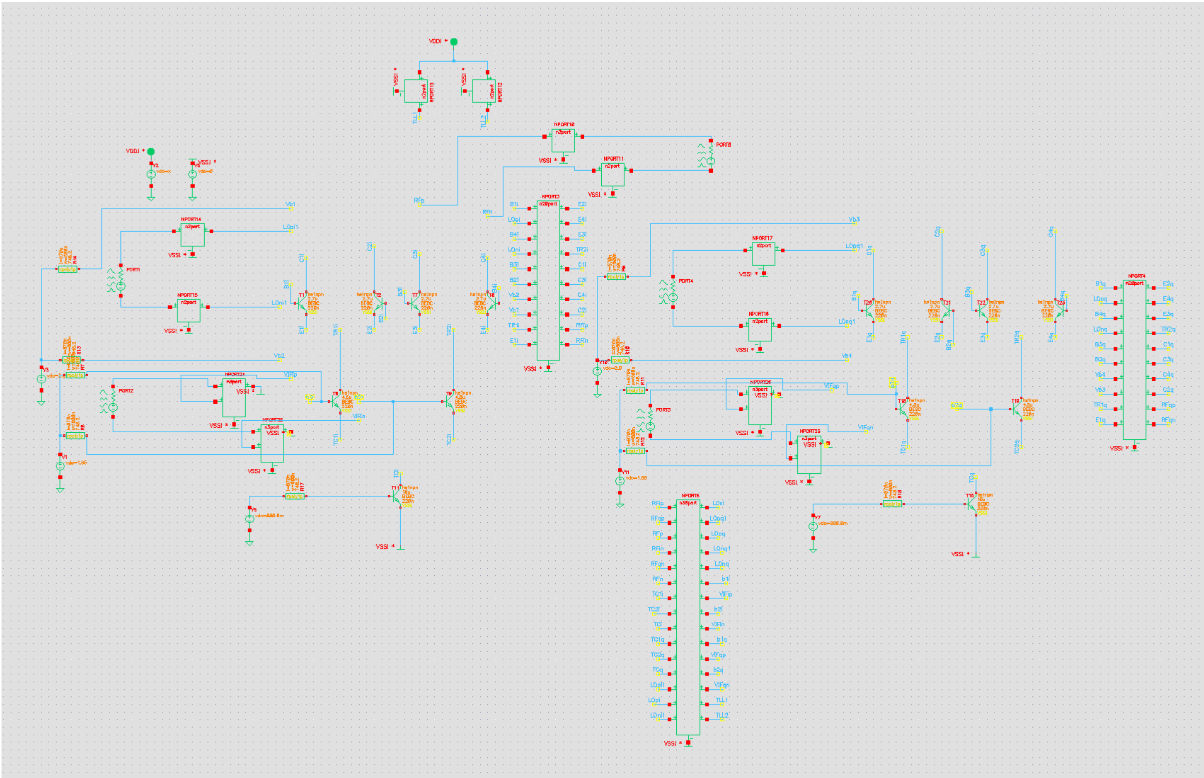


Figure 5. 36: Final Cadence schematic of the proposed I/Q Modulator, containing all S-parameter data from ADS.

The simulation results are presented in the graphs below.

The output spectrum for f_{LO} = 160 GHz, P_{LO} = 0 dBm, f_{IF} = 10 GHz, P_{IF} = -25 dBm, is shown in Figure 5.37. A 40dBc LO rejection, or LO leakage, is accomplished for this frequencies and power levels and a 41dBc image suppression.

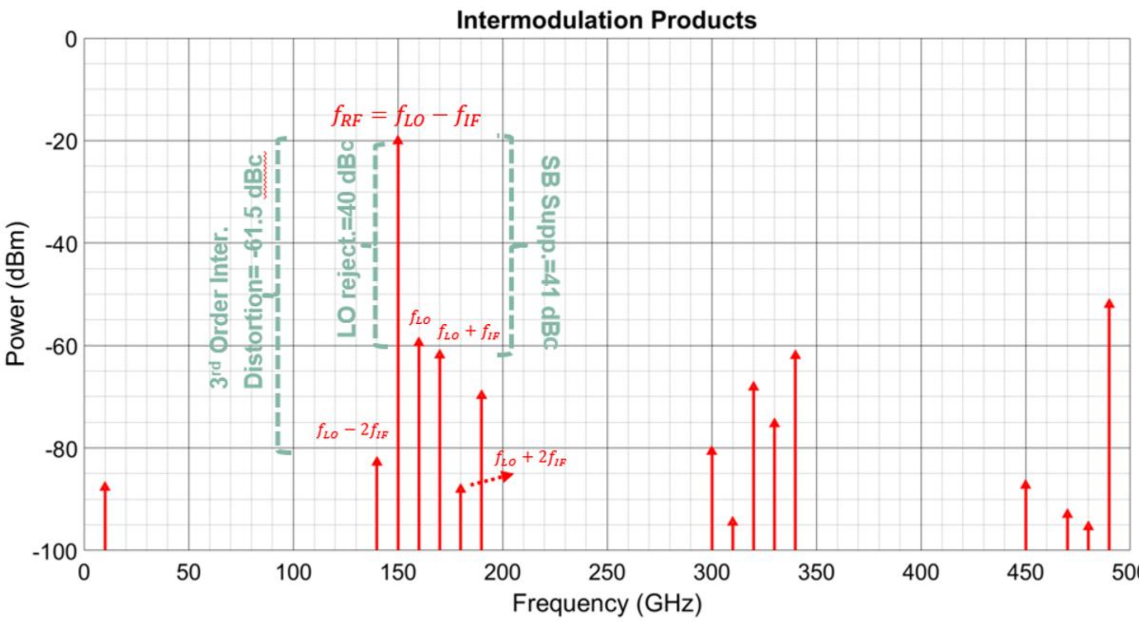


Figure 5. 37: Output spectrum for f_{LO} = 160 GHz, P_{LO} = 0 dBm, f_{IF} = 10 GHz, P_{IF} = -25 dBm of LSB Up-Conversion Modulator.

For the conversion gain versus the IF frequency f_{IF}, for different LO frequencies f_{LO}, the following graph, Figure 5.38, was extracted, indicating, for the whole input frequency range and with IF power equal to -30 dBm, LO power equal to 0 dBm and temperature at 45ºC, an almost flat gain, higher than 5dB.

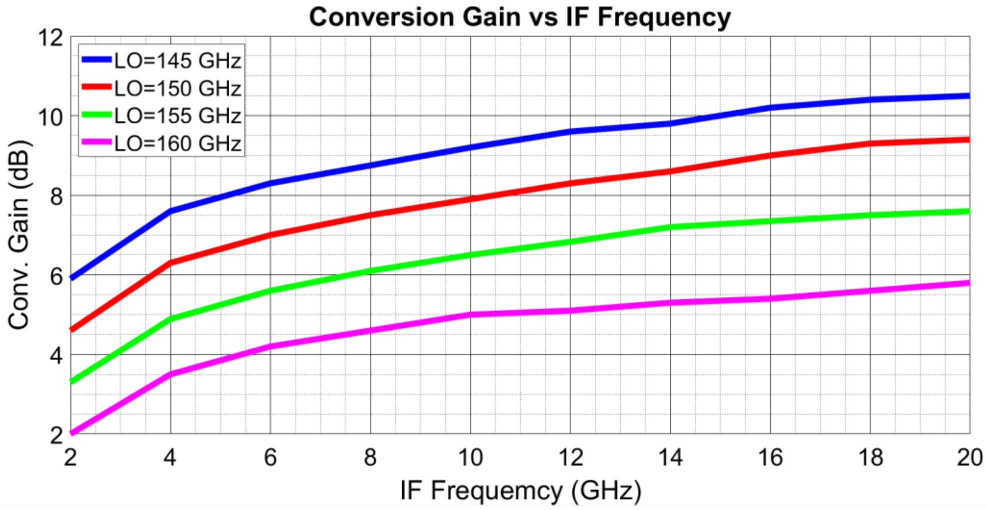


Figure 5. 38: Conversion gain vs. f_{IF} for four different f_{LO} values, P_{LO} = 0 dBm, P_{IF} = -30 dBm of LSB Up-Conversion Modulator.

Also, conversion gain versus IF and LO power is presented in two separate graphs, for IF frequency at 5 GHz, LO frequency at 150 GHz and temperature at 45ºC, Figure 5.39 and 5.40. For the specified power range of operation, sweeping the IF power we get satisfying results for the conversion gain. Sweeping the LO power, in figure 5.39, the conversion gain is lower than expected for LO power below -3dBm and further increase of LO power does not correspond to further increase of the conversion gain, due to mixer's compression.

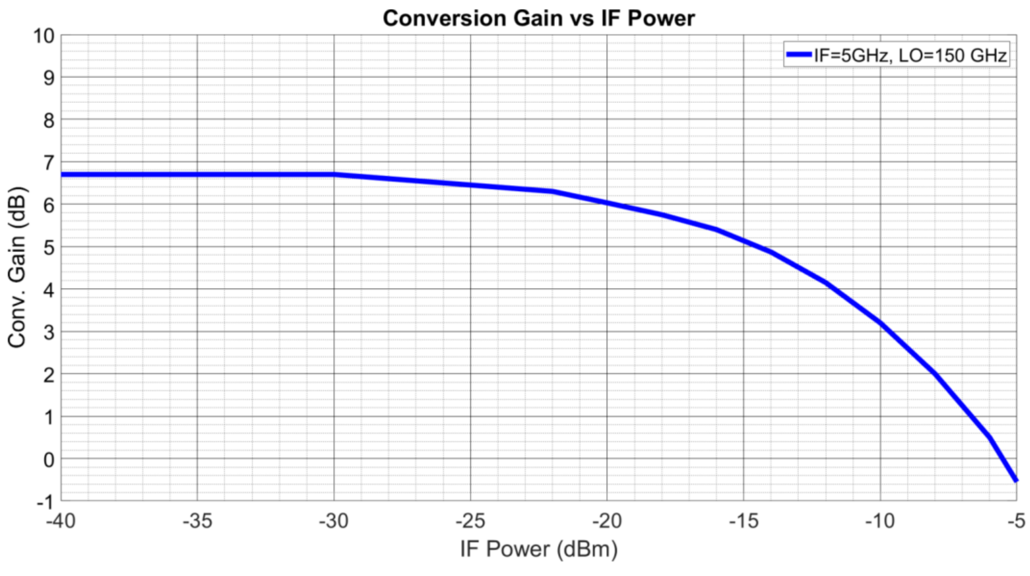


Figure 5. 39: Conversion gain vs. PIF, fLO = 150 GHz, PLO = 0 dBm, fIF = 5 GHz of LSB Up-Conversion Modulator.

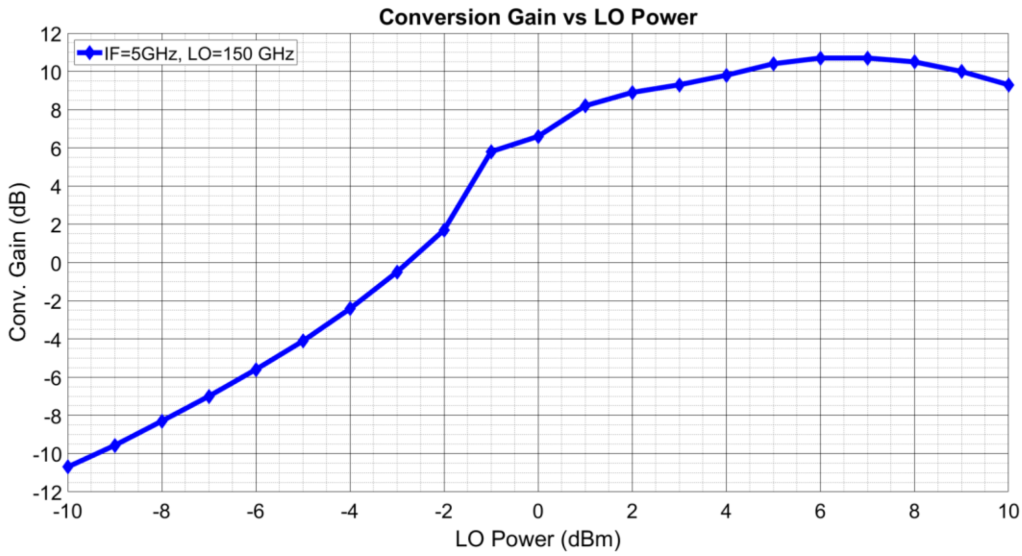


Figure 5. 40: Conversion gain vs. P_{LO}, f_{LO} = 150 GHz, f_{IF} = 5 GHz, P_{IF} = -30 dBm, of LSB Up-Conversion Modulator.

The output power versus input IF power is, also, illustrated at Figure 5.41, for IF Frequency at 10 GHz, LO Frequency at 160 GHz and temperature at 45ºC. The input referred 1dB compression point is around -15dBm and the output referred around -11dBm, for LO power equal to 0dBm.

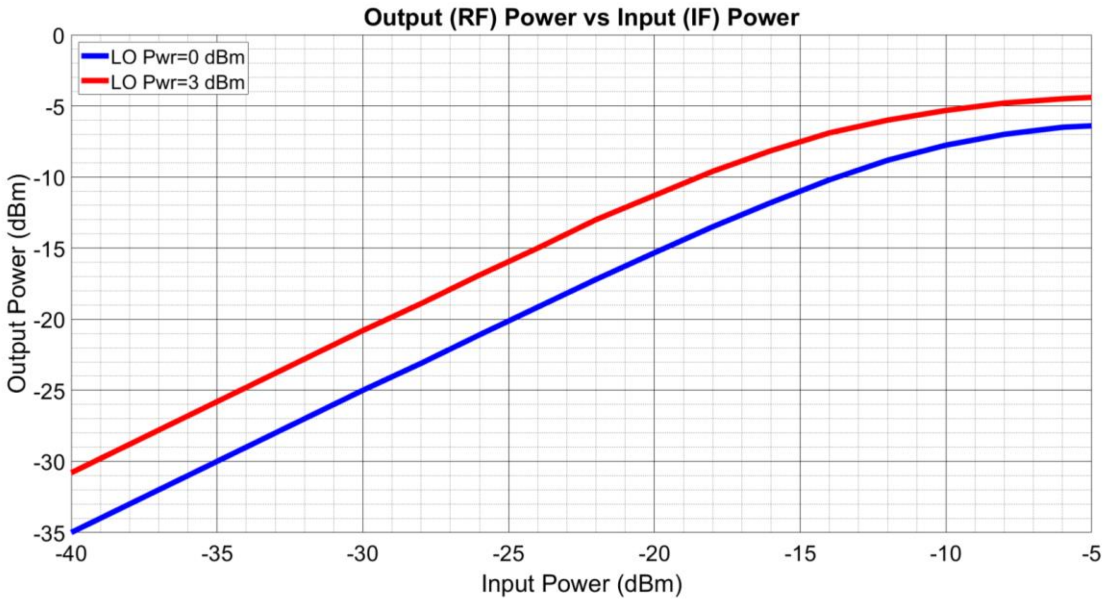


Figure 5. 41: Output power vs. P_{IF}, f_{LO} = 160 GHz, f_{IF} = 10 GHz, for two P_{LO} values, of LSB Up-Conversion Modulator.

A graph representation of the LO leakage is illustrated below, Figure 5.42, versus the LO frequency, for two different LO power levels. In both cases the LO rejection ratio is higher than 35 dBc for the entire LO frequency range. Also, it is clearly denoted that for lower LO power level the LO rejection ratio maintains higher values.

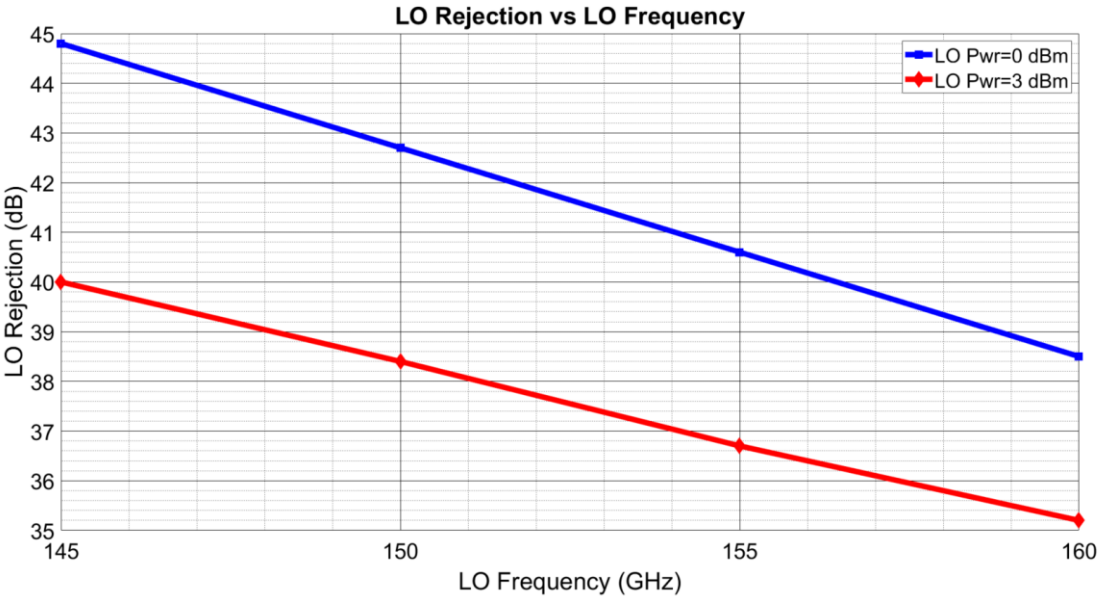


Figure 5. 42: LO Rejection vs. f_{LO}, f_{IF} = 5 GHz, P_{IF} = -25 dBm, T = 45ºC, for LSB Up-Conversion Modulator.

Moreover, the sideband suppression versus the LO frequency is represented in Figure 5.43, similarly, for two different LO power levels. In both cases the sideband suppression is higher than 38 dBc.

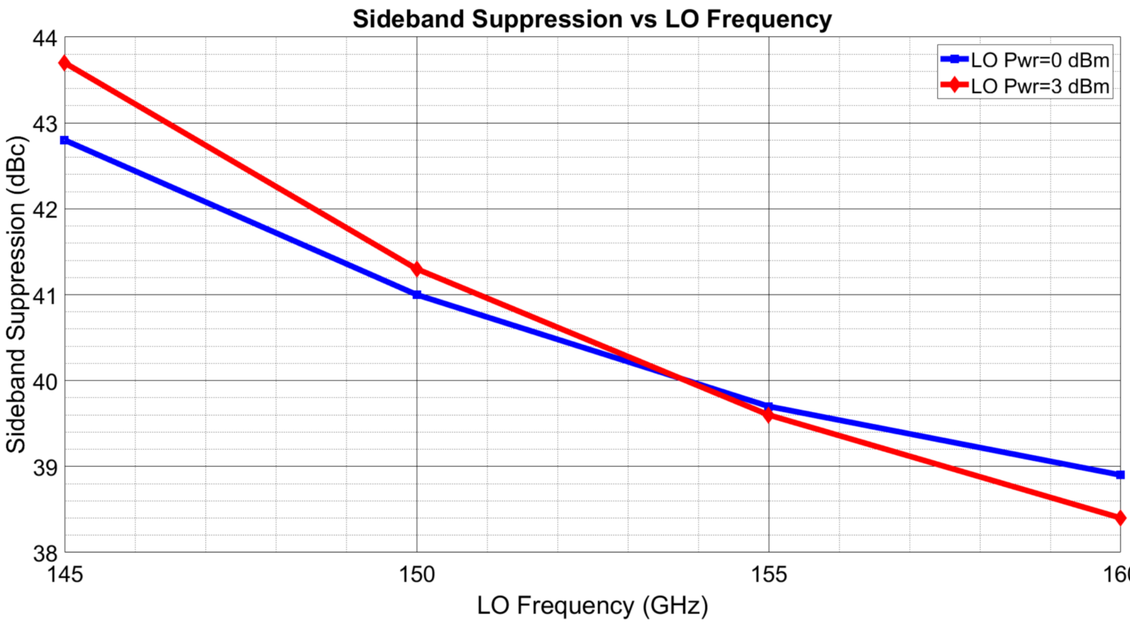


Figure 5. 43: Sideband Suppression vs. f_{LO}, f_{IF} = 5 GHz, P_{IF} = -25 dBm, T = 45ºC, for LSB Up-Conversion Modulator.

Finally, the scattering parameters of the input and output ports, using the matching networks, are depicted in Figure 5.44. The small-signal simulation results show that the LO and RF ports are well-matched to the differential 100 Ω load while the matching at the IF port is almost flat for the frequency band of interest.

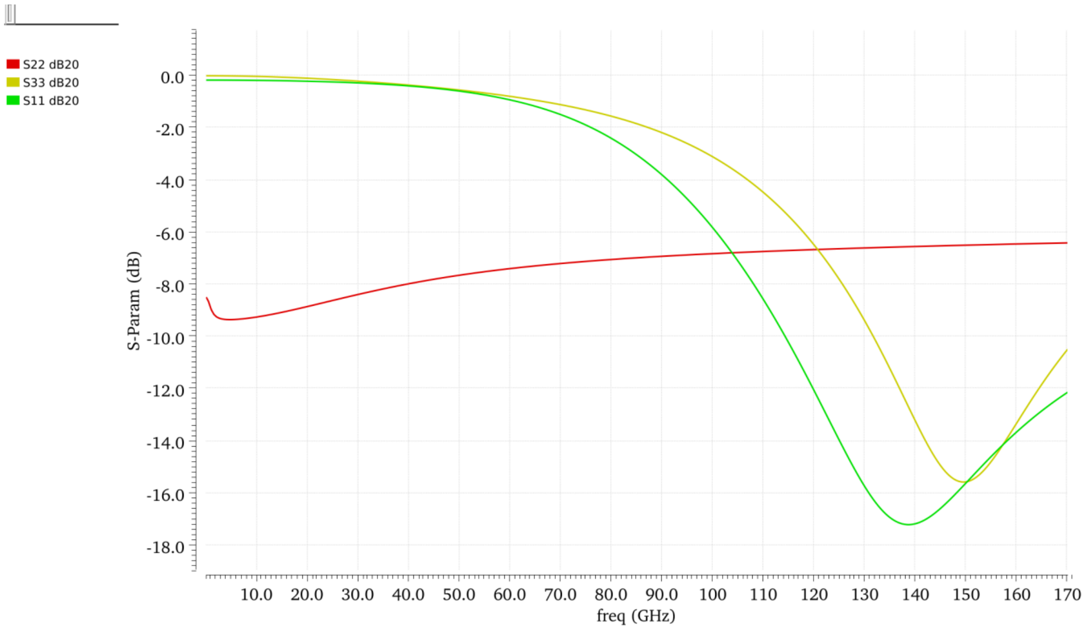


Figure 5. 44: S parameters (reflection coefficients). S11 stands for LO input, S22 for IF input and S33 for RF output.

A summary of the simulation results compared to the initial specifications is presented in Table II.

TABLE II. SUMMARY OF SIMULATION RESULTS

Metrics	***Specification***	***Schematic simulations***	***Layout Simulations***
SSB Conversion Gain	0-10dB	> 10dB	> 5 dB
OP1dB	> -18dBm	~ -3dBm	> -12dBm
OIP3	> -7 dBm	> -7 dBm	> -7 dBm
Power Consumption	< 100mW	~ 90mW	~ 90mW
LO Rejection	> 30dBc	~ 210 dBc	~ 40 dBc
Sideband Suppression	> 35 dBc	~ 240 dBc	~ 40 dBc

Table 5. 1: Summary of simulation results for the I/Q Modulator.

CHAPTER 6: DESIGN OF DOWN-CONVERSION MODULATOR

In this chapter the design of the down-conversion modulator, with 145GHz center frequency, is described. The design was carried out in the Virtuoso® environment of Cadence® while the mixer fabrication technology, is the B11HFC from Infineon Technologies.

The design flow includes the following key points:

1. Establishing the specifications for the performance of the amplifier.

2. Selection of the transistors that characterize the active device of the mixer, based on the transistor models of the technology.

3. Design of the mixing circuit with ideal passive elements of the analog lib library and active HBTs of the technology.

4. Replacing the ideal passive elements with real models of the technology, designing input and output circuits and extracting graphical simulation results (Cadence Virtuoso® Spectre®).

6.1 Targets for mixer performance

For this down-conversion mixer, similarly with the up-conversion mixer, some operational limits were set for both to operate autonomously and to operate within the group project, emphasizing on the following specifications.

Key top-level specifications for the QDB Mixer:

- RF Bandwidth: 30GHz (130GHz-160GHz);
- 3dB RF Signal Power dBm ~ -35 → -5 dBm;
- LO Bandwidth: 30GHz (130GHz-160GHz);
- LO Power ~ -5 dBm → 5 dBm;
- 3dB IF Bandwidth: 20GHz (1-20GHz);
- SSB Conversion Gain: 0 – 10 dB;
- OP1dB more than -18 dBm;
- OIP3 > -7 dBm;
- IRR more than 20 dBc;
- LO-to-IF isolation more than 30 dBc;
- Power Consumption less than 100mW;
- Terminations at 100Ω;

More specifically, all port terminations were designed at 50Ω and, therefore, differentially at 100Ω. Therefore, for all three input and output ports of the circuit it was required to design matching networks at 100Ω. Then, due to the requirements of this telecommunication application, the RF input signal bandwidth is from 130 to 160GHz, with signal power from -35dBm to -5dBm, and the LO bandwidth is required to be from 130GHz to 160GHz, with LO power from -5dBm to 5dBm. The above aim to achieve, approximately, an output IF bandwidth of 20GHz, from 1 to 20GHz. For the specification of conversion gain (CG) it is desired to achieve a value from 5 to 10 dB, and more strictly to be higher than 0dB. The 1dB compression point (output referred) needs to be higher that -18dBm, the 3rd order intercept point (output referred) higher than -7dBm and the image rejection ration (IRR) higher than 20dBc. Moreover, for the power consumption criterion, Pdc (mW), which is required to be the minimum possible, an upper limit of 100mW was set.

The complete receiver chain of the team project is presented below in figure 6.1, with the mixing stage designed and implemented in the context of this thesis indicated by the red frame.

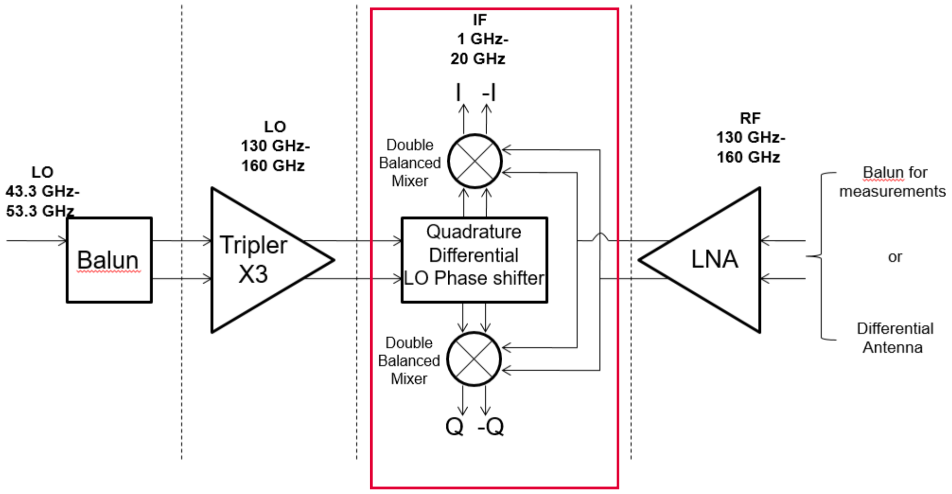


Figure 6. 1: Receiver chain for short-medium range datalinks using PMF

6.2 Demodulator Design

As for the demodulator, a gilbert cell was chosen for the mixer core. Moreover, a buffer was added, as shown in figure 6.2.

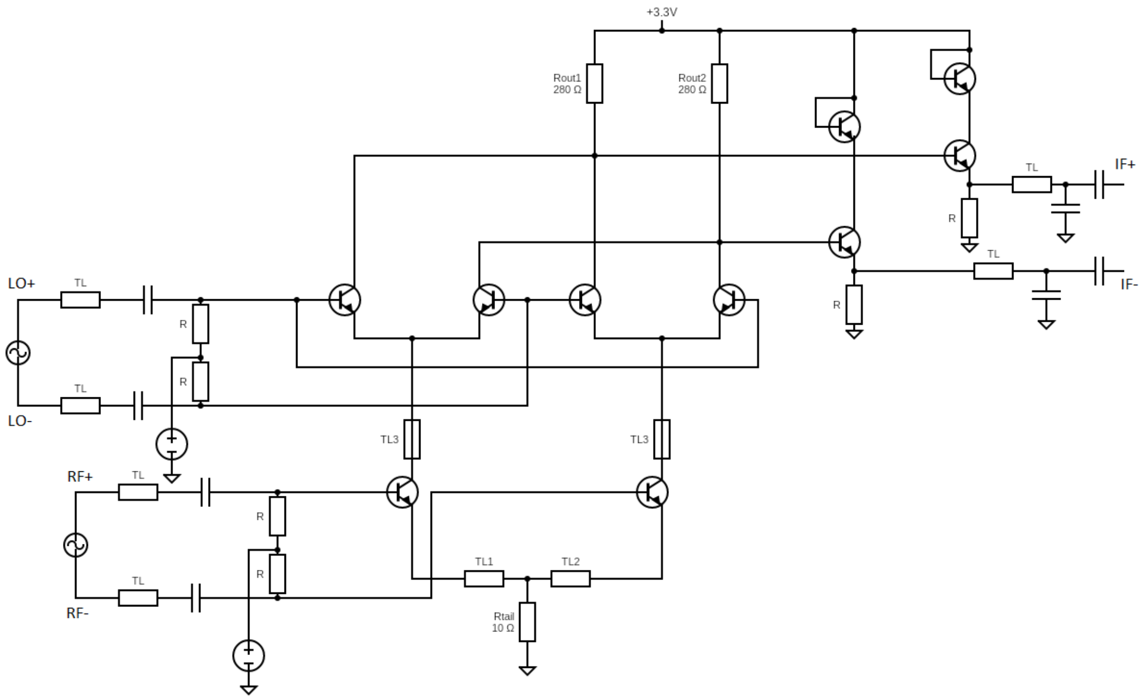


Figure 6. 2: Down-conversion mixer, in gilbert cell topology with a buffer stage.

From the above figure we can identify some basic parts of our circuit.

First of all, the Vcc supply voltage is applied to the output matching network and the other dc voltage sources are applied at the base of the HBTs in order to properly bias the transistors.

In addition to the known gilbert cell, three RC matching networks are used, one for each port. It should be noted that all ports are differential, which is indicated by the plus (+) and minus (-) indexes in each port, LO, RF and IF.

The supply voltage was selected similarly for the demodulator, as for the modulator.

6.3 Selection of the active and passive devices

The HBT that was used for this circuit was the high speed npn. Different emitter lengths were set for each stage, but the same emitter width, with the value of 0.22μm, was used.

According to figure 3.3 for the current density, it is suggested that for optimal operation the HBT should have a current density around 10 to 14 mA/μm^2.

For the switching stage, as the name implies, transistors are biased near to pinch-off region to act as switches at LO frequency, from 130GHz to 160GHz. Thus, it is needed these transistors to have small dimensions and, of course, to use the high speed npn transistor model. Nevertheless, for the switching stage, it is suggested the transistors to be biased with current density that equals to $f_T/1.5$ at figure 3.3.

For the transconductance stage, which converts the RF voltage signal to current, transistors have emitter lengths equal to 4.3um and are biased to operate in saturation region, with current density that equals to f_T. Transistors at the transconductance stage have higher emitter length than those at the switching stage, because the quiescent current is doubled, but not too high, as the RF input port is tuned for D-band frequencies, from 130GHz to 160GHz. The tail-current consists of a 10 Ohm TaN resistor, to minimize the demanding voltage range.

Tlines TL1 and TL2, used as emitter degeneration, improve the linearity of the mixer and rpoly at the output, act as load to increase conversion gain [13].

A second stage of two emitter followers, for each output, is added, to act as an output buffer.

On-chip matching networks are added at all ports to achieve the broadband frequency tuning. DC biasing is provided through rpoly resistors, for the switching and transconductance stage, and independent voltage sources and the main supply voltage, at the level of 3.3V, is provided through the output resistors, of 280Ohm.

6.4 Demodulator Design

For the demodulator we employ two such mixers, separately operating, receiving the same differential RF input, while the LO input is received differentially in quadrature.

The demodulator design in Cadence is presented below for the I demodulator, figure 6.3.

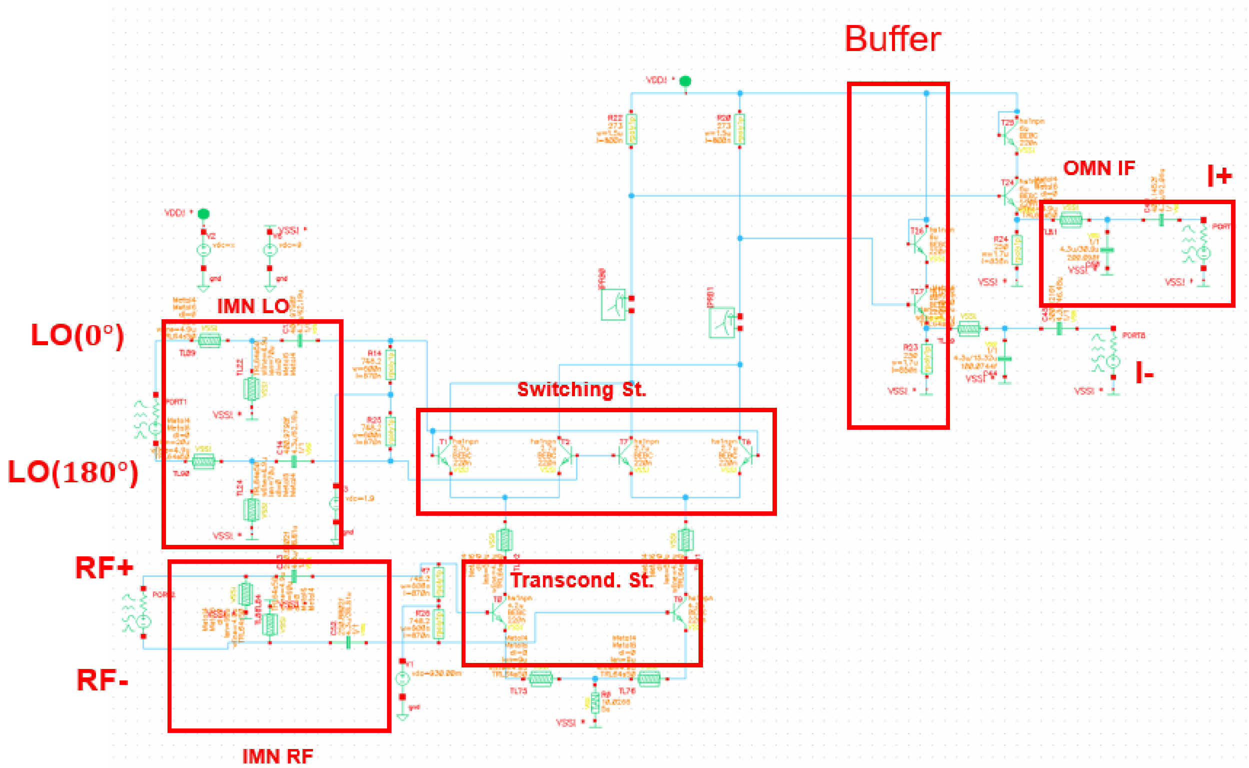


Figure 6. 3: Demodulator schematic in Cadence.

6.5 Simulations

Similar simulations, on schematic level, were performed for the demodulator, to characterize the design. The same analysis, HB, trans, SP, DC, were used for this purpose.

The output spectrum for f_{LO} = 150 GHz, P_{LO} = 0 dBm, f_{RF} = 140 GHz, P_{RF} = -20 dBm, is shown in Figure 6.4.

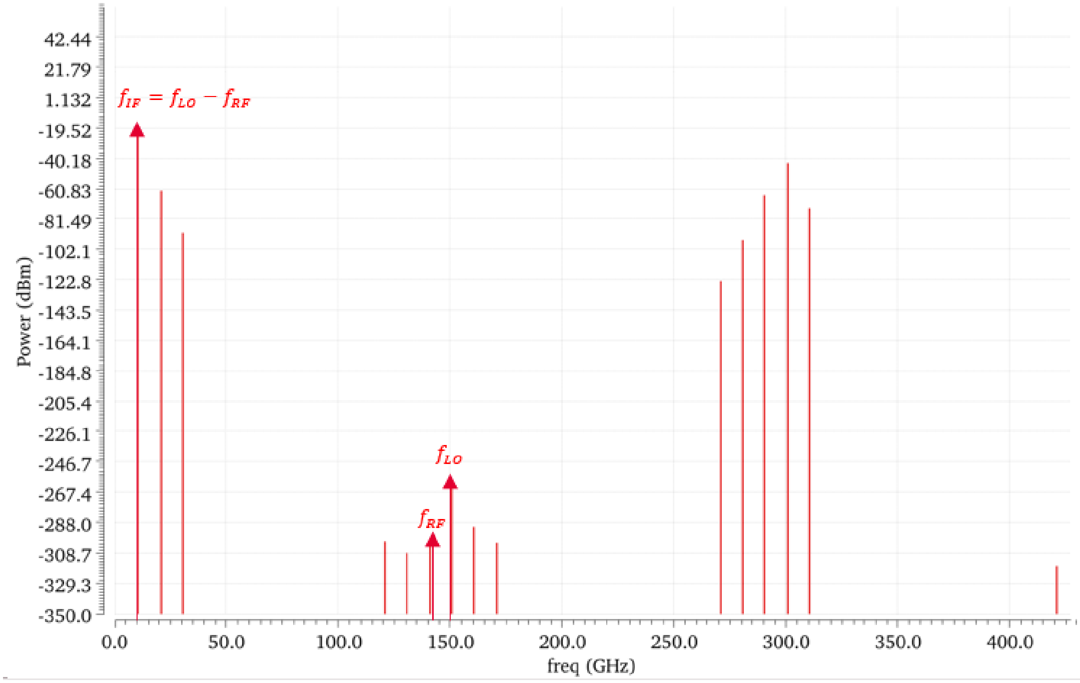


Figure 6. 4: Output spectrum for f_{LO} = 150 GHz, P_{LO} = 0 dBm, f_{RF} = 140 GHz, P_{RF} = -20 dBm of Demodulator.

For the conversion gain versus the RF frequency f_{RF}, for different LO frequencies f_{LO}, the following graph, Figure 6.5, was extracted, which indicates that the conversion gain specification, for all input frequencies and with RF power equal to -20 dBm, LO power equal to 0 dBm and temperature at 45ºC, is satisfied.

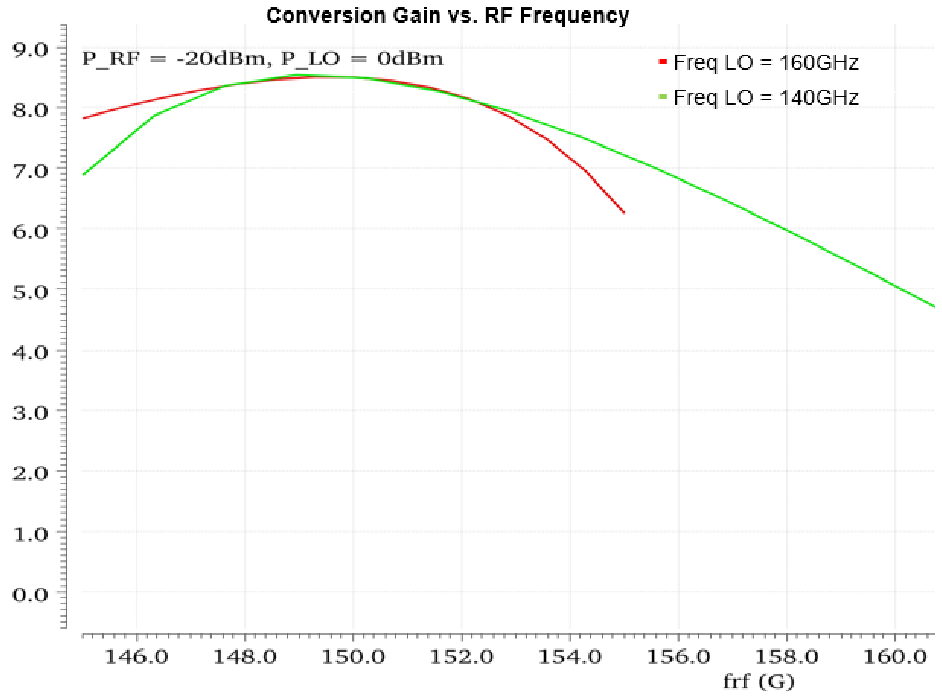


Figure 6. 5: Conversion gain vs. f_{RF} for two different f_{LO} values, P_{LO} = 0 dBm, P_{RF} = -20 dBm of Demodulator.

Also, conversion gain versus RF and LO power is presented in two separate graphs, for RF frequency at 140 GHz, LO frequency at 150 GHz and dBm and temperature at 45ºC, Figure 6.6 and 6.7.

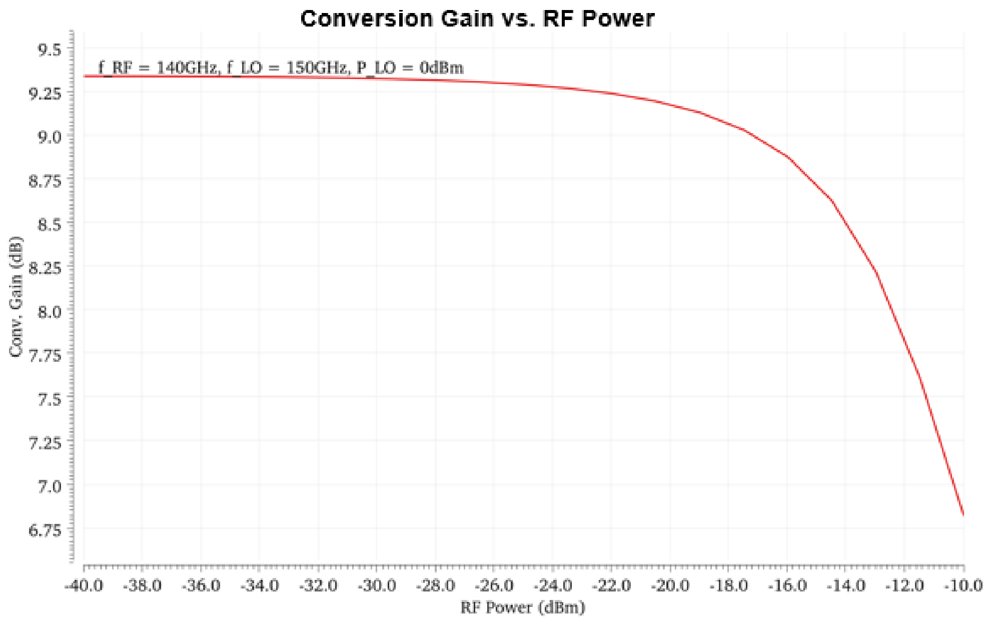


Figure 6. 6: Conversion gain vs. P_{RF}, f_{LO} = 150 GHz, P_{LO} = 0 dBm, f_{RF} = 140 GHz of Demodulator.

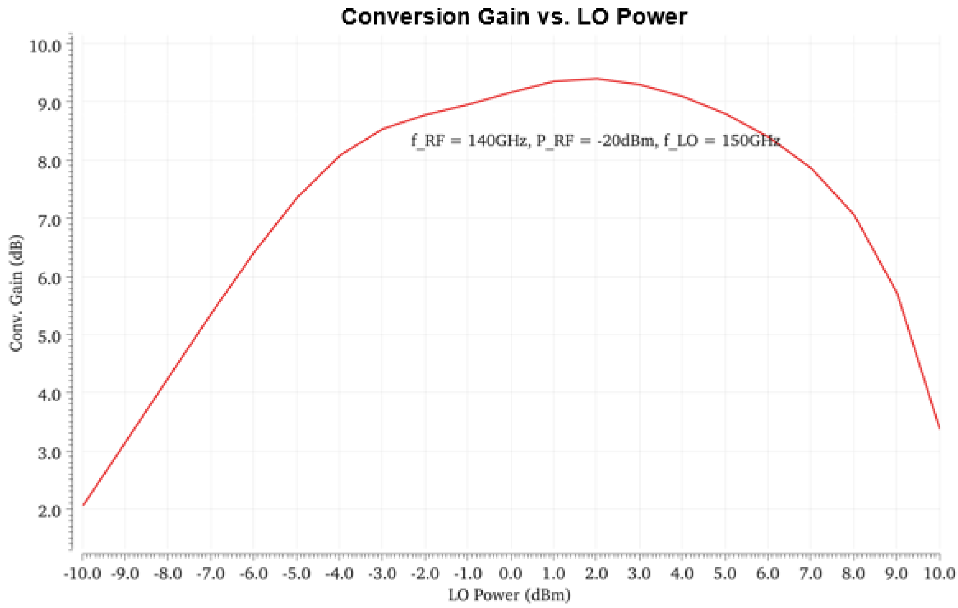


Figure 6. 7: Conversion gain vs. P_{LO}, f_{LO} = 150 GHz, f_{RF} = 140 GHz, P_{IF} = -20 dBm, of Demodulator.

The output power versus input RF power is, also, illustrated at Figure 6.8, for IF Frequency at 140 GHz, LO Frequency at 150 GHz and temperature at 45ºC. The input referred 1dB compression point is around -12.2dBm and the output referred around -5.5dBm, for LO power equal to 0dBm.

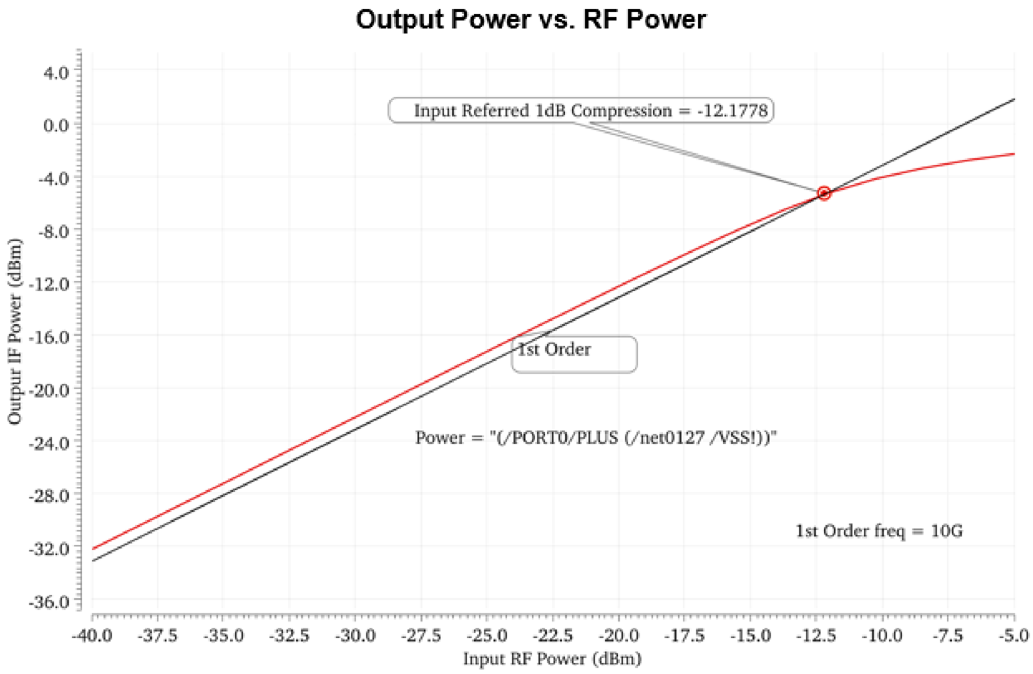


Figure 6. 8: Output power vs. P_{RF}, f_{LO} = 150 GHz, f_{RF} = 140 GHz, P_{LO} = 0dBm, of Demodulator.

In addition, the third-order intercept point is illustrated in Figure 6.9.

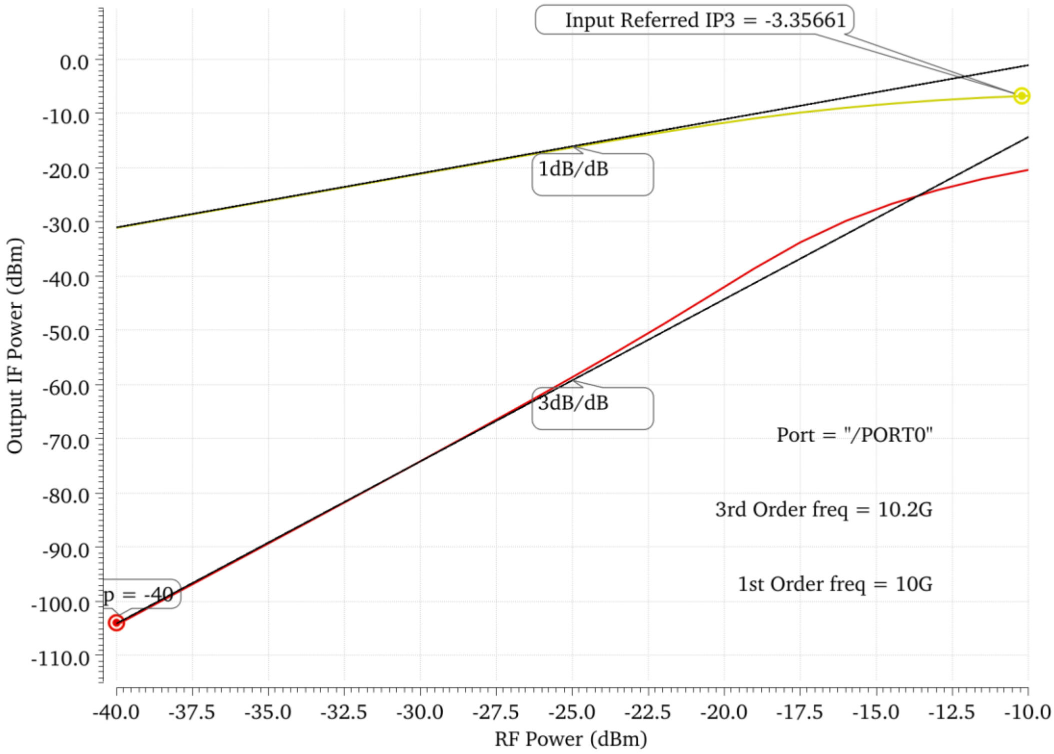


Figure 6. 9: Output power vs. P_{RF}, f_{LO} = 150 GHz, f_{RF} = 140 GHz, P_{LO} = 0dBm, IIP3 = -3.36dBm, of Demodulator.

Finally, the scattering parameters of the input and output ports, using the matching networks, are depicted in Figure 6.10.

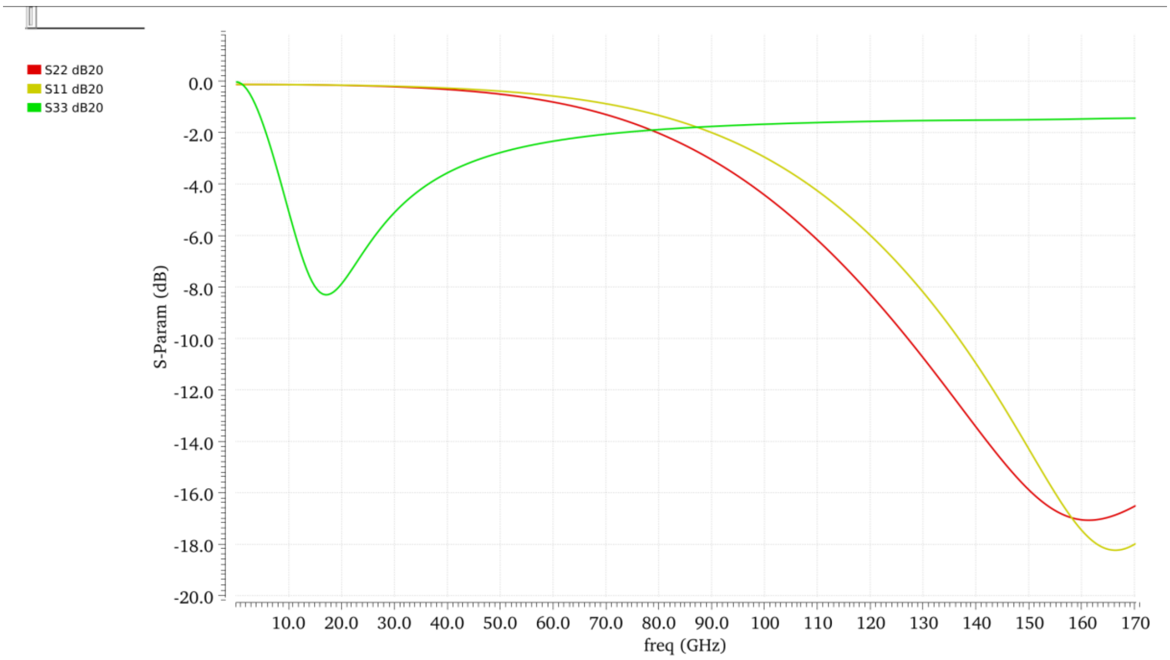


Figure 6. 10: S parameters (reflection coefficients). S11 stands for LO input, S22 for RF input and S33 for IF output.

Also, other coefficients that prove the ports isolations are presented below, figure 6.11.

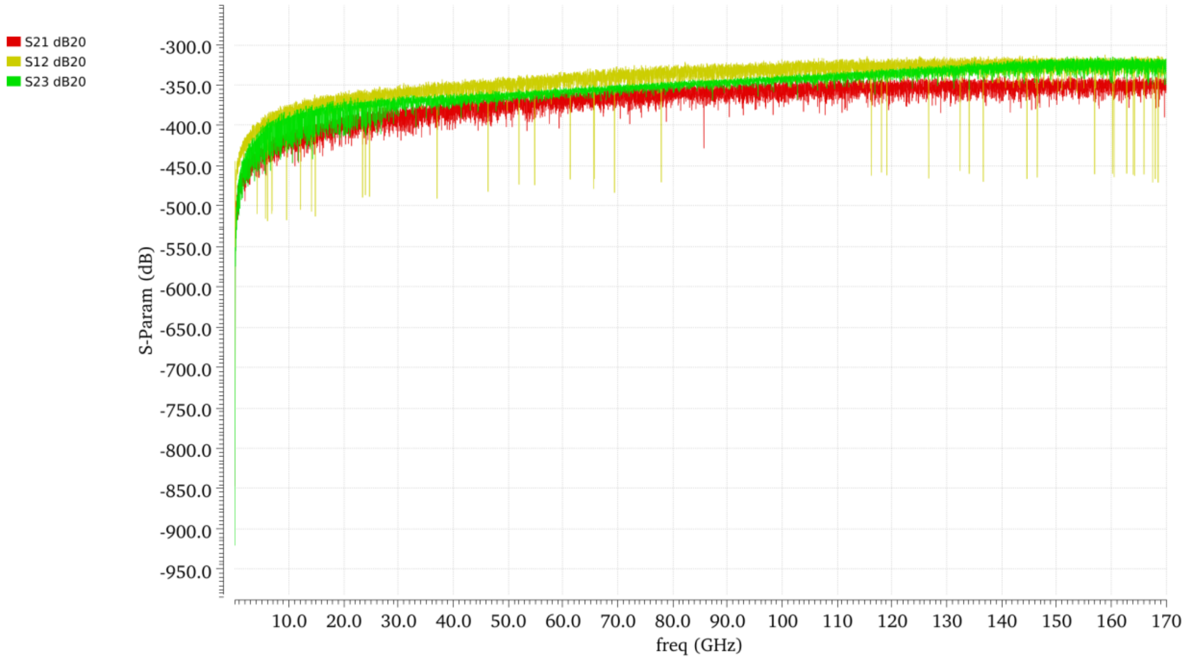


Figure 6. 11: Scattering coefficients for port isolation, from SP Analysis 0-170GHz, of demodulator.

A summary of the simulation results is presented in Table III.

TABLE III. SUMMARY OF SIMULATION RESULTS

Metrics	***Specification***	***Simulated***
SSB Conversion Gain	0-10dB	> 5 dB
OP1dB	> -18dBm	> -12.2 dBm
IIP3	> -7 dBm	> -3.4 dBm
Power Consumption	< 100mW	~ 90mW
LO Rejection	> 30dBc	~ 200 dBc

Table 6. 1: Summary of simulation results for the I/Q Demodulator.

CHAPTER 7: CONCLUSION AND FUTURE WORK

In this work, we implemented an active double-balanced, up-conversion mixer, in gilbert cell topology from schematic level to layout level and an active double-balanced, down-conversion mixer, in gilbert cell topology in schematic level, both with 145GHz center frequency. The mixer is one of the most important components in microwave and millimeter-wave telecommunication systems and, therefore, was a crucial part of the team project of short-medium range datalinks, using PMF. The main challenge of design and implementation was to achieve the demanding specifications but, as it turned out, it was LO leakage that determined the course of the layout design, due to the high frequencies causing strong parasitic phenomena.

The performance of the modulator, as is already presented in Table5, is satisfying, as all specifications are within the suggested limits. More specifically, for the LSB up-conversion modulator the SSB Conversion Gain was above 5dB for the whole frequency range, a logical value for an active mixer but demanding for a frequency range of 30GHz, and the LO Rejection and the Sideband Suppression were both around 40dB, implying an optimal behavior in the rejection of unwanted frequencies. The OP1dB was -11dBm and the OIP3 around -6dBm, maintaining the desired linearity limits. Finally, the Power Consumption was limited to around 90mW. the minimum area of 0.455mm^2 is occupied by the complete layout.

Respectively for the demodulator, similar simulation results were extracted from the schematic level. The SSB Conversion Gain was above 5dB for the whole frequency range, a logical value for an active mixer but demanding for a frequency range of 30GHz, and the LO Rejection was around 200dB. The OP1dB was -12dBm and the OIP3 around -3.5dBm, maintaining the desired linearity limits. The Power Consumption level was again around 90mW.

The modulator circuit is currently under construction and, therefore, the next steps include the measurement of the integrated circuit, in order to confirm the results of the simulations, to identify the deviations and improve the design to further enhance its performance. Also, an important step would be to implement the demodulator's physical design too, or else the layout, to obtain a complete picture for mixers in the D-band.

A performance comparison between the proposed design and the state-of-the-art I/Q modulators is provided in Table IV. It should be noted that the performance of the current work is related to simulation results.

TABLE IV

COMPARISON TABLE OF PUBLISHED D-BAND I/Q MODULATORS

Ref.	Process	Freq.	Conv. Gain (dB)	LO-RF (dB)	RF/IF BW (GHz)	P_{dc} (mW)
This work	130 nm SiGe BiCMOS	120-160	>5	>35	40/20	90
[6]	250 nm SiGe BiCMOS	150-168	34	-	-	610
[24]	130 nm SiGe BiCMOS	119-152	9.8	31	33/13	53
[25]	65 nm CMOS	144	9.7	-	3.3/	219

Table 7. 1: Comparison table of published D-band I/Q Modulators.

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