NATIONAL TECHNICAL UNIVERSITY OF ATHENS

SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

DEPARTMENT OF COMMUNICATIONS, ELECTRONICS AND COMPUTING SYSTEMS

Design and implementation of an integrated frequency multiplier, with operating frequency range 130-160 GHz, in 130nm SiGe BiCMOS technology

DIPLOMA THESIS

Panteleimon Gavalas

Supervisor: Ioannis Papananos

Professor NTUA

ELECTRONICS LABORATORY

Athens, September 2022

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Περίληψη

Στην διπλωματική αυτή εργασία πραγματοποιείται η ανάλυση, η σχεδίαση και η υλοποίηση ενός ολοκληρωμένου πολλαπλασιαστή συχνοτήτων, δύο σταδίων, ακολουθούμενου από έναν τρισταδιακό ενισχυτή ισχύος, σε μικροκυματικές συχνότητες και στην τεχνολογία SiGe BiCMOS 130nm. Συγκεκριμένα, παρατίθενται με αναλυτικό τρόπο η αρχιτεκτονική και τα βήματα που ακολουθήθηκαν για την κατασκευή του προαναφερθέντος πολλαπλασιαστή και ενισχυτή, σε κεντρική συχνότητα 145GHz, με εύρος λειτουργίας 130-160GHz. Στην εργασία παρουσιάζεται η διαδικασία, ενώ πραγματοποιείται και η σύγκριση των επιδόσεων μεταξύ των σταδίων της σχεδίασης, δηλαδή την μετάβαση από επίπεδο ιδανικού σχηματικού στο επίπεδο layout του τελικώς υλοποιήσιμου κυκλώματος.

Αρχικά, παρουσιάζεται ο ρόλος του κυκλώματος και σχολιάζεται η θέση του στην αλυσίδα ενός σύγχρονου πομποδέκτη στα προϊόντα τεχνολογίας D-band συχνοτήτων. Εν συνεχεία, αναλύονται θεωρητικά οι προδιαγραφές και τα χαρακτηριστικά των ολοκληρωμένων κυκλωμάτων πολλαπλασιαστών συχνοτήτων, ενώ μετέπειτα ακολουθεί η ανάλυση του κυκλώματος, εκκινώντας από το σχηματικό, ιδανικό επίπεδο κατευθυνόμενοι προς το επίπεδο layout του επιλεγμένου πολλαπλασιαστή και ενισχυτή.

Τέλος, πραγματοποιείται η παρουσίαση των αποτελεσμάτων των προσομοιώσεων του κυκλώματος καθώς και πιθανές βελτιώσεις που θα μπορούσαν να λάβουν χώρα, ως μελλοντική εργασία πάνω στο συγκεκριμένο ολοκληρωμένο.

Λέξεις Κλειδιά: πολλαπλασιαστής συχνοτήτων, ενισχυτής ισχύος μικροκυματικών συχνοτήτων, SiGe, BiCMOS, 130nm, 145GHz, εύρος λειτουργίας, layout.

Abstract

In the present thesis, the realization of the analysis, design and implementation of an integrated, two-stage, Frequency Multiplier, followed by a three-stage Power Amplifier, operating at mm-wave frequencies and fabricated in a 130nm SiGe BiCMOS technology takes place. Specifically, the architecture and the steps followed for the implementation of the aforementioned Frequency Multiplier and Power Amplifier, in a central frequency of 145GHz, with a bandwidth of 130-160GHz, are listed in an analytical way. In the thesis, the entire procedure is represented, while the comparison of the performance between the design stages, which is the transition from an ideal schematic level to the layout level of the manufactured circuit, is realized.

Initially, the work presents the role of the circuit and comments on its position in the chain of a modern transceiver used for products of D-band frequencies. Continuing, it theoretically analyses the specifications and characteristics of the integrated Frequency Multipliers, while subsequently, it follows to analyze the entire circuit, starting from the ideal, schematic level and moving towards the layout of the chosen Frequency Multiplier and Power Amplifier.

Finally, the presentation of the results, provided by the simulations realized on the circuit and the several, possible improvements that could occur as a future work on this integrated circuit, takes place.

Key words: Frequency Multiplier, mm-wave frequency Power Amplifier, SiGe, BiCMOS, 130nm, 145GHz, bandwidth, layout.

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First of all, I would like to thank my professor, Ioannis Papananos, for his guidance and for our excellent and effective cooperation. Furthermore, for the opportunity that he gave me to work on this thesis at Infineon Technologies AG, in Villach, Austria, where and through this professional environment I gained knowledge, experience and met a lot of people. In addition, I would like to thank Franz Dielacher and Siegfried Krainer for giving me the opportunity to work in this team and for our smooth cooperation.

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Chapter 1 - Introduction

1.1 Motive and mm-Wave Frequency Spectrum

As there is an increasing congestion in the low frequency bands, there is an impetus to explore the untapped higher frequency bands. These underutilized bands are the sub-terahertz frequencies, which lie between millimeter waves and infrared light, and range from 0.1 to 10 THz.

This frequency band is particularly attractive for wireless communications because of the high bandwidth that can be obtained, possibly solving the problem of high mobile traffic and addressing the demand for ultra-fast communication systems. At the same time, it satisfies the ever-increasing demand for spectral resources [1][2]. In addition, it promises high data rates of more than 10 Gbps [3].

Taking into consideration Edholm's law of bandwidth, over the last two decades, the demand for bandwidth has doubled every 18 months for short-range communications [2]. From Figure 1.1, we see that according to Edholm, wired communications will soon one day be a thing of the past [2][4].

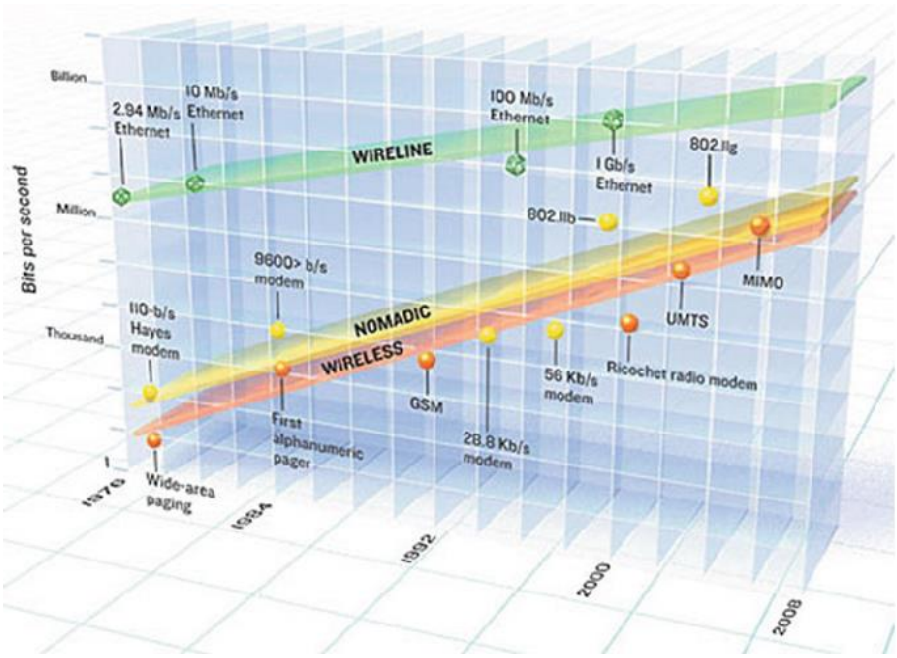

Figure 1. 1 - Edholm's law for the convergence of the three descents in telecommunications

In addition to wireless communication, other applications require high frequencies. One such application is spectroscopy, as high frequencies produce sharper images. In addition, the medical sector is another area for the application

of these high frequencies, as they are not harmful to soft tissues and would provide an alternative to X-rays and other imaging systems.

While their advantages are many, these high frequencies are particularly difficult to achieve in electronics. Research into them is ongoing, with the aim of bridging the gap between the theories, already developed, in the tools needed to implement high frequency applications. There are limitations in semiconductor devices that prevent the design of hardware for extremely high frequencies. However, because the demand for high frequencies remains, research teams continue to develop new designs to achieve electronic devices that can facilitate high frequency applications.

In order to meet this demand, electrical engineers have attempted to use various means to achieve millimeter wave and terahertz frequencies. Although optoelectronic devices, quantum cascade lasers (QCL) and other still nano devices have been explored to generate these high frequencies, they lack the advantages possessed by silicon devices [1]. Silicon devices are inexpensive and readily available. In addition, they are not as bulky as some of the alternative devices and can operate reasonably well in uncontrolled environments [1].

In addition, as the frequency increases, the oscillator application is plagued by phase noise and instability. Interleaving therefore a low frequency oscillator with a frequency multiplier is one way to solve this problem [5].

1.2 Brief Introduction to Frequency Multipliers

The operation of a frequency multiplier is verbatim - a frequency multiplier is a circuit that takes a signal of a specific frequency at its input and produces harmonic multiples of that frequency at its output. Historically, their use has been widespread, especially in the application of frequency synthesis. When implemented as part of a large system, a chain of multipliers can be used to synthesize multiple signals from a single high-performance oscillator. [6].

Many early frequency multipliers were implemented using vacuum tubes [7], and the devices used for frequency multiplication have varied since then. Any non-linear device, such as tubes, diodes, transistors or even transformers [8] and other circuits, can be used to excite higher harmonics from a signal. For the purpose of this paper, the design is done with HBTs (Heterojunction Bipolar Transistors) as the non-linear element.

1.3 Objective of this Thesis

This thesis presents both the theory and design behind frequency multipliers and develops an intuitive understanding of both parasitic and non-linear operation through the implementation of a, sub-terahertz frequency multiplier for the generation of the LO signal in a transceiver system. The central operating frequency for the output signal is set to 145GHz, while an operating range between 130-160GHz is targeted.

1.4 Structure of the Work

In this work, firstly, a reference to the required theory will be made. Subsequently, the design steps and the gradual transition from the ideal to the real models and subsequently to the layout level will be presented. Finally, the paper will conclude with the presentation of the simulation results and the corresponding conclusions.

Chapter 2 - Frequency Multiplier and Microwave Networks Theory

2.1 Overview of Frequency Multiplier Theory

As mentioned above, a frequency multiplier receives at its input a signal at a particular frequency and extracts a harmonic of that signal. Figure 2.1 shows a simplified, ideal block diagram for the operation of this circuit.

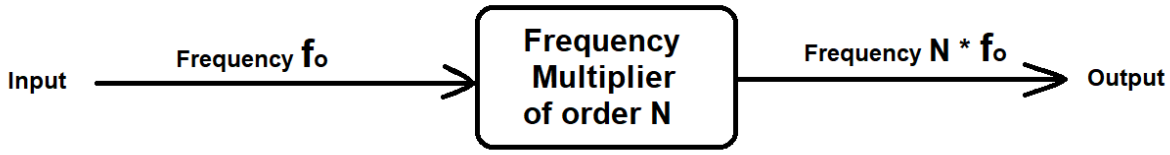

Figure 2. 1 - Frequency Multiplier Functional Diagram

To achieve this operation, the multipliers use the non-linear characteristics of the semiconductors [9]. These non-linear characteristics can be understood by examining the following power series as shown in [9]:

$$I = \alpha_0 + \alpha_1 \cdot V + \alpha_2 \cdot V^2 + \alpha_3 \cdot V^3 + \cdots \quad (2.1)$$

So, if we assume that V is the signal at the input,

$$V = V_1 \cdot cos(\omega_1 \cdot t) \quad (2.2)$$

then the currents resulting from the power series are as follows:

$$i_1(t) = \alpha_1 \cdot V = \alpha_1 \cdot V_1 \cdot cos(\omega_1 \cdot t) \quad (2.3)$$

$$i_2(t) = \alpha_2 \cdot V^2 = \alpha_2 \cdot {V_1}^2 \cdot cos^2(\omega_1 \cdot t) = \frac{1}{2} \cdot \alpha_2 \cdot {V_1}^2 (cos(2 \cdot \omega_1 \cdot t) + 1) \quad (2.4)$$

$$i_3(t) = \alpha_3 \cdot V^3 = \alpha_3 \cdot {V_1}^3 \cdot cos^3(\omega_1 \cdot t) = \alpha_3 \cdot {V_1}^3 (\frac{3}{4}\cos(\omega_1 \cdot t) + \frac{1}{4} cos(3 \cdot \omega_1 \cdot t)) \quad (2.5)$$

As can be seen from the above equations, harmonics start to generate as the power series develops. The role of frequency multipliers is to extract the desired harmonic of the fundamental signal by suppressing all other frequencies.

Frequency multipliers have an input at a low frequency produced by an oscillator and through their non-linear characteristics are capable of producing the frequency N·fo. Ideally, the fundamental frequency is suppressed by the circuit so that only the desired frequency appears at the output. A spectral analysis shows that this is not actually the case, as the unwanted fundamental frequency is not completely cancelled out. One of the goals therefore in the design is to achieve high rejection of the fundamental frequency signal.

In addition, frequency multipliers introduce phase noise into the circuit since they actually multiply the phase of a signal to achieve higher frequencies [10][11]. The more frequency multipliers are placed in series, the higher the phase noise is, as we can see from Table 2.1 below [12].

Input Signal Properties	**Input Function**	**Output Function**
Frequency	*fo*	*N·fo*
Fractional Frequency	$\frac{\Delta f}{f}$	$\frac{\Delta f}{f}$
Phase noise	*L(f)*	*L(f) + 20 · log(N)*

Table 2. 1 - Signal properties of an ideal frequency multiplier with multiplication factor N

With the multiplication factor N, the fractional frequency of the input signal is transferred directly to the output signal. Thus, if in an ideal frequency multiplier we have a signal at the input with a certain precision, the signal at the output will also have this precision. This becomes obvious by looking at the equation:

$$\frac{\Delta f}{f} = \frac{f(t) - fo}{fo} \qquad (2.6)$$

It can be seen that if all frequencies in the right-hand side of the equation are multiplied by the factor N, they are simplified, thus leaving the original expression.

Phase noise, L(f), is a particularly important characteristic for an oscillator. Phase noise is defined as the noise introduced by the rapid, short-term, random phase variation that occurs in a signal. Therefore, it is essentially a measurement of the short-term stability of the signal. Ideal signals have a single spectral power, which corresponds to a perfect sine wave. An ideal signal, therefore, has zero phase noise. Real world signals, however, have phase and fluctuations that cause the spectral power to be distributed over the frequency spectrum. This distributed power is then characterized as phase noise by measuring the power in a 1Hz bandwidth at a specified offset from

the carrier, fm, in units of dBc/Hz [13]. The aforementioned difference in power spectrum between ideal and real signal is shown in Figure 2.2.

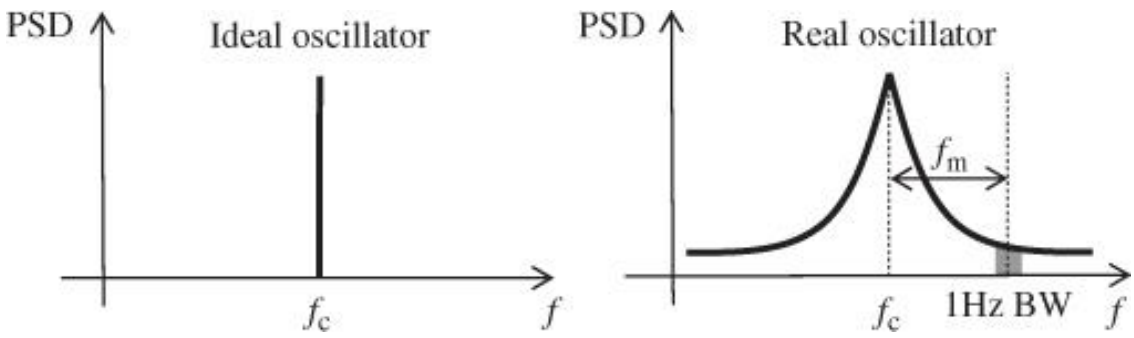

Figure 2. 2 - Power spectrum of ideal and real oscillator

From Table 2.1, frequency multiplication adds phase noise at a rate of 20·log(N). Multiplying the power magnitude is equivalent to adding the logarithmic power, hence the addition shown in the plot is logical. By multiplying the frequency, the power spread of the input signal is further distributed by a factor of N.

Having analyzed the above, maintaining the fractional frequency of the input signal as well as adding phase noise at a rate of 20·log(N) are particularly important points for frequency multiplication when considering the performance of various oscillators. At frequencies below 100MHz, various crystal technologies are available which have orders of magnitude better stability than LC oscillators [14]. The disadvantage of these crystal oscillators is that crystals fabricated with resonances above 100MHz are fragile, difficult to manufacture and very expensive. Therefore, to achieve higher frequencies, in the hundreds of MHz and GHz ranges, LC oscillators and other less stable types of oscillators must be used or large sums must be paid for more complex frequency synthesis methods [15]. Frequency multipliers avoid this disadvantage by allowing the use of a lower frequency, high efficiency reference oscillator, maintaining frequency stability and increasing the phase noise only by a factor of N, instead of whole orders of magnitude. Of course, large multiplier chains can cause small instabilities in the reference frequency of the oscillator to affect system applications, for example in satellite telemetry transmitters [16]. This, however, means that the performance of the reference oscillator must be increased to meet system specifications.

2.2 Passive and Active Frequency Multipliers

There are two main categories of frequency multipliers that can be used, passive and active. Active frequency multipliers use active circuit elements

while passive elements are used in passive multipliers. Of course, there are advantages and disadvantages found in both categories.

2.2.1 Passive Multipliers

Passive multipliers use the non-linear behavior of the passive circuit elements. In this class, diodes, such as Schottky diodes, and non-linear capacitors, such as varactors, are used to achieve frequency multiplication. Passive multipliers are expected to have high order multiplication, low noise and wide bandwidths and are either impedance multipliers or capacitive multipliers [11].

2.2.2 Active Multipliers

Active frequency multipliers have many advantages over passive multipliers. First, they have a very high conversion gain and are therefore more efficient [10]. In addition, they are highly broadband and efficient in DC to RF conversion [10]. The non-linear active elements used are generally FETs and BJTs. Thus, efficient multipliers are realized which dissipate very little heat compared to passive elements.

2.3 S-Parameters

Traditionally, for the description of the linear behavior and the analysis, in general terms, of an n-port at low frequencies, the Z and Y parameters are chosen. Similarly, the analysis of noise in any frequency range is carried out using the H- and G-parameters. However, these aforementioned parameters require open circuit or short circuit measurement conditions, which are difficult to perform accurately at high frequencies. In practice, therefore, at microwave and mm-wave frequencies, the S-parameters, defined as the ratios of incident and reflected power waves, play a primary role because of their ease of extraction and measurement [17].

In further analysis, if we consider the same characteristic impedance Zo in all branches of an n-port, then the equations for the normalized incident and reflected power wave are formulated as follows:

$$a_i = \frac{V_i^+}{\sqrt{Z_o}} \qquad (2.7)$$

$$b_i = \frac{V_i^-}{\sqrt{Z_o}} \tag{2.8}$$

For the relationship between the vectors for incident waves a_i and reflected waves b_i the scattering matrix can be used

$$\begin{bmatrix} b_1 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \times \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} \tag{2.9}$$

where

$$S_{ij} = \frac{b_i}{a_j} \ [a_\kappa = 0 \ \gamma\iota\alpha \ \kappa \neq j \ ] \tag{2.10}$$

in order to fully characterize the behavior of a linear n-port.

The above equation (2.10), suggests that S_{ij}, representing the transmission coefficient from port j to port i, is found by driving port j with the incident wave a_j and measuring the reflected wave b_i from port i, while the incident waves at all ports except j are zero, meaning that these ports are terminated with the characteristic impedance Zo in order to avoid reflections. S_{ii} represents the reflection coefficient at port i when all other ports are terminated at the tailored Zo load. In this way, the S-parameters are satisfied with respect to the reference impedance characteristic Zo.

Specifically for the two-port case, which we are interested in for this work as it can represent our frequency multiplier and an amplifier in general, we have the following:

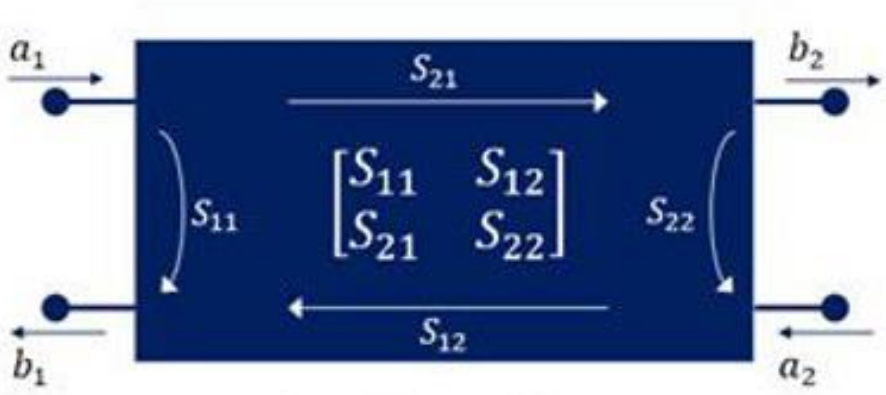

Figure 2. 3 - Amplifier representation as a biplane

$$\begin{bmatrix} b_1 \\ b2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a2 \end{bmatrix} \tag{2.11}$$

From the analysis of the above system, we obtain the following equations:

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (2.12)$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (2.13)$$

Considering an incident wave a_1 at port 1, as shown in Figure 2.3, we will get reflected waves at each of the ports. However, port 2 is terminated with a load equal to the characteristic impedance Zo, thus maximizing the energy transfer to the load and zeroing the reflected wave a_2 at port 2. In this way, the following results are obtained for S-parameters S_{11} and S_{21}, while correspondingly, by terminating port 1 with a load Zo, $a_1 = 0$ and the following results are obtained for S-parameters S_{12} and S_{22}:

- $S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \Rightarrow S_{11} = \frac{\frac{V_1^-}{\sqrt{Z_o}}}{\frac{V_1^+}{\sqrt{Z_o}}}\Big|_{a_2=0} \Rightarrow S_{11} = \frac{V_1^-}{V_1^+}\Big|_{a_2=0}$ *(2.13)*

- $S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} \Rightarrow S_{21} = \frac{\frac{V_2^-}{\sqrt{Z_o}}}{\frac{V_1^+}{\sqrt{Z_o}}}\Big|_{a_2=0} \Rightarrow S_{21} = \frac{V_2^-}{V_1^+}\Big|_{a_2=0}$ *(2.14)*

- $S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} \Rightarrow S_{12} = \frac{\frac{V_1^-}{\sqrt{Z_o}}}{\frac{V_2^+}{\sqrt{Z_o}}}\Big|_{a_1=0} \Rightarrow S_{12} = \frac{V_1^-}{V_2^+}\Big|_{a_1=0}$ *(2.15)*

- $S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0} \Rightarrow S_{22} = \frac{\frac{V_2^-}{\sqrt{Z_o}}}{\frac{V_2^+}{\sqrt{Z_o}}}\Big|_{a_1=0} \Rightarrow S_{22} = \frac{V_2^-}{V_2^+}\Big|_{a_1=0}$ *(2.16)*

Based on the above, we draw some conclusions about the operation of amplifiers, in general, as microwave 2-ports [18]:

- S_{11} Parameter → Reflection coefficient at the input of the 2-port
- S_{12} Parameter → Inverse gain between output and input of the 2-port
- S_{21} Parameter → Power gain of the 2-port

- S_{22} Parameter → Reflection coefficient at the output of the 2-port

In general, S-parameters are complicated numbers and are conveniently expressed in the form of complex numbers with amplitude and phase, as shown below:

$$S_{mn} = |S_{mn}| \cdot e^{j\varphi_{mn}} \quad (2.17)$$

They are usually calculated in decibel(dB) as $20 \cdot log|S_{mn}|$.

2.4 Stability

A central issue in all amplifier and oscillator design problems is the analysis of the stability of the 2-port. In general, if the input or output impedance of the 2-port has a negative real part, it is possible for oscillation to occur. At the same time, the resistances of the 2-port are obtained as a function of the resistances of the signal source and the load, which respectively drive and terminate the network.

Therefore, in order to determine the requirements that satisfy the unconditional stability of the window, we impose the amplitude of the reflection coefficients of both the input and output to be less than 1 for any value of load or source impedance, provided that the effective part of the load and source impedance is positive.

For unconditional stability we therefore have the following:

$$|\Gamma_{in}| = \left|S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - S_{22} \cdot \Gamma_L}\right| < 1 \quad (2.18)$$

$$|\Gamma_{out}| = \left|S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_S}{1 - S_{22} \cdot \Gamma_S}\right| < 1 \quad (2.19)$$

On the contrary, if the above conditions of (2.18) and (2.19) are satisfied for only certain values of the reflection coefficients Γ_S and Γ_L, at a certain operating frequency, we have conditional stability.

In practice, simpler tests can be used to determine unconditional stability. Among them is the K-Δ [19] test, which determines the condition known as Rollet's condition, and is defined as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2 \cdot |S_{12} \cdot S_{21}|} > 1 \quad (2.20)$$

as well as the condition

$$|D| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| < 1 \qquad (2.21)$$

The simultaneous satisfaction of these conditions, which can be easily evaluated, is sufficient and necessary for the unconditional stability of the system. In case the scattering parameters do not satisfy the K-D test, we do not have unconditional stability in the system and a check for its conditional stability must be made through (2.18) and (2.19) as defined above.

2.5 Establishing Gain and Power Criteria

In this section, an analysis of some concepts and criteria describing a multiplier and power amplifiers in general is carried out. In an amplifier circuit, there are many powers entering and exiting it. In the first category belongs the P_{in} input power as well as the DC power of the power supply, which is necessary to polarize the amplifier. On the other hand, at the output, we have the P_{out} power, which is the useful output power, also known as the RF power, and we also have the P_{loss} power, which is the portion consumed due to the passive and parasitic elements, which we try to minimize during the design. The concepts and criteria that will be analyzed therefore, based on the above powers, are as follows:

2.5.1 Conversion gain or power gain

The primary purpose of a frequency multiplier is to produce a harmonic from a signal of a particular frequency. The Conversion Gain, or CG, of a frequency multiplier is a measurement of how strong the desired harmonic output signal is compared to the input signal, whose frequency is being multiplied. Therefore, for a frequency multiplier of order N, the equation describing the conversion gain is:

$$CG = \frac{P_{out}(N \cdot f_o)}{P_{in}(f_o)} \qquad (2.22)$$

while in dB scale it is:

$$CG = P_{out}(N \cdot f_o) - P_{in}(f_o) \quad (2.23)$$

For the special case of N=1, where we do not have multiplication in power but merely amplification of the power of the input signal, the term Power Gain is used.

2.5.2 Bandwidth

In the design process, the Conversion Gain will not only apply to the exact design frequency. The Conversion Gain will remain around its maximum value for a range of frequencies. The bandwidth to be used is therefore defined as the range over which the Conversion Gain is within 3dB of its maximum value.

2.5.3 Suppression of unwanted harmonics

The harmonic selectivity of a frequency multiplier is not inherent in the non-linear device used. At the device level, many harmonics are excited by the input signal. Thus, when designing a frequency multiplier, the suppression of unwanted harmonics is particularly important. An ideal multiplier would have only the desired harmonics at its output, but in the real world, nearby harmonics will always be encountered.

Therefore, harmonic suppression is defined as the ratio of the undesirable harmonic to the desirable harmonic. Thus, for a frequency multiplier of order N, the following equation is used:

$$M^{th} Harmonic\ Suppresion = \frac{P_{out}(M \cdot f_o)}{P_{out}(N \cdot f_o)} \quad (2.24)$$

2.5.4 Efficiency

By efficiency, we define the percentage of the supplied DC power that is converted to the useful RF power at the output. The following relationship follows:

$$\eta = \frac{P_{out}(N \cdot f_o)}{P_{DC}} \cdot 100\% \quad (2.25)$$

2.5.5 Power-Added Efficiency

The efficiency of an amplifier, and therefore of a frequency multiplier as defined above, does not take into account its gain. This can lead to the implementation of circuits which give high performance but which do not take into account the conversion gain. For this purpose, an additional performance measure has been defined, which is the Power-Added Efficiency or PAE. To calculate it, we have the following relationship:

$$PAE = \frac{P_{out}(N \cdot f_o) - P_{in}(f_o)}{P_{DC}} \cdot 100\% \qquad (2.26)$$

and based on the efficiency equation (2.25), it becomes:

$$PAE = \frac{1 - \frac{P_{in}}{P_{out}}}{\frac{P_{DC}}{Pout}} \cdot 100\% = \eta \cdot \left(1 - \frac{1}{CG}\right) \qquad (2.27)$$

At this point, it is worth mentioning that for each amplifier, there is a value of input power, known as the saturation power, which if overtaken, as the input power increases, the gain of the amplifier begins to decrease. Thus, setting the Conversion Gain to tend to -∞ for equation (2.27) we get:

$$\lim_{CG \to -\infty}(PAE) = \lim_{CG \to -\infty}\left[\eta \cdot \left(1 - \frac{1}{CG}\right)\right] = \eta \qquad (2.28)$$

So, we can see that by reducing the conversion gain to -∞, we have an identification of PAE with efficiency.

2.6 Operation Classes of Amplifiers

Considering that an active frequency multiplier is essentially a power amplifier, with different simply harmonics at the input and output, it is

important to understand the classes of operation of power amplifiers and how they can be used for frequency multiplication. The distinction, between the classes of operation, is made on the basis of conduction angle, as shown in Figure 2.4. This section is followed by an analysis of the basic classes of operation of power amplifiers and a reference to other classes of amplifiers.

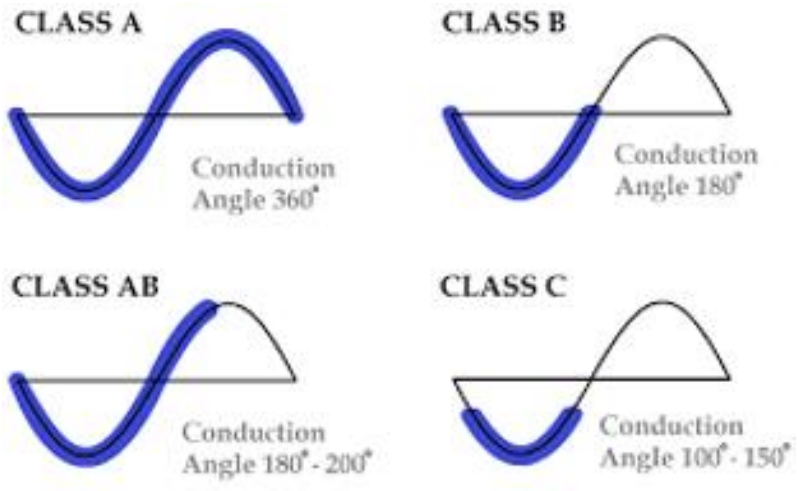

Figure 2. 4 - Classes of Amplifiers and Conductivity Angles

2.6.1 Class A

In conventional power amplifiers and low noise amplifiers, the main advantage of Class A bias is linearity. The Q point on the load line is chosen to give the maximum free space for the output waveform to be linearly amplified from input to output. For the frequency multiplier, therefore, this represents the worst case scenario, i.e. a signal at the input that is carried to the output with minimal additional harmonics.

This, however, does not render Class A useless for implementing a frequency multiplier. If sufficient amplification is performed, the signal at the output can be cut off at its positive and negative peaks. Thus, by examining this clipped output signal based on Fourier analysis, we understand that a symmetrically clipped waveform is rich in odd-order harmonics. As this gain increases and more and more of the signal is truncated, it approximates the shape of a square wave, consisting only of odd-order harmonics. In this approach it is noted that careful biasing must be used to ensure optimal symmetrical clipping, in order to produce odd order harmonics of [6].

For operational Class A, there are also several disadvantages. An important one of them is stability. The device is biased to pass DC current continuously at rest, which means that the small-signal gain is high. So, at RF frequencies, at certain values of impedances, the transistor can be prone to oscillation. Even in the case where this oscillation would be at the output frequency of interest, this can be problematic. Although some designs have successfully used self-oscillation as a reference oscillator [20], the oscillation occurring in the transistor may be less stable than that coming from a reference oscillator. Thus, a frequency multiplier will add significant phase noise. Class A design often warrants stabilization networks, which adds complexity and can cause losses in the system.

With constant DC current, there is also a loss of efficiency. Ideally, the maximum efficiency of a Class A amplifier is 25%, a value that is the lowest of all amplifier classes.

2.6.2 Class AB/B

Classes AB and B are both classes of operation with reduced conduction angle. Class AB operates the transistor at a conduction angle between 180 and 360 degrees, while Class B has a conduction angle of 180 degrees, acting as a half-wave amplifying rectifier. Class AB faces similar stability issues to Class A as the Q point has DC current flowing continuously through the device. Class B is polarized to have a Q point with a DC current of nearly 0. However, such a small signal gain is discouraged, and circuit stability is less of a problem.

In the application of frequency multipliers, Class AB has been used to generate a frequency comb similar to that of SRD [21]. Class B provides an output waveform that is rich in second and low in third harmonic component. This bias point, can then be well used in doubling applications where high third harmonic suppression is crucial [22].

2.6.3 Class C

Further reduction of the conduction angle below 180 degrees produces the operational Class C. In this Class, the transistor amplifies only a portion, less than half, of the input signal. As with Class B, Class C amplifiers are much less prone to oscillation, due to the fact that they have no DC quiescent current and therefore the small signal gain is small. In addition, Class C is the most efficient reported so far, with a possible efficiency in the range of 70%.

Class C amplifiers work very well when it comes to harmonic frequency generation. The reduced conduction angle output signal is rich in higher harmonics. This is evident from Figure 2.5, which represents the amplitude of the harmonic components in the collector current as the conduction angle decreases.

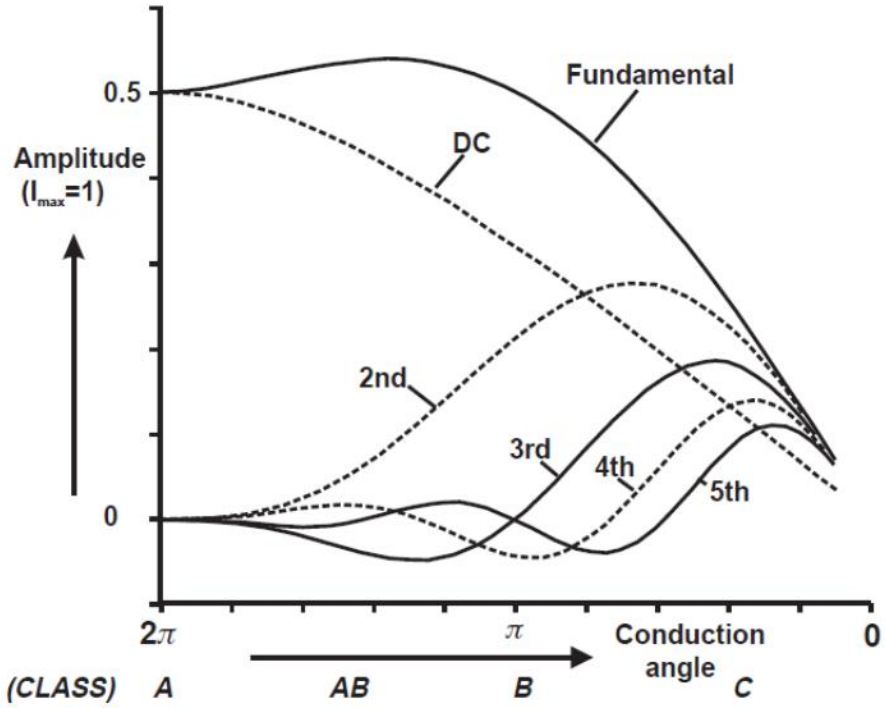

Figure 2. 5 - Collector current of harmonics as a function of decreasing conduction angle

The references in the previous sub-sections, regarding other Classes, can also be verified from Figure 2.5. The output signals of the ideal Class A consist entirely of the DC and fundamental components. Class B offers a point of increased second harmonics and minimum third harmonics. Class C, however, contains the full range of conduction angles including the peaks for the harmonics. Thus, a Class C amplifier ends up being the most flexible of all classes of amplifiers for harmonic generation, as a simple change in circuit polarization allows the higher harmonics to be excited and output successfully. To this end, the Class C amplifier plays a vital role in the design of the frequency multiplier in this paper.

2.6.4 Other Classes

The analyses in the aforementioned sub-sections treat the transistor, in a power amplifier, as a current source, with the only parameter that changes being the polarization. With some other classes of operation that follow, more variables are introduced.

With the basic Class E amplifier, the transistor is treated as a switch, in a pseudo-class C biasing scheme. The transistor then has two states. Those of on and off. Thus, the current and voltage waveforms have minimal crossover, which means minimal power dissipation. The performance is then limited only by the switching time for the transistor [23]. This leads to the addition of harmonic source and load terminations to result in faster switching time and a more square waveform, as in Class F amplifiers [24]. In these frequency multiplier topologies, the square current waveform is of interest. As discussed in the Class A section, square waves are inherently rich in odd harmonics. However, with Class E, the stability and efficiency issues of Class A do not exist. Additionally, Class E, by adjusting the conduction angle of Class C, offers the ability to adjust the output duty cycle of the square wave. Although this may require complexity in the load network, it allows higher harmonics to be excited with lower duty cycles [25].

Subsequently, Class J returns to using the transistor as a current source, pushing the device into Class AB or Class C. Similar harmonic termination methods are used in Class J as in Classes E and F. In Class J, the design focuses primarily on resonating the second and higher harmonics at the output. The higher harmonics are used to enhance the fundamental and the phase shifting in the output voltage waveform, with specific harmonic termination impedances, helps to increase efficiency by minimizing the crossover of the current and voltage waveforms [26][27][28].

Chapter 3 - Design of the Frequency Multiplier of order N = 3

In this chapter, the whole design process of the frequency multiplier, of class 3, with a central output signal frequency of 145GHz is described in detail. The design of the multiplier was carried out through the environment of Virtuoso of Cadence and Advanced Design System (ADS) of Keysight. The fabrication technology is Infineon Technologies' B11HFC. Below, the performance objectives for the IC, the technology characteristics, and the design flow throughout the frequency multiplier synthesis process will be listed.

3.1 Performance objectives and design flow

In order to define the specifications for the multiplier in this paper, a review of the characteristics in similarly fabricated integrated circuits was carried out [32][33][34][35][36][37][38][39][40][41][42][43][44][45][47][48]. A summary of some of the performance is presented in Table 3.1 below:

No	**Ref.**	**Process**	**Out Freq.** (GHz)	**Out Power** (dBm)	**Conv. Gain** (dB)	**×N**	**P_{DC}** (mW)
1.	(2)	0.1μm InP HEMT	158-172	5.0	-2.0	**×2**	95.2
2.	(3)	50nm mHEMT	150-220	4.8	-7.2	**×2**	25
3.	(4)	100nm mHEMT	110-130	5.0	3.0	**×2**	62.5
4.	(5)	0.13μm SiGe HBT	215-240	-3.0	-3.0	**×2**	630
5.	(6)	90nm CMOS	91-97	-12.5	-18.5	**×3**	5.5
6.	(7)	2μm InP DHBT	0-100	-11.0	1.0	**×2**	730
7.	(10)	50nm mHEMT	140	-1.5	-11.0	**×3**	40
8.	(tripler paper)	250nm InP DHBT	119-135	10.0	7.0	**×3**	45

9.	(1)	0.15μm GaAs mHEMT	72-114	-5.0	-19.5	×6	125
10.	(2)	0.1μm GaAs mHEMT	77-105	7.0	7.0	×6	470
11.	(3)	0.25μm InP DHBT	155-195	0.0	-6.5	×6	92.5
12.	(4)	0.13μm SiGe HBT	110-125	-3.5	-10.5	×6	20
13.	(5)	0.13μm SiGe HBT	231.5-248.5	-4.0	-4.0	×6	900
14.	(7)	0.13μm SiGe HBT	121-137	-2.4	0.6	×4	35.2
15.	(8)	0.13μm SiGe HBT	129-171	2.2	5.0	×4	100
16.	(chalmers paper)	0.13μm SiGe HBT	109.5-146.5	4.5	0.2	×6	310

Table 3. 1 - Characteristics of implemented frequency multipliers

In particular, we focus more on lines number 12 and 14 to 16 where the implementation technology is SiGe and the operating frequency range is close to the range of interest for this work.

Therefore, based on the above, we establish the following performance objectives for our frequency multiplier:

- Central Frequency = 145GHz
- Bandwidth of Operation → 130-160GHz
- Output Power > 0dBm
- Conversion Gain > 0dB
- Power dissipation < 400mW

When designing the integrated circuit, the flow includes the following points:

1. Defining objectives and specifications for the circuit.
2. Study of the topology and role of each transistor, that make up the active devices of the IC, along with their selection.
3. Study of biasing and power supply for each individual stage.

4. Design of output, intermediate and input networks with ideal passive components.
5. Replacement of each network with components of B11HFC technology.
6. Extraction of parasitic elements (QRC extraction).
7. Layout design based on circuit schematic.
8. Electromagnetic simulations of individual networks as well as matching them with the networks of B11HFC components.
9. Update of overall layout.
10. DRC (Design Rule Check) and LVE (Layout Versus Schematic) checks.
11. Further simulations to characterize the performance and proper operation of the frequency multiplier.

3.2 Features of B11HFC technology

In this section, the technology used to implement the circuit of this work will be discussed, which is the B11HFC provided by Infineon Technologies. This technology, B11HFC, is a 400GHz/130nm SiGe BiCMOS technology with copper metallization for analog as well as mixed signal mmWave applications, which has high performance while achieving low power consumption [29]. This technology offers a layer stack with 6 levels of copper metallization and 1.0µm aluminum as the last metal.

The B11HFC technology finds scope for use in applications such as Automotive Radar MMICs, RF ASICs as well as applications for high-speed wireless data links. Briefly, the technology includes three types of NPN HBT devices in various sizes and contact multiplicities, metal film resistors, MIM capacitors, various types of varactors, PIN diodes and also various types of RF transmission lines [30].

3.2.1 High Speed NPN device

Infineon Technologies AG's B11HFC technology provides a variety of SiGe npn heterojunction bipolar transistors, which are high-speed npn, medium-speed npn and high-voltage npn. As the name suggests, the high-speed npn can reach much higher frequencies than the other two types. For example, the fT passband frequency for high-speed npn is twice or more that of the others.

For this thesis, it is of paramount importance to achieve the highest possible frequencies to achieve the 6G standard, therefore only high-speed npn transistors were used.

The HBTs have two dimensions, the emitter length, which ranges from 0.7 µm to 10 µm, and the emitter width, which ranges from 0.22 µm to 0.34 µm. To

find the actual dimensions, the actual Aeff surface area, we subtract the mask surface area which adds 0.09 μm in both length and width.

In order to extract some basic characteristics of the high-speed npn transistor of this technology, the following schematic diagram, Figure 3.1, was used.

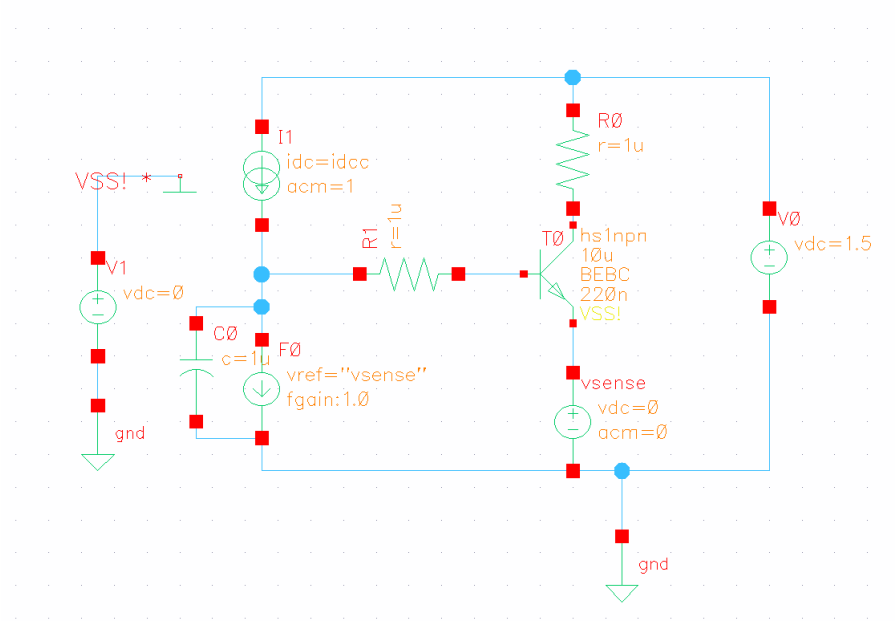

Figure 3. 1 - Cadence schematic diagram designed for high speed HBT characterization

For proper design it is advisable to have an estimate of the current density for the optimal speed of the device. Figure 3.2 shows that, the highest unit frequency gain (passband frequency) fT~280 GHz is achieved when the transistor collector is traversed by a current density of about 14 mA/μm2. It should be noted that transistor models are updated frequently and, therefore, it is possible that there may be discrepancies from time to time.

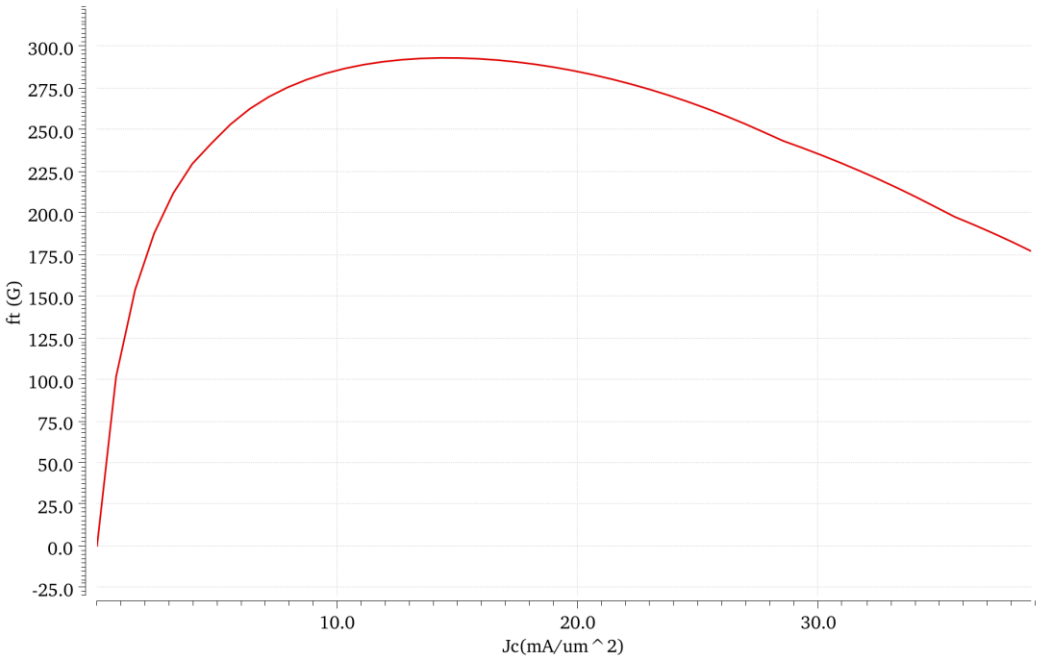

Figure 3. 2 - Plot of FT frequency versus collector current for a 0.22 x 10um^2 high-speed HBT

Also, for illustrative purposes, Figure 3.3 of the beta gain (b) versus frequency was extracted.

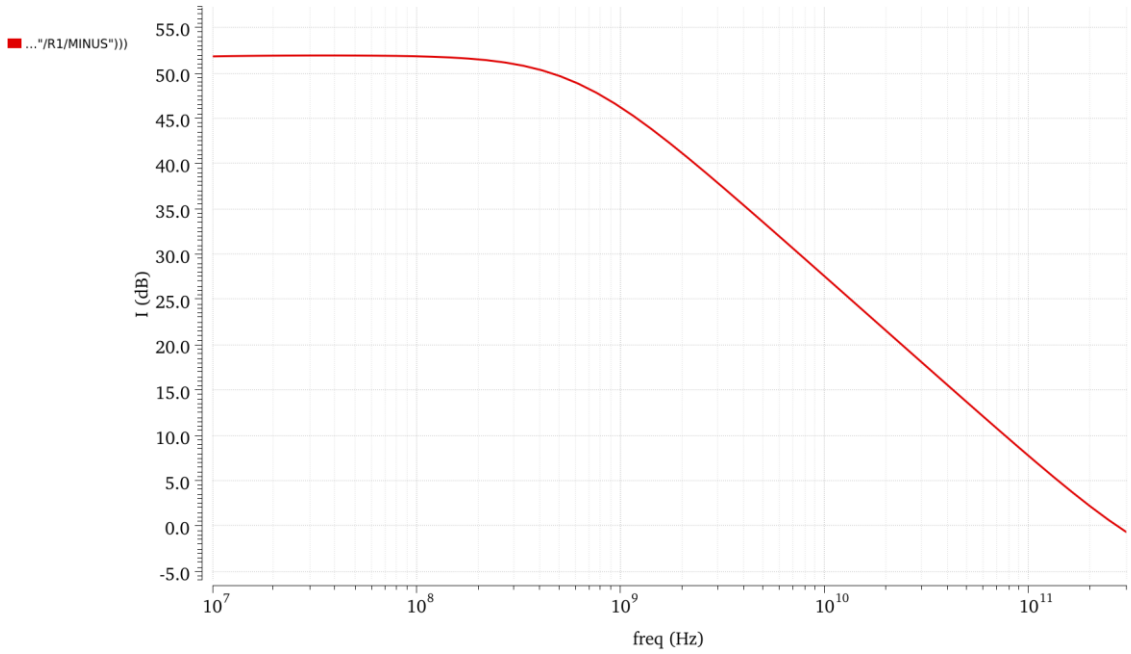

Figure 3. 3 - Beta gain versus frequency plot for a high speed HBT of 0.22 x 10um^2 area.

In general, the equation relating the current density to the current in the HBT collector uses the effective surface area Aeff as shown below:

$$J_C = \frac{I_C}{A_{eff}}$$

3.2.2 MIM Capacitors

We randomly select a 100fF MIM capacitor from the library of and examine it for the dependence of its capacitance C and its quality factor Q versus frequency f. Figure 3.4 illustrates the Capacitance versus frequency plot, from which we can conclude that the capacitance of the MIM capacitor is inversely proportional to the frequency.

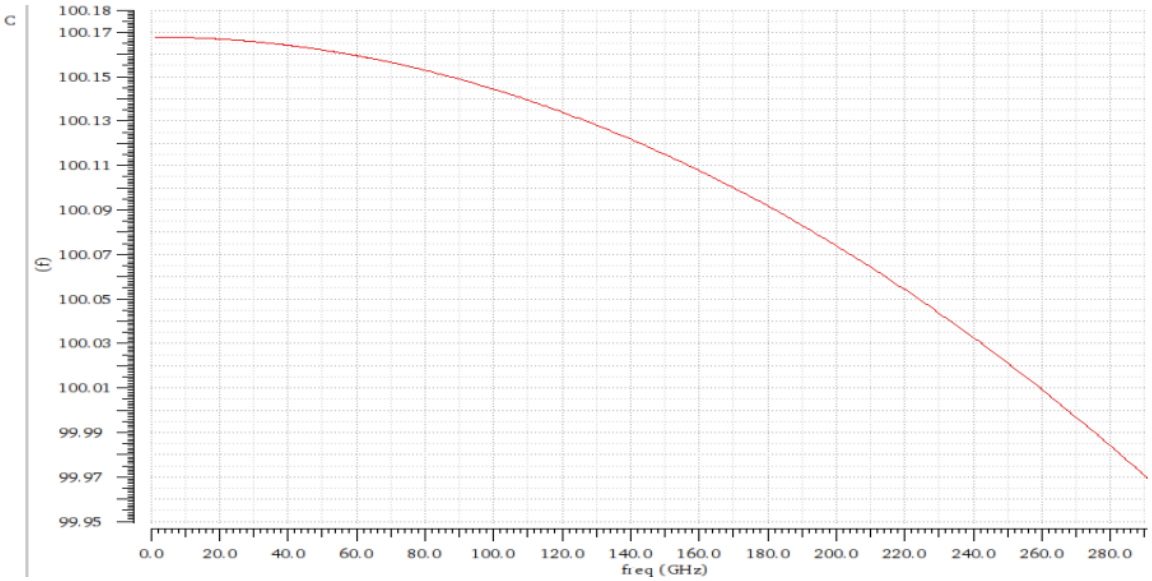

Figure 3. 4 - Capacitance versus frequency of a MIM capacitor 100fF

Figure 3.5 shows the Quality factor versus frequency plot, from which we can conclude that the quality factor of the MIM capacitor is inversely proportional to the frequency.

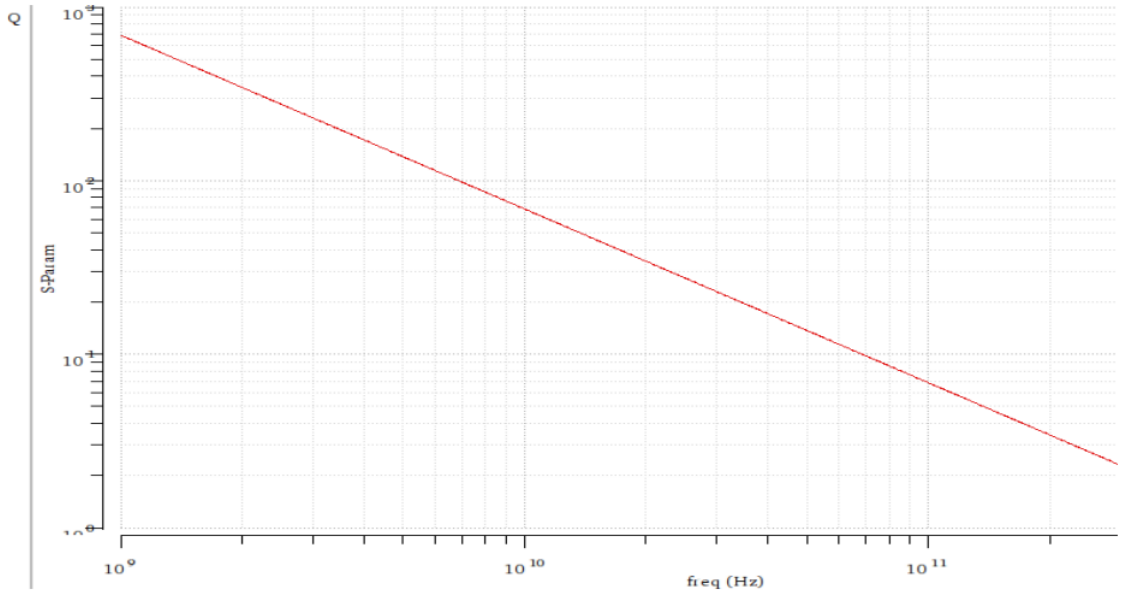

Figure 3. 5 - Quality factor versus frequency of a MIM capacitor 100fF

3.2.3 TaN Resistors

As shown in Figures 3.6 and 3.7, the TaN resistance models, like the MIM capacitor models, exhibit a frequency dependence. Their value versus frequency appears to change as if some parasitic capacitance is connected in parallel to the resistor. Furthermore, the performance of the resistors seems to depend on their dimensions, as resistors of larger dimensions seem to have a larger parasitic capacitance. Figure 3.6 shows the plot of the real part of a 200 Ω TaN resistor TaN versus frequency and Figure 3.7 shows the corresponding plot for the imaginary part of the resistor.

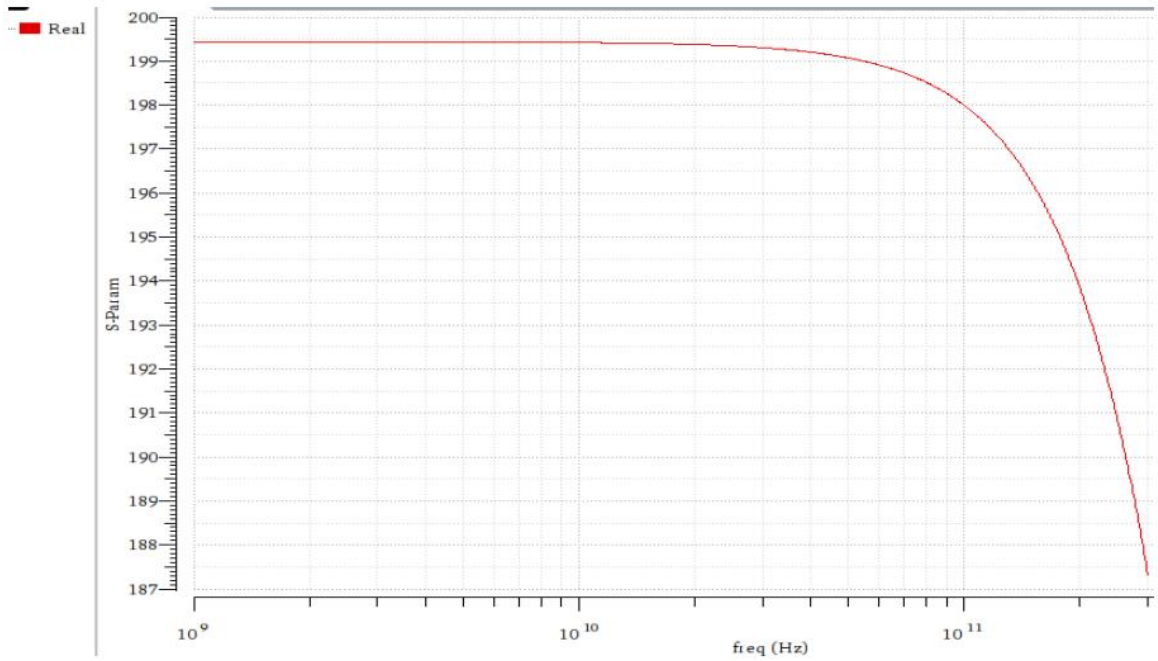

Figure 3. 6 - Real part of a TaN resistor 200Ω versus frequency plot

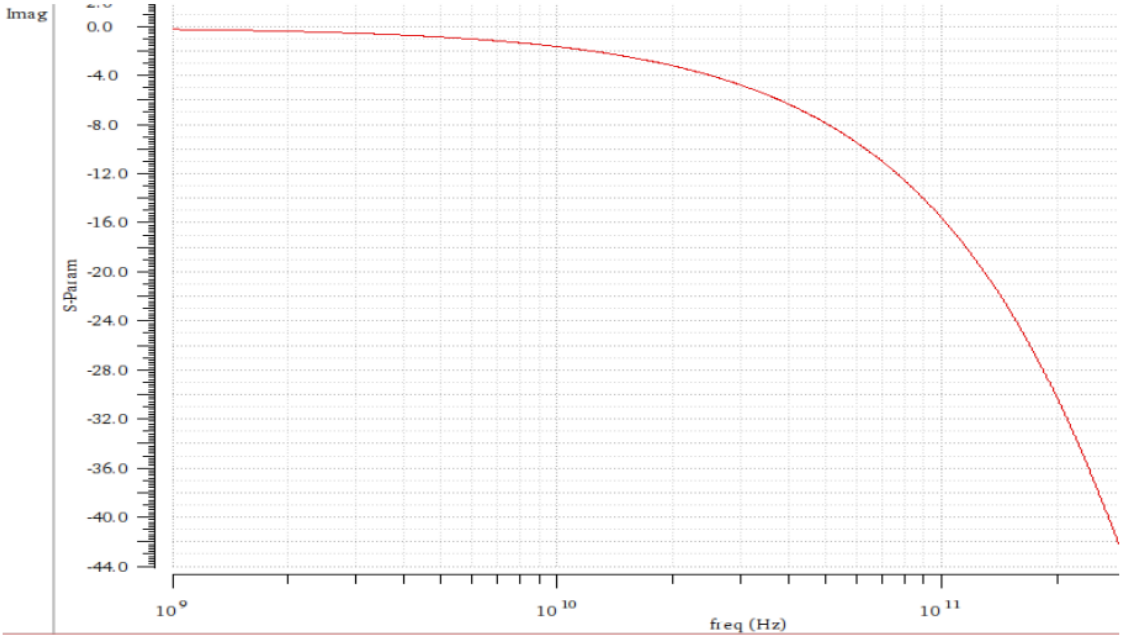

Figure 3. 7 - Imaginary part of a TaN resistor 200Ω versus frequency plot.

3.3 The Frequency Multiplier from a macroscopic point of view and the General Topology

The main idea for the design of the frequency multiplier in this work is shown in Figure 3.8 below:

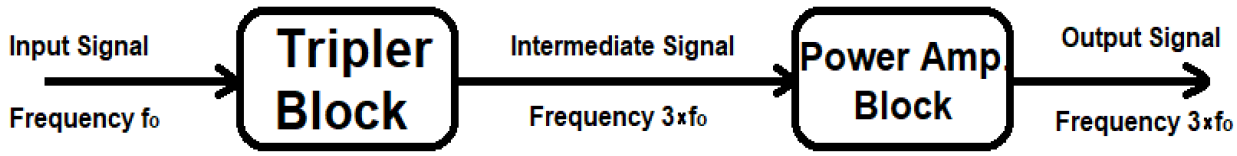

Figure 3. 8 - Diagram of the signal flow in the frequency multiplier

So, as it can be observed, initially, the circuit receives at the input a signal at a fundamental frequency fo. At this point, a block is inserted which aims to excite the third harmonic component of the signal (Tripler Block), taking advantage of the non-linear behavior of its active devices. Subsequently, this third harmonic is transmitted to the next block, while further suppressing the remaining harmonics. This block receiving the third harmonic component is essentially a Power Amplifier Block, which is centered at the operating frequency of the third harmonic, i.e. three times the frequency

of the signal received by the circuit at the input. Finally, this amplified third harmonic, of frequency 3×fo, is transmitted to the output of the circuit.

3.3.1 Differential Input - Differential Output

In the process of studying the topology to be used for the circuit, the design of a differential input and differential output multiplier was initially chosen. Based on what was previously mentioned, the desired harmonic sought to be excited, and then amplified by the power amplifier block, is the third harmonic. The decision for the differential input and output therefore arises due to the rejection of the even harmonics of the fundamental signal being achieved. In detail, we have the following analysis:

As we know, the signal at the output of an amplifier can be written as:

$$V_o = \alpha_0 + \alpha_1 \cdot V_i + \alpha_2 \cdot {V_i}^2 + \alpha_3 \cdot {V_i}^3 + \cdots \quad (3.1)$$

Moreover, for the differential output therefore of an amplifier we have that:

$$V_{o,diff} = {V_o}^+ - {V_o}^- \quad (3.2)$$

while at the same time,

$${V_o}^+ = \alpha_0 + \alpha_1 \cdot V_i + \alpha_2 \cdot {V_i}^2 + \alpha_3 \cdot {V_i}^3 + \cdots \quad (3.3)$$

and

$${V_o}^- = \alpha_0 + \alpha_1 \cdot (-V_i) + \alpha_2 \cdot (-V_i)^2 + \alpha_3 \cdot (-V_i)^3 + \cdots \Leftrightarrow$$
$${V_o}^- = \alpha_0 - \alpha_1 \cdot V_i + \alpha_2 \cdot {V_i}^2 - \alpha_3 \cdot {V_i}^3 + \cdots \quad (3.4)$$

Thus, substituting the representations of equations (3.3) and (3.4) into equation (3.2), we obtain the following:

$$V_{o,diff} = 2\alpha_1 \cdot V_i + 2\alpha_3 \cdot {V_i}^3 + 2\alpha_5 \cdot {V_i}^5 + \cdots \Leftrightarrow$$
$$V_{o,diff} = \alpha_1' \cdot V_i + \alpha_3' \cdot {V_i}^3 + \alpha_5' \cdot {V_i}^5 + \cdots \quad (3.5)$$

from which it is obvious that the even harmonics are not included in the final signal at the reaching output.

3.3.2 Tripler Block

The initial block of the multiplier, which is the tripler block, is the one responsible for generating the third harmonic component of the input signal. As shown in Figure 3.9, it consists of two stages of active devices.

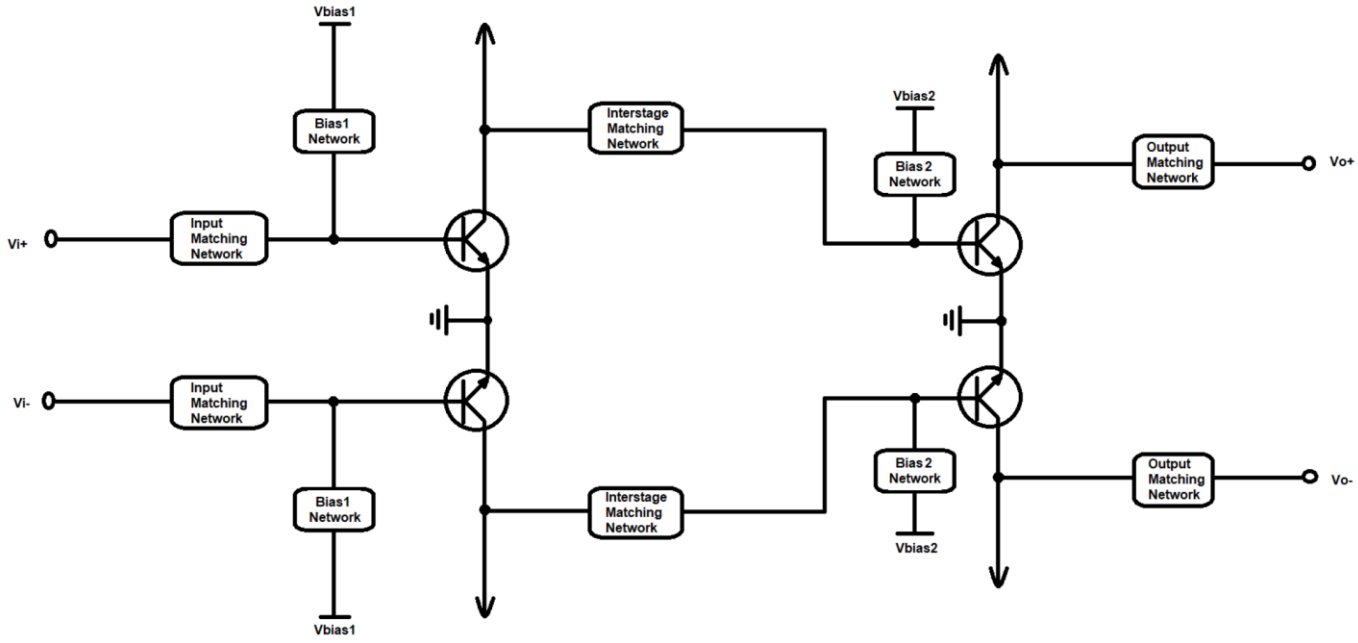

Figure 3. 9 Schematic representation of the Tripler Block

The first stage is an amplifying stage of the input signal. For this reason, the HBTs in this stage will be biased, with Vbias1, as Class A amplifiers, as discussed in Chapter 2, in order to produce at their output a stronger signal that will be the input to the second stage.

Subsequently, we want the second stage to produce the highest harmonics of the signal at its input. This leads to the conclusion that this stage acts as a Class C amplifier and is therefore biased accordingly, with the value of Vbias2. Of course, both at the input, the output and between the stages, matching networks are used, at the desired frequency each time, to achieve the conjugate matching of the impedances seen by the transistors at their base and collector respectively.

3.3.3 Power Amplifier Block

The aforementioned Tripler Block is followed by the Power Amplifier Block, PA Block, which takes care of amplifying the generated third harmonic signal, which is the signal at the output

frequency. Figure 3.10 below shows the general topology of the power amplifier, which consists of three stages.

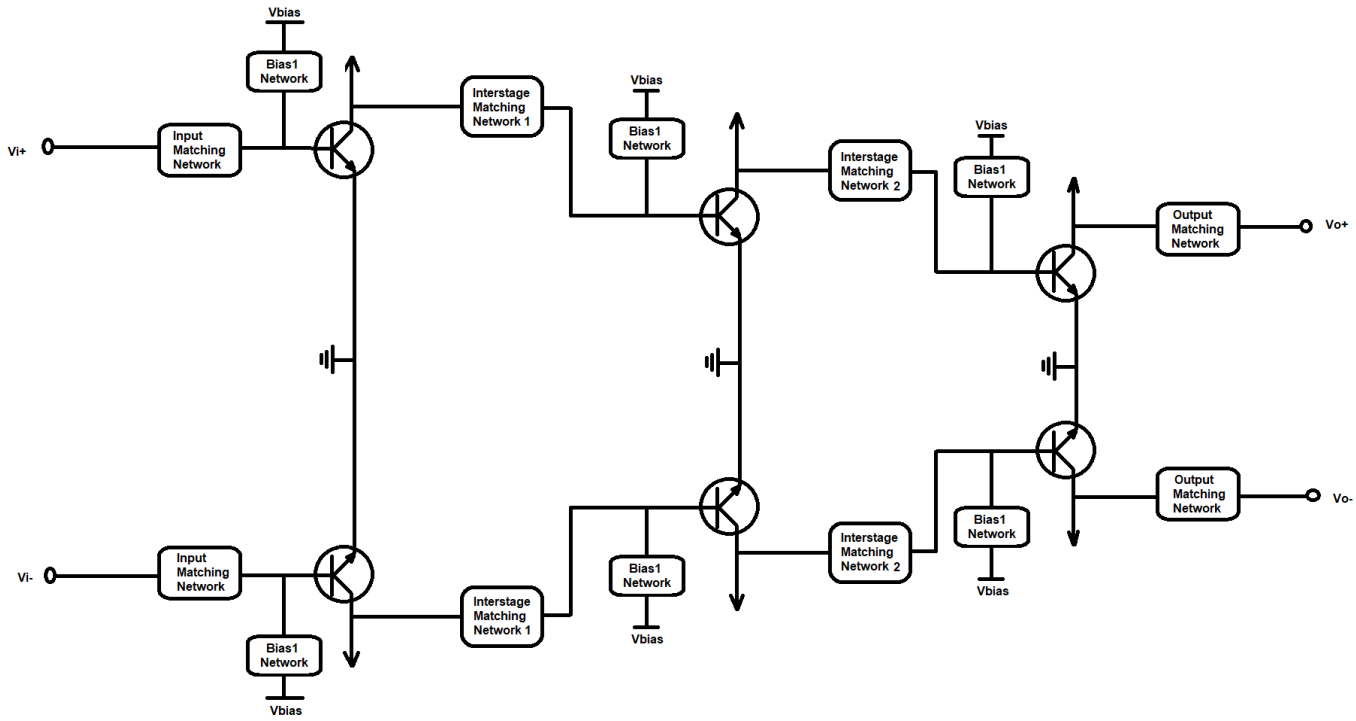

Figure 3. 10 Schematic representation of the Power Amplifier Block

The stages of the power amplifier are all three Class A amplifier stages, biased by the Vbias value, as they receive at their input a signal whose amplification, at its fundamental frequency, is sought.

At the input and output of each of the first two stages, conjugate matching of the impedances seen by the transistors is performed. The distinction noted in the last stage of the power amplifier is that the matching performed is based on the Load-Pull technique, as discussed subsequently in the following section, in order to maximize the power of the signal at the output.

Having therefore, connected in series, the two blocks mentioned above, which make up the overall frequency multiplier, the topology of the overall circuit is produced, as shown in Figure 3.11. To achieve this connection, the output and input matching networks of the Tripler and Power Amplifier Block are removed, respectively, and their place is taken by a network designed for the conjugate matching of their impedances.

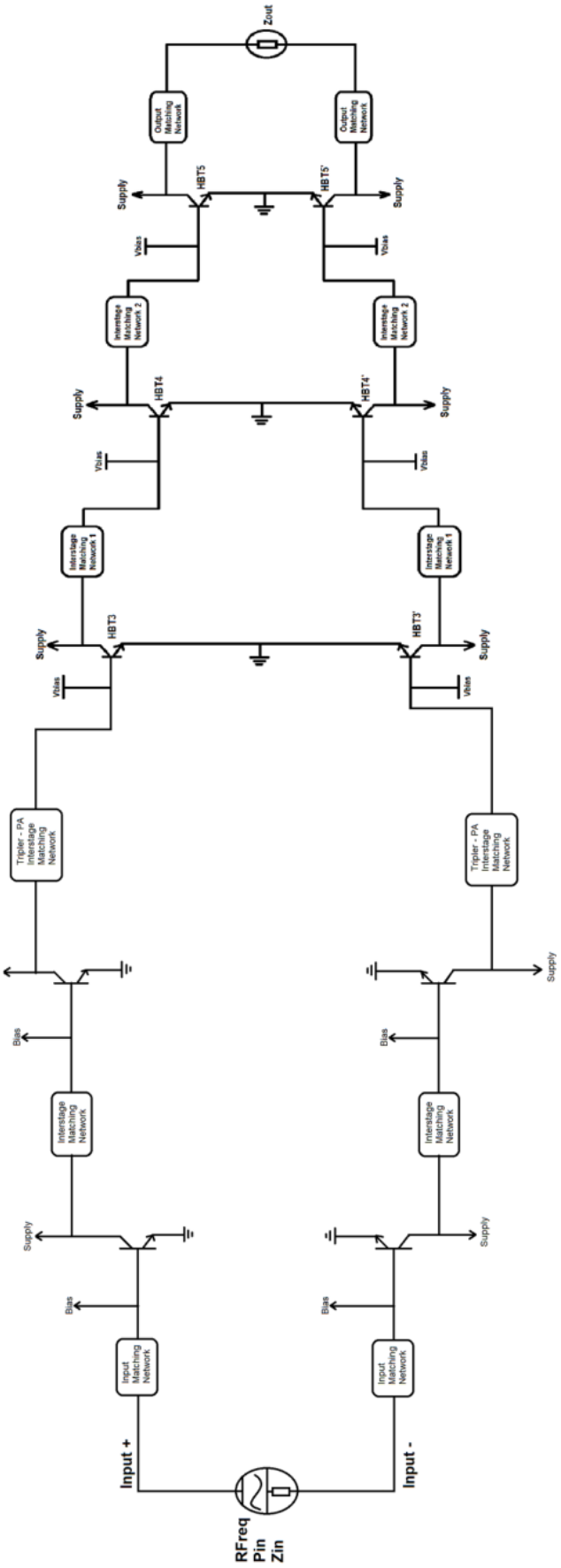

Figure 3. 11 - Topology of the Frequency Multiplier

3.4 Simulation Setup and Definition of Equations

As mentioned in the introduction of the chapter, the design of the multiplier was done through Virtuoso as well as ADS. The use of the ADS tool during the design required the use of the dynamic link feature between the two programs, in order to pass the B11HFC technology models from the Virtuoso libraries to those of ADS. The components for which this process was done are the high speed npn HBTs, the MIM capacitors, the tlines, and the TaN Resistors. As an example, the process for a high speed HBT is given. As shown first in Figure 3.12, a schematic is created in Virtuoso, in which the element we want to pass to ADS is placed. With the value "em_length" we set the length of the emitter as a parameter so that we can change its value and from the ADS afterwards.

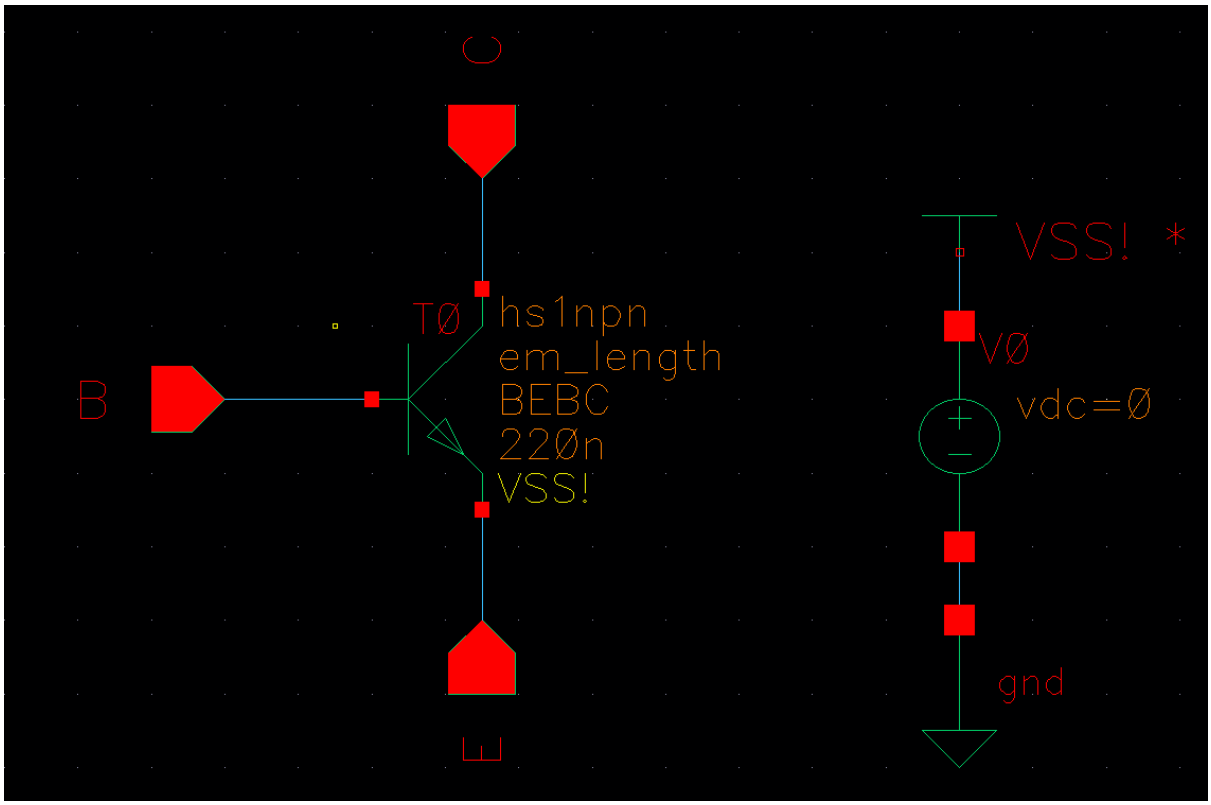

Figure 3. 12 –Virtuoso schematic of a High Speed HBT

Then, as we can see from Figure 3.13, we create a symbol for our element, which we will enter into ADS when we want to use it during the circuit design.

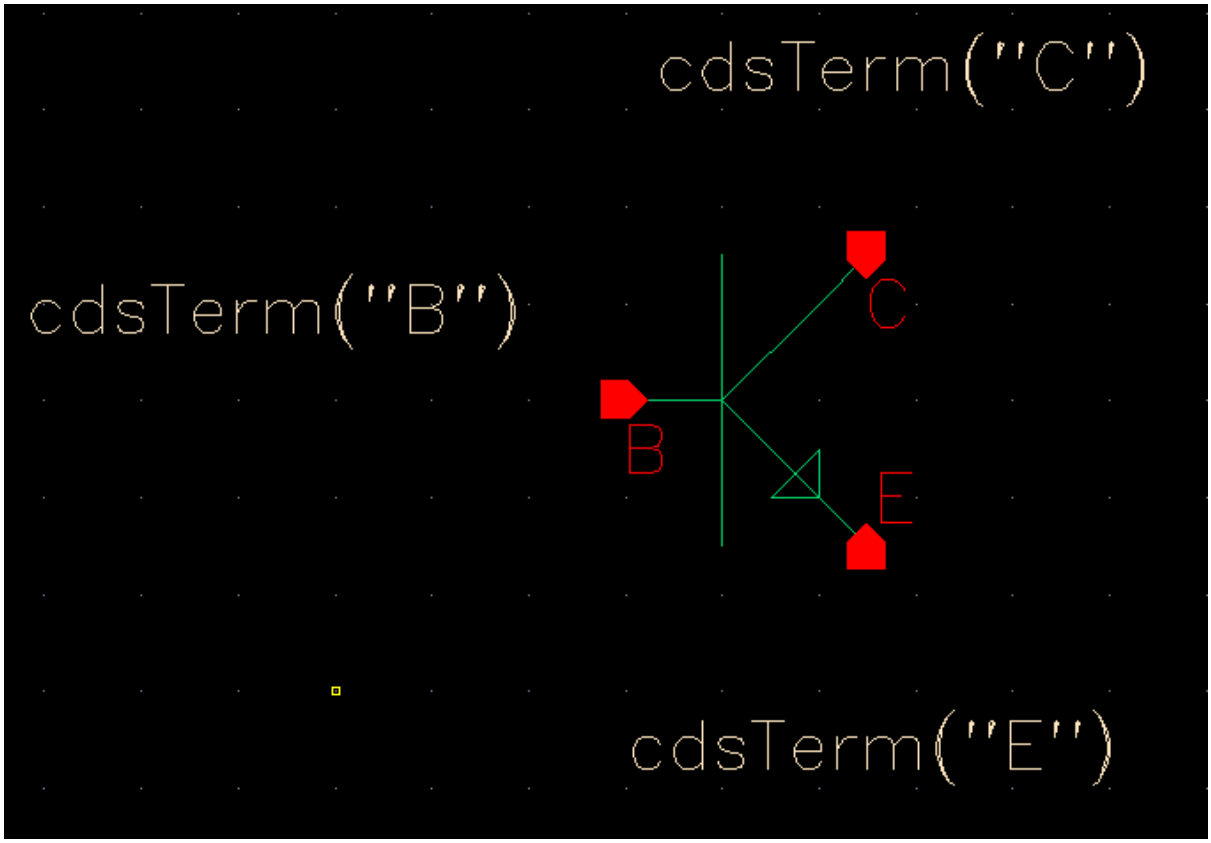

Figure 3. 13 - High Speed HBT symbol in Virtuoso

Having created the desired symbols for our components, we open the ADS program by dynamically linking the two, as shown in Figure 3.14.

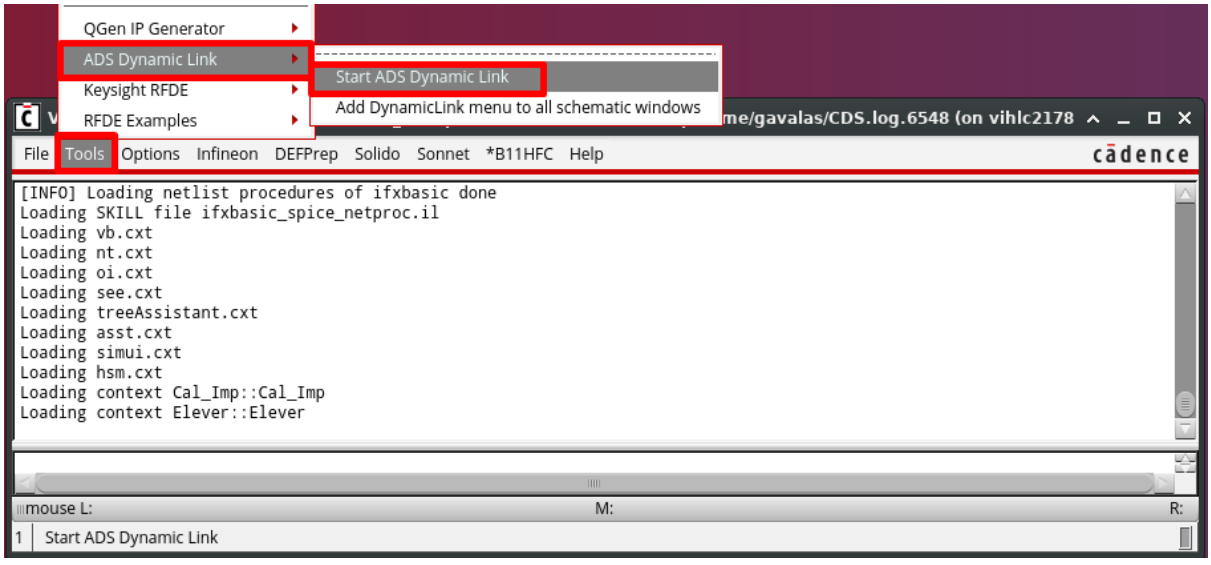

Figure 3. 14 - Open ADS via Dynamic Link

Finally, after opening ADS, we create a schematic, and navigate to DynamicLink → Instance → Add Instance of Cellview, as shown in Figure 3.15.

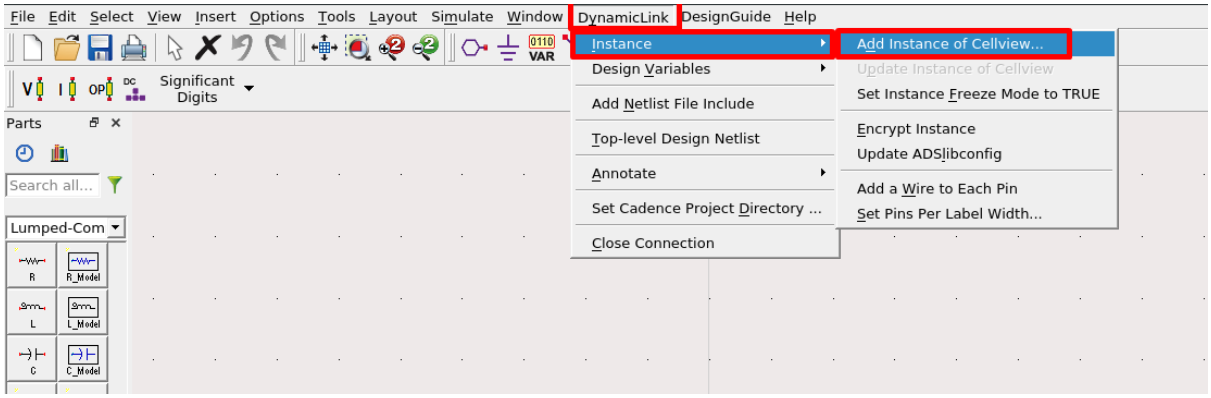

Figure 3. 15 - Import element with Dynamic Link in ADS

Throughout the design of the individual, aforementioned parts, which make up the frequency multiplier, various simulations are used to check the results, in order to have an overall overview of the design process. Some of them, which were extensively used, are the S-Parameters simulation, the Harmonic Balance simulation as well as the Transient simulation. These, as shown in Figure 3.16 below, are deposited on the circuit schematic, with a gear symbol. In particular, the S-Parameter Simulation, from 1GHz to 300GHz with a step of 0.1GHz, the Harmonic Balance Simulation, for the RFfreq parametric frequency, up to the 7th order, and finally the Transient Simulation up to 1 nanosecond with a maximum step of 0.01 nanosecond are shown.

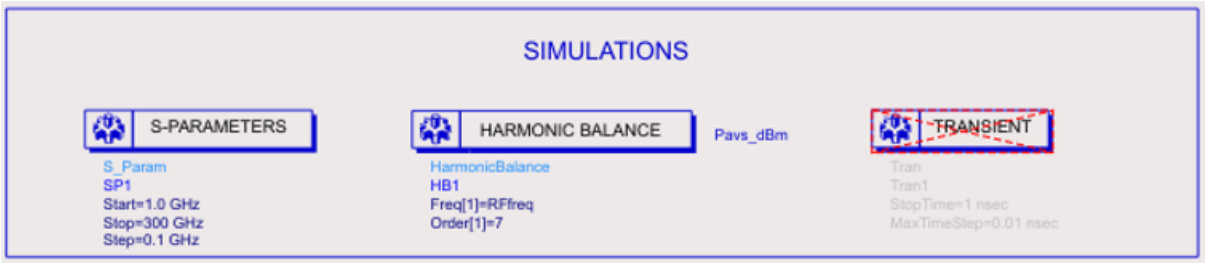

Figure 3. 16 - Defined simulations

In addition to the simulations available from the Advanced Design System (ADS) design program, some equations are used to determine the input and output power of the various harmonics, the Conversion Gain (CG), Power Consumption, Power Analysis Efficiency (PAE) and others. These equations, are presented in Figure 3.17 below:

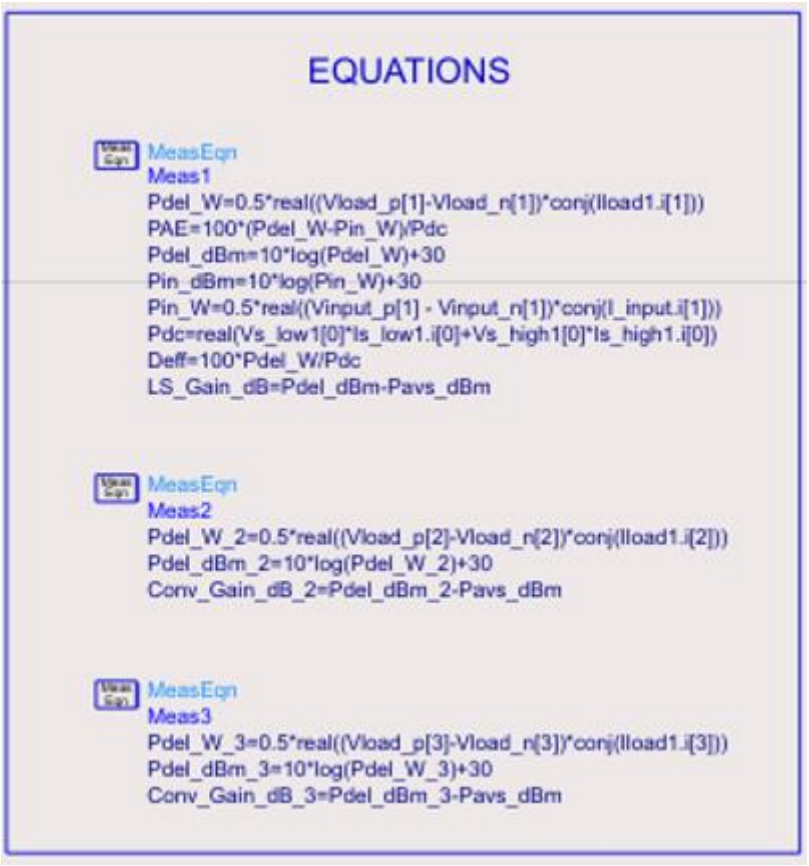

Figure 3. 17 - Defined equations

3.5 Definition of parameters and selection of HBTs

The active device of our frequency multiplier is the device that will generate the required power to the output load. As we know from theory, this device not only produces power, but also consumes power due to the non-idealities that describe it. Our goal is to reduce these effects and select an active device that meets our requirements at all levels.

The critical point in selecting an active device that fits the power and performance requirements of the application at hand is to study and compare the transistor models available from the technology and then select the appropriate area and the voltage at which they are polarized [31]. The transistors available from the technology, as derived from the B11HFC technology manual, were presented in Section 3.2, followed by the method followed to select the most suitable area and polarization voltage for each stage of the individual parts of the overall multiplier.

Therefore, to select the aforementioned parameters, a differential topology is used with DC_Block and DC_Feed at the input and output respectively. The requested quantities of the emitter length as well as the bias voltage are set as parameters, the value of which is varied. So by taking the graphs with the power results for each case and controlling the current in the

collector of the transistor, we arrive at the task at hand which is the selection of the most suitable parameters for our active device. Below, Figure 3.18 shows the topology used to select each active device.

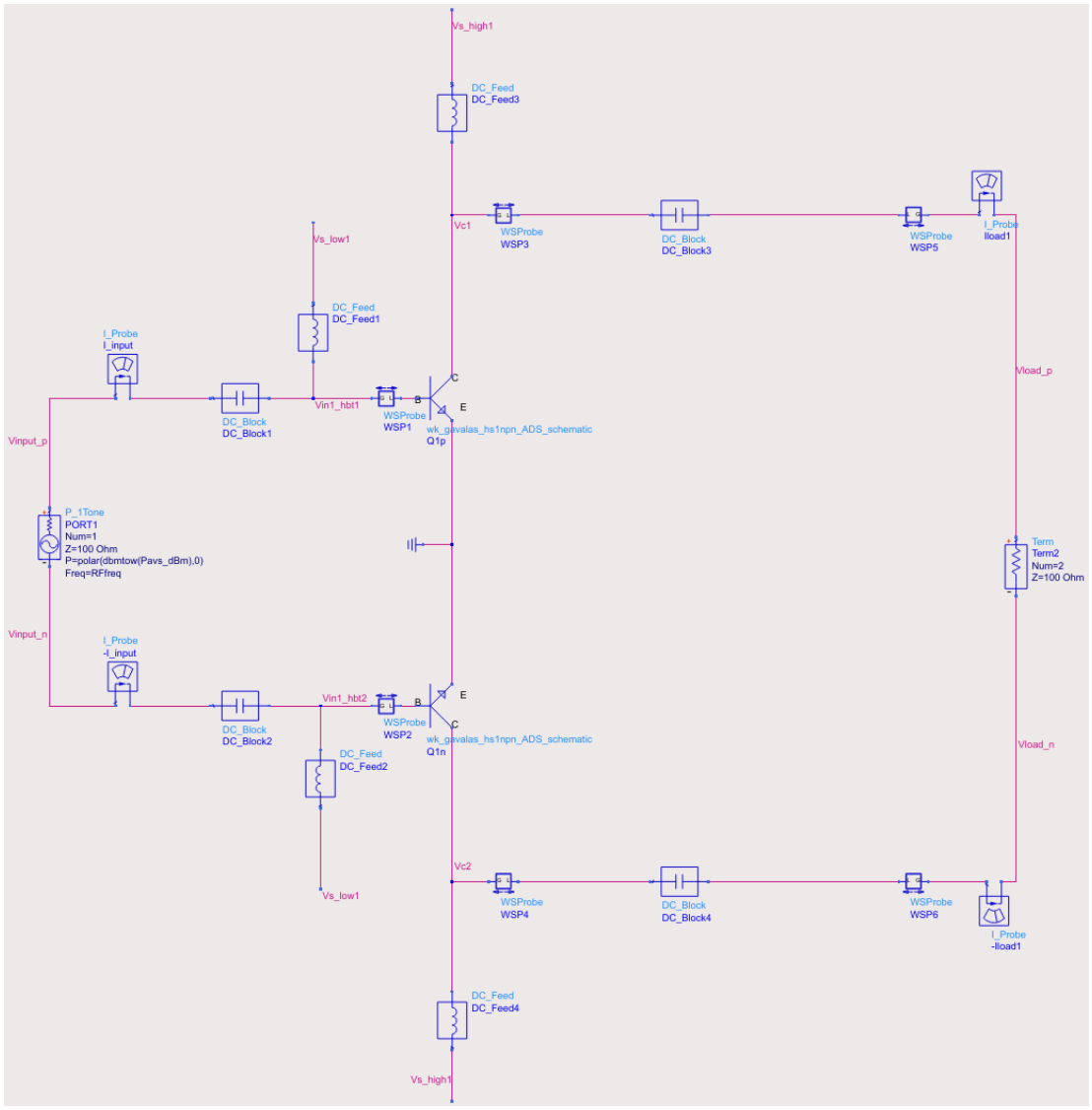

Figure 3. 18 - Topology of HBT feature selection

3.5.1 1st Stage – Tripler Block

As discussed in subsection 3.3.2, the first stage of the Tripler Block, aims to amplify the input signal, namely the 1st harmonic, hence it is to be biased as a Class A amplifier. A first approximation of the scan of the parameter values is shown in Figure 3.19.

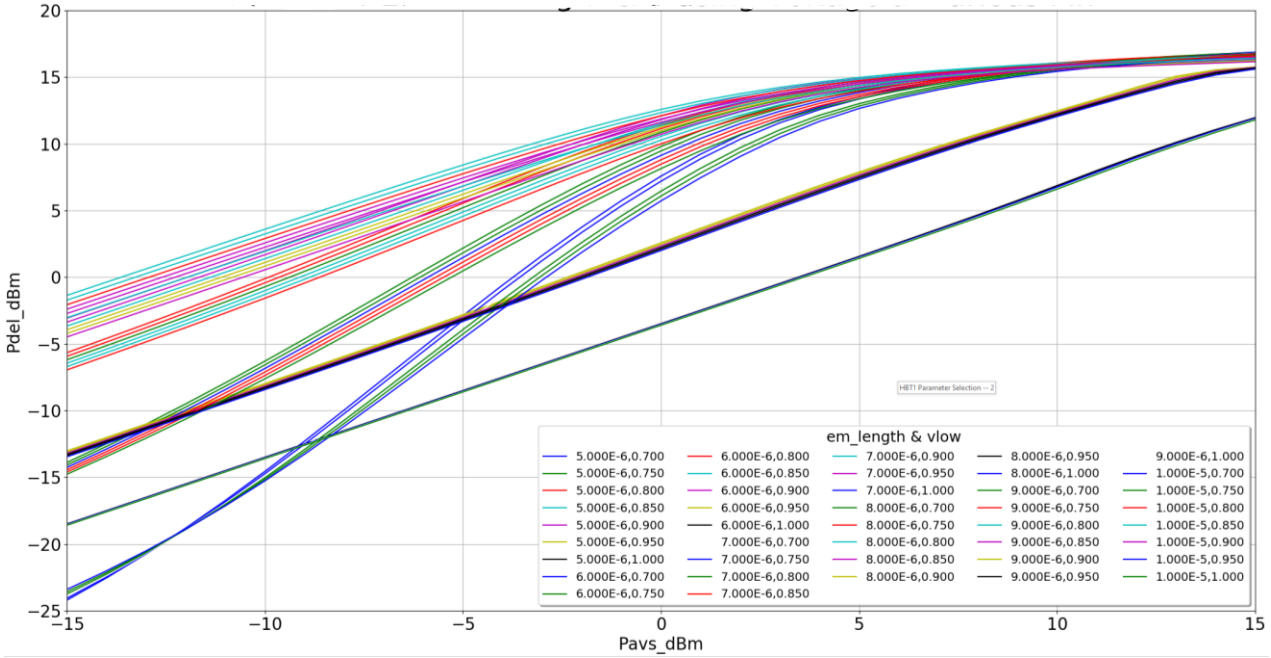

Figure 3. 19 - Stage 1, Tripler Block: output power versus emitter length, bias voltage and input power

In addition, some more detailed simulations are made regarding the parameters whose values are scanned. In the following Figures 3.20 - 3.22 we see the output power, for different values of the input power, with respect to the transistor size only, and with respect to the bias voltage respectively.

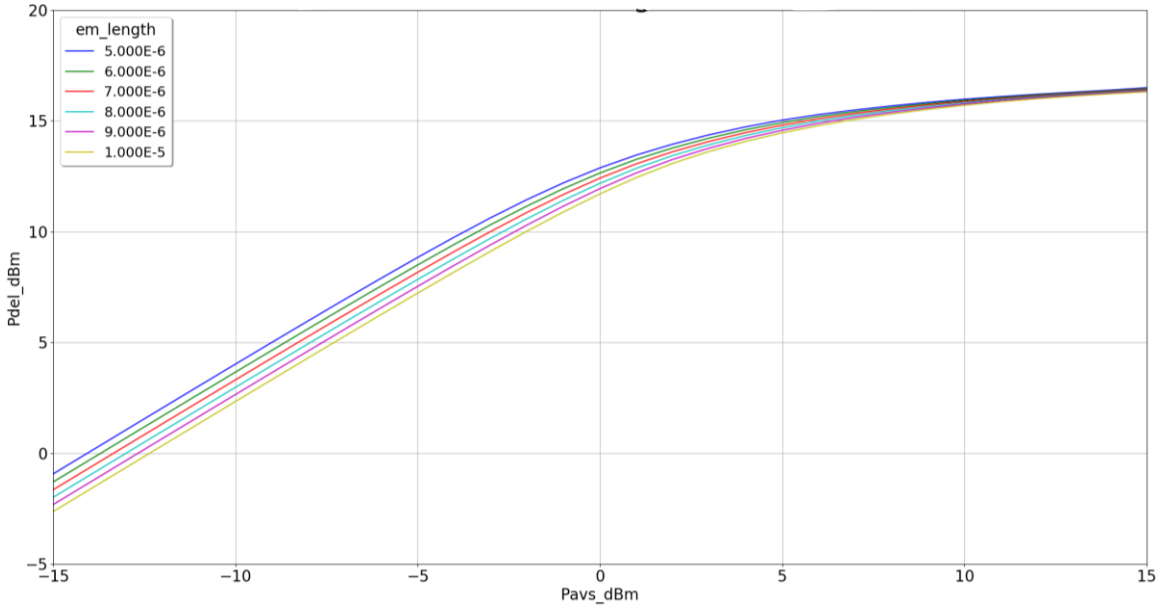

Figure 3. 20 - Stage 1, Tripler Block: output power versus emitter length

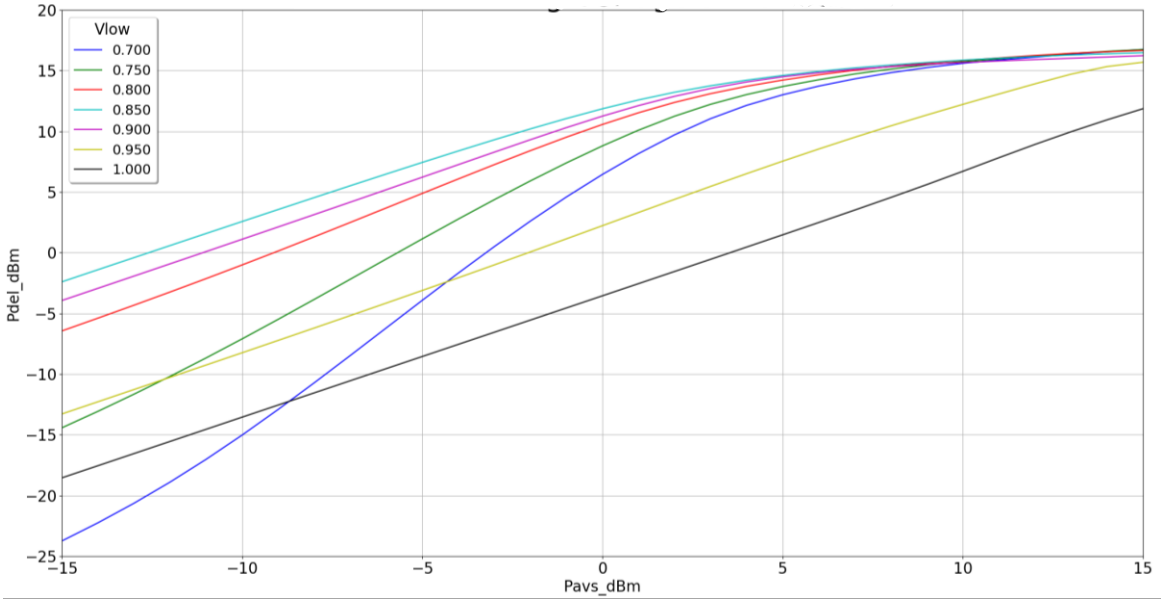

Figure 3. 21 - Stage 1, Tripler Block: output power versus bias voltage

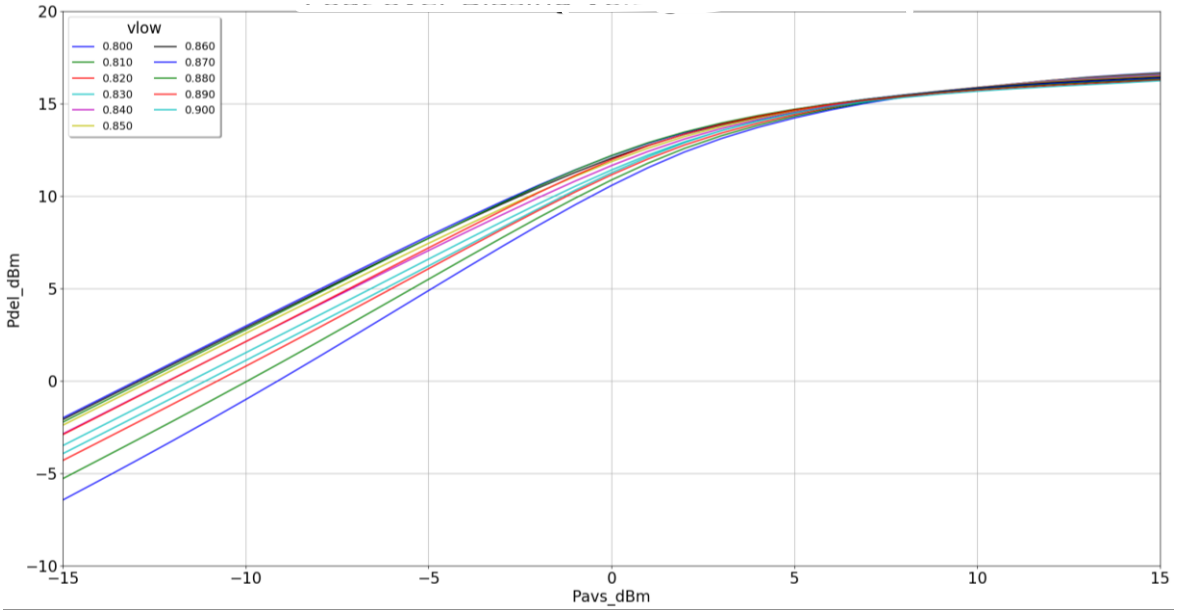

Figure 3. 22 - Stage 1, Tripler Block: output power versus bias voltage (2)

3.5.2 2nd Stage – Tripler Block

The second stage of the Tripler Block, aims to excite the above harmonics, specifically the 3rd harmonic component, hence it is to be biased as a Class C amplifier. A first approximation of the parameter value scan is shown below, in Figure 3.23.

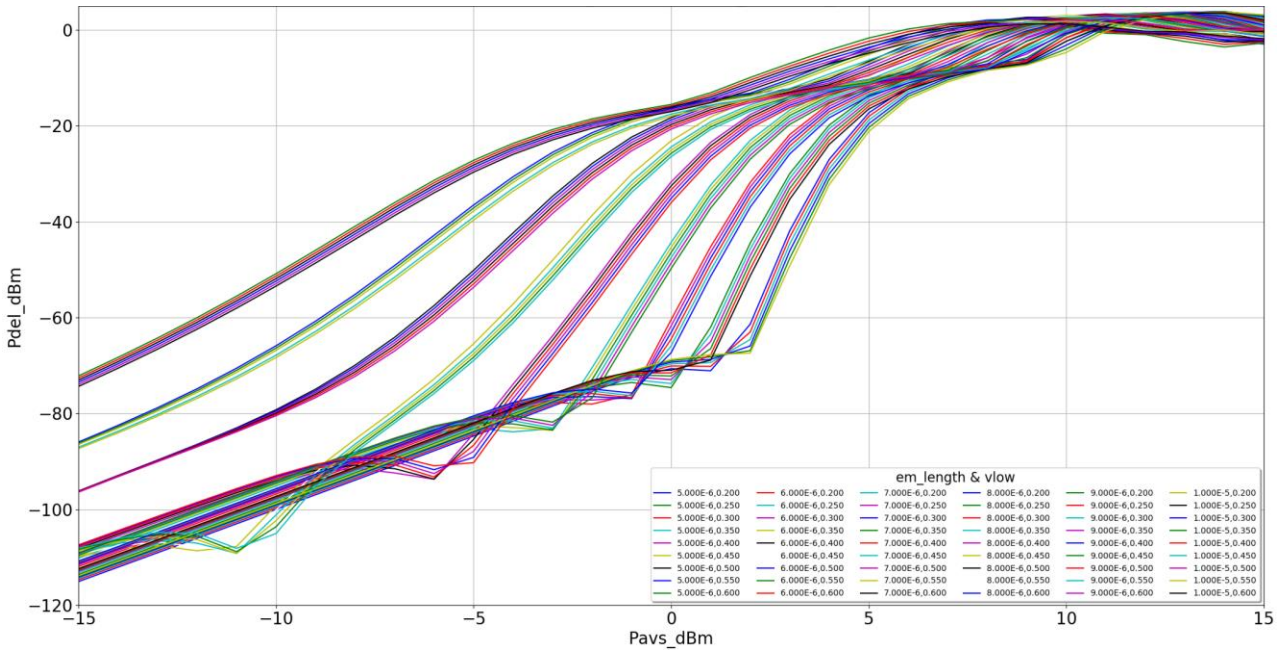

Figure 3. 23 - Stage 2, Tripler Block: output power versus emitter length, bias voltage and input power

Again, some more detailed simulations are made regarding the parameters whose values are scanned. In the following Figures 3.24 - 3.26 we see the output power, for various values of input power, with respect to transistor size only, and with respect to bias voltage respectively, from which the final selection of the requested parameters is derived.

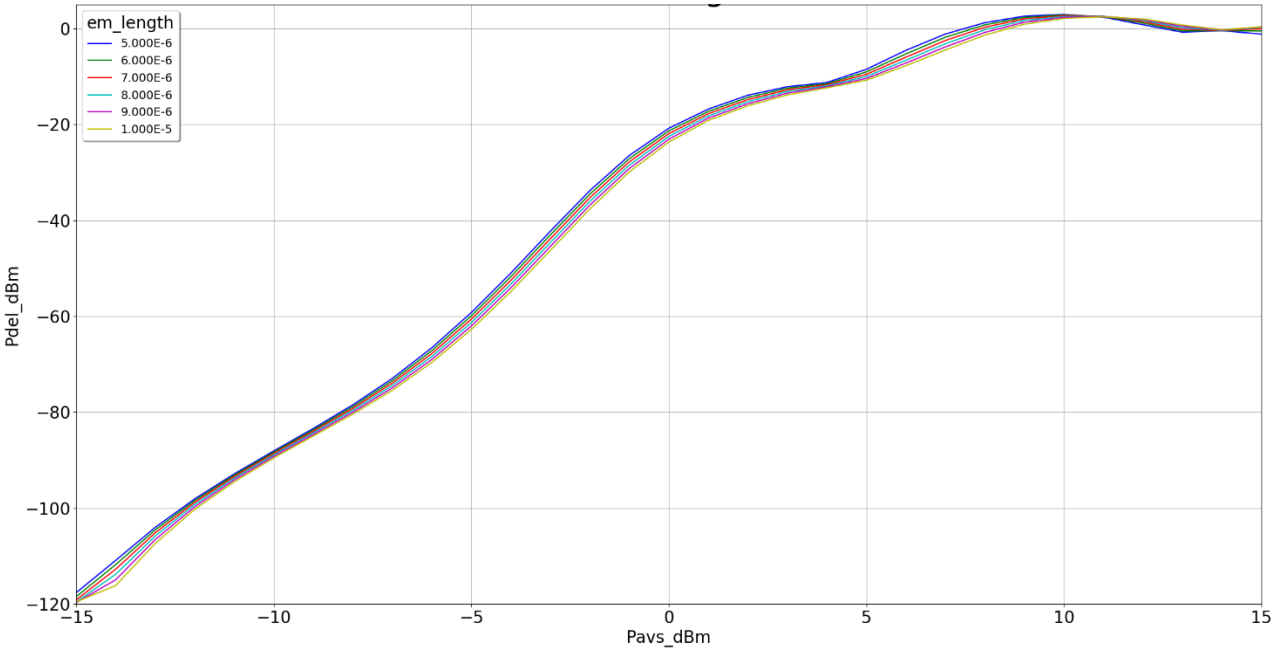

Figure 3. 24 - Stage 2, Tripler Block: output power versus emitter length

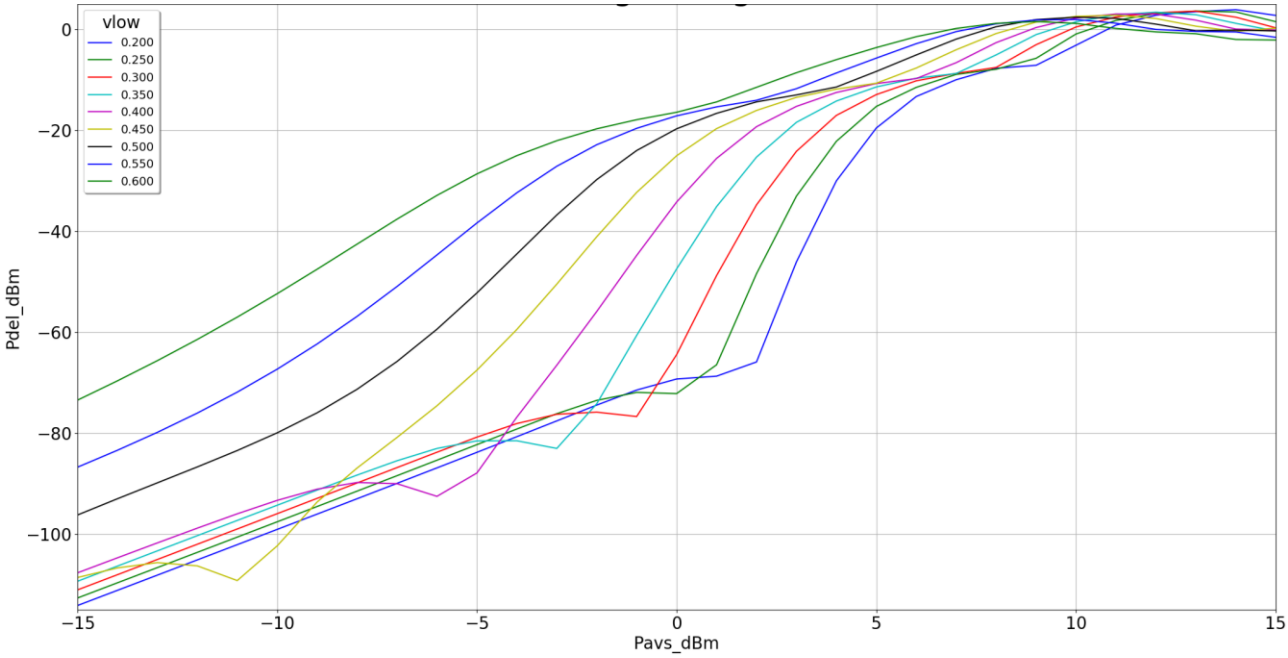

Figure 3. 25 - Stage 2, Tripler Block: output power versus bias voltage

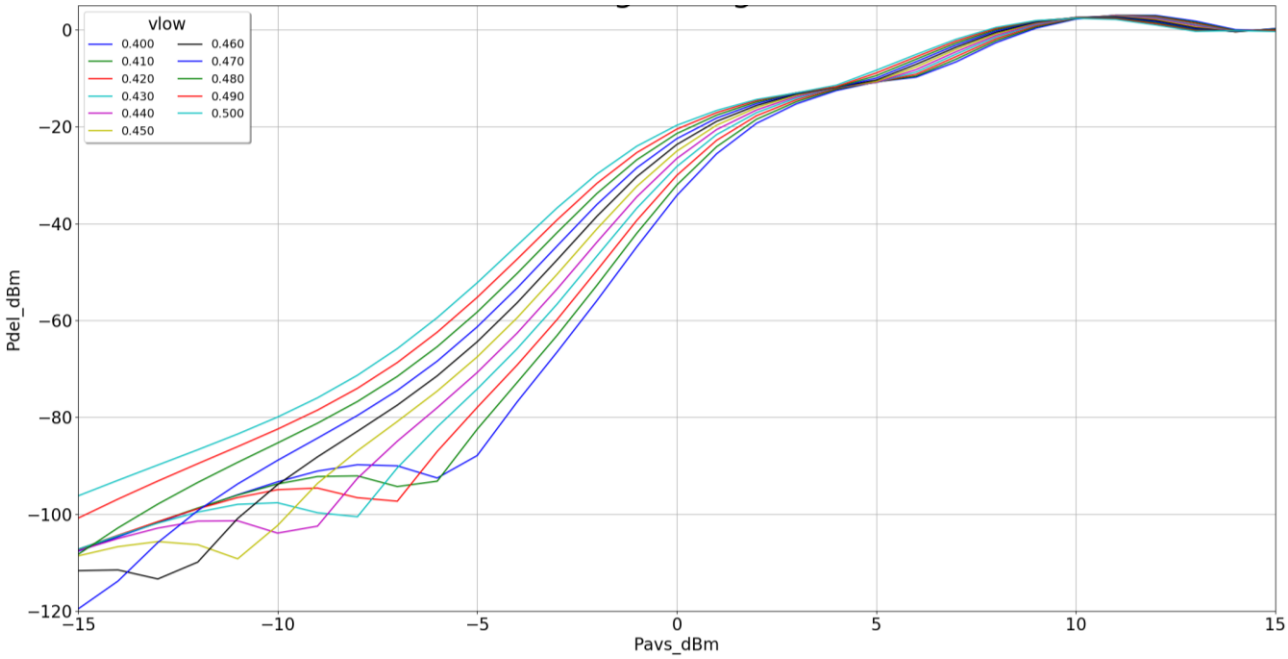

Figure 3. 26 - Stage 2, Tripler Block: output power versus bias voltage (2)

3.5.3 1st & 2nd Stage – Power Amplifier Block

The first and second stages of the Power Amplifier Block, aim to amplify the third harmonic produced by the Tripler Block. For this purpose, they are to be biased as Class A amplifiers. The difference with respect to the third and last stage of the Power Amplifier Block, as we will see in more detail below, lies in the fact that in the first

two stages conjugate matching is used, while on the contrary, the last stage uses the Load Pull technique, which will be analyzed later in subsection 3.5.4. A first approximation of the scanning of the parameter values for the active devices in the first two stages of the PA Block is therefore shown below, in Figure 3.27.

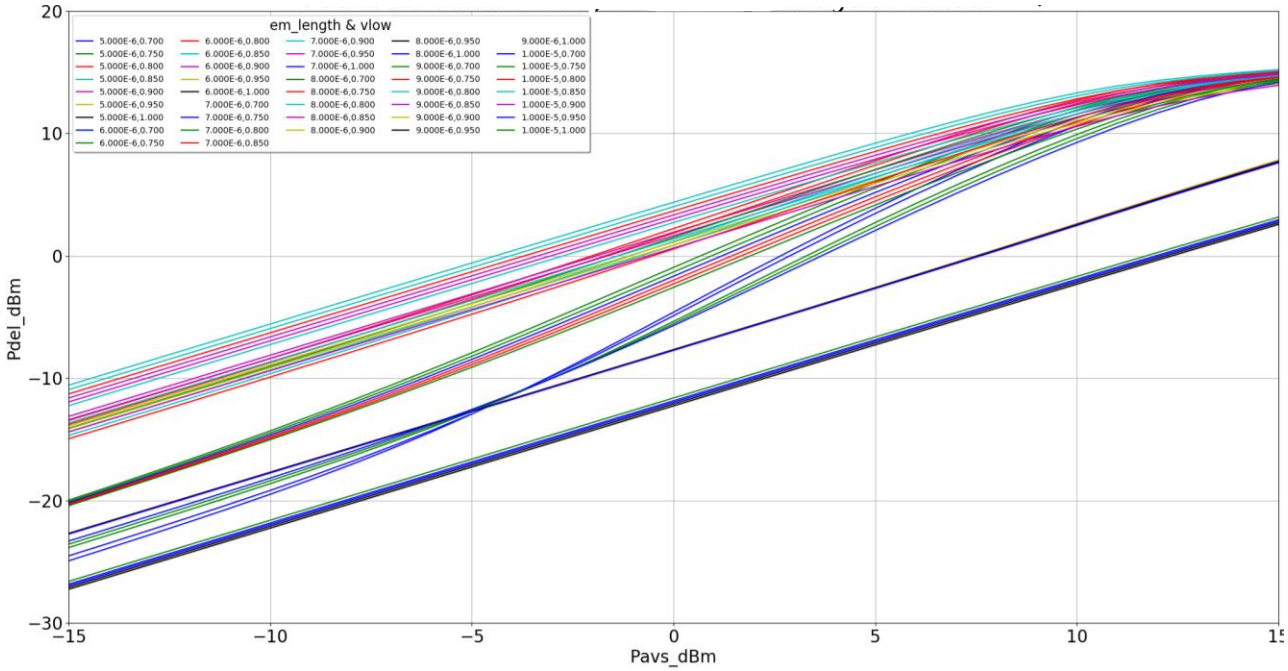

Figure 3. 27 - Stage 1 & 2, PA Block: output power versus emitter length, bias voltage and input power

As for the Tripler Block stages, the more detailed simulations, that follow the general one, give us the final choice of the requested parameters. In the following Figures 3.28 - 3.30 we see the output power, for various values of input power, with respect to transistor size only, and with respect to bias voltage respectively, from which the final selection of the requested parameters is derived.

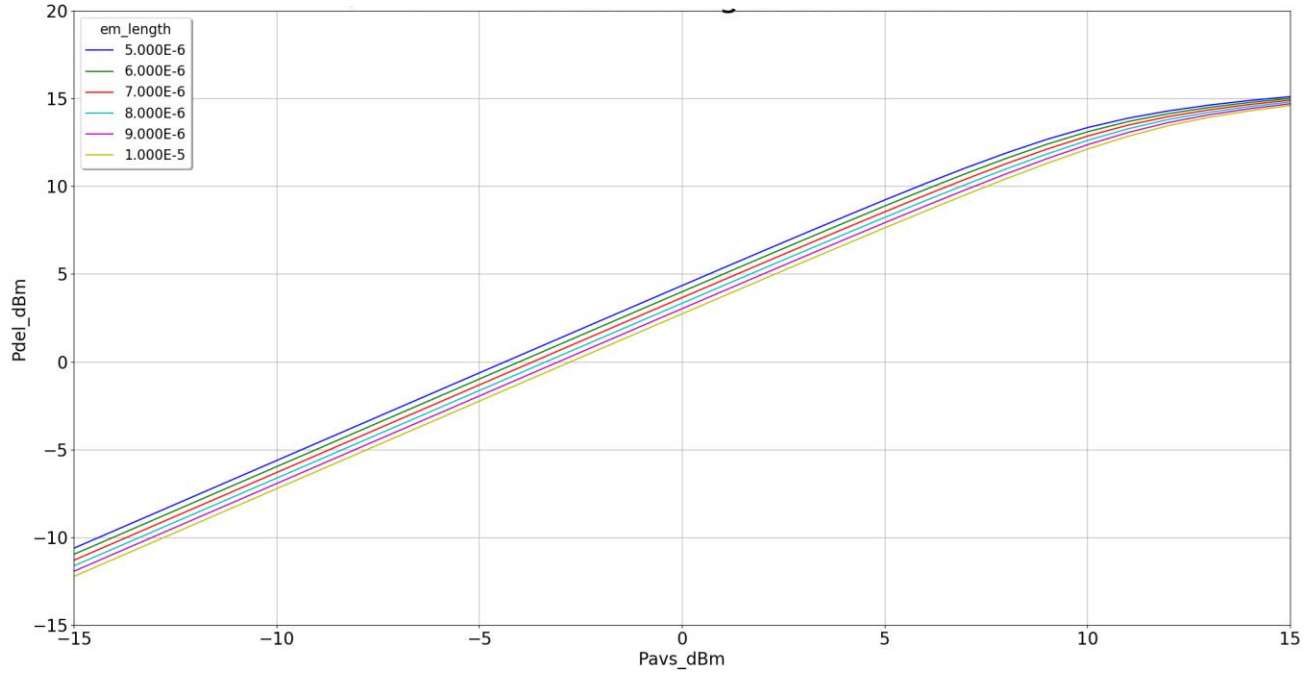

Figure 3. 28 - Stage 1 & 2, PA Block: output power versus emitter length

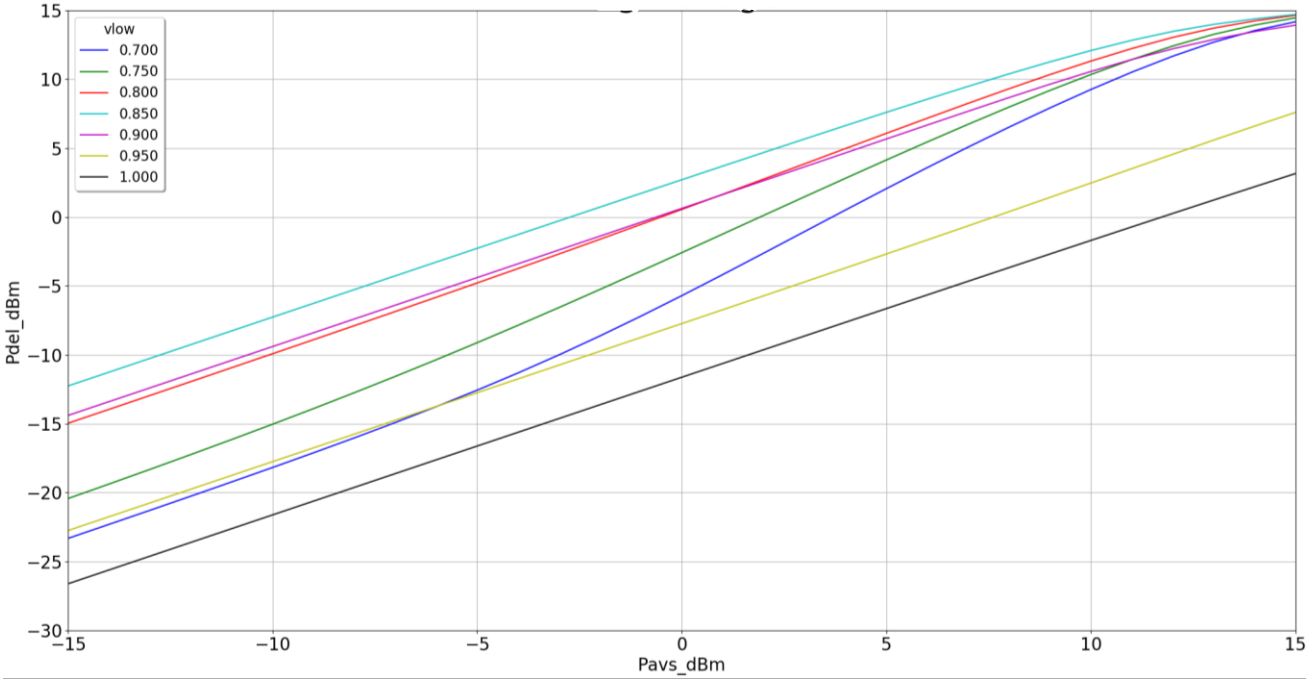

Figure 3. 29 - Stage 1 & 2, PA Block: output power versus bias voltage

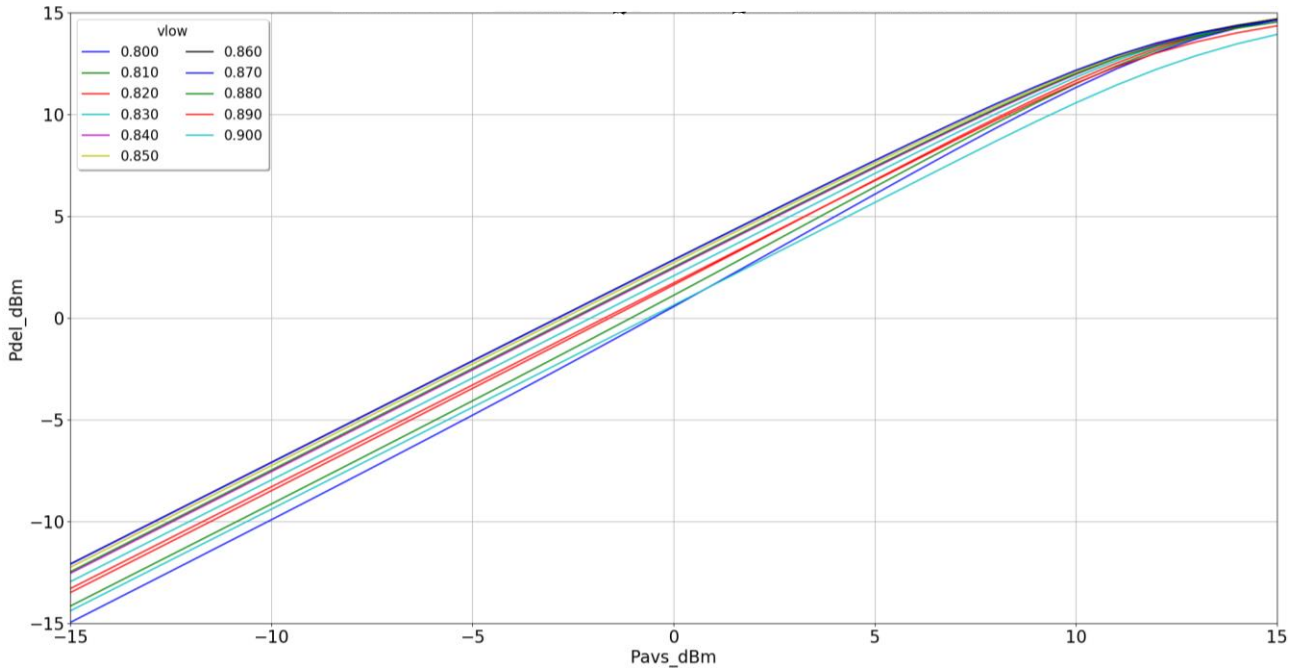

Figure 3. 30 - Stage 1 & 2, PA Block: output power versus bias voltage (2)

3.5.4 Load – Pull Technique

The Load Pull technique is a measurement method in which the characteristics of a device are measured while the load impedance is modified using an impedance resonance system.

Load Pull analysis is used to construct a set of contours, which determine the maximum output power that can be achieved given the load impedance. These contours are very useful for evaluating the actual impedance that a device should see when used in an amplifier.

The ADS program used for the circuit design in this paper offers a ready-made Load Pull tool, with the only requirement being the input of the device for which we want to perform the Load Pull analysis. The procedure followed is to start by creating a new schematic. Then, from the options tab, we navigate to the Design Guide option, and from there we select the Load Pull technique. These options described are represented below in Figure 3.31:

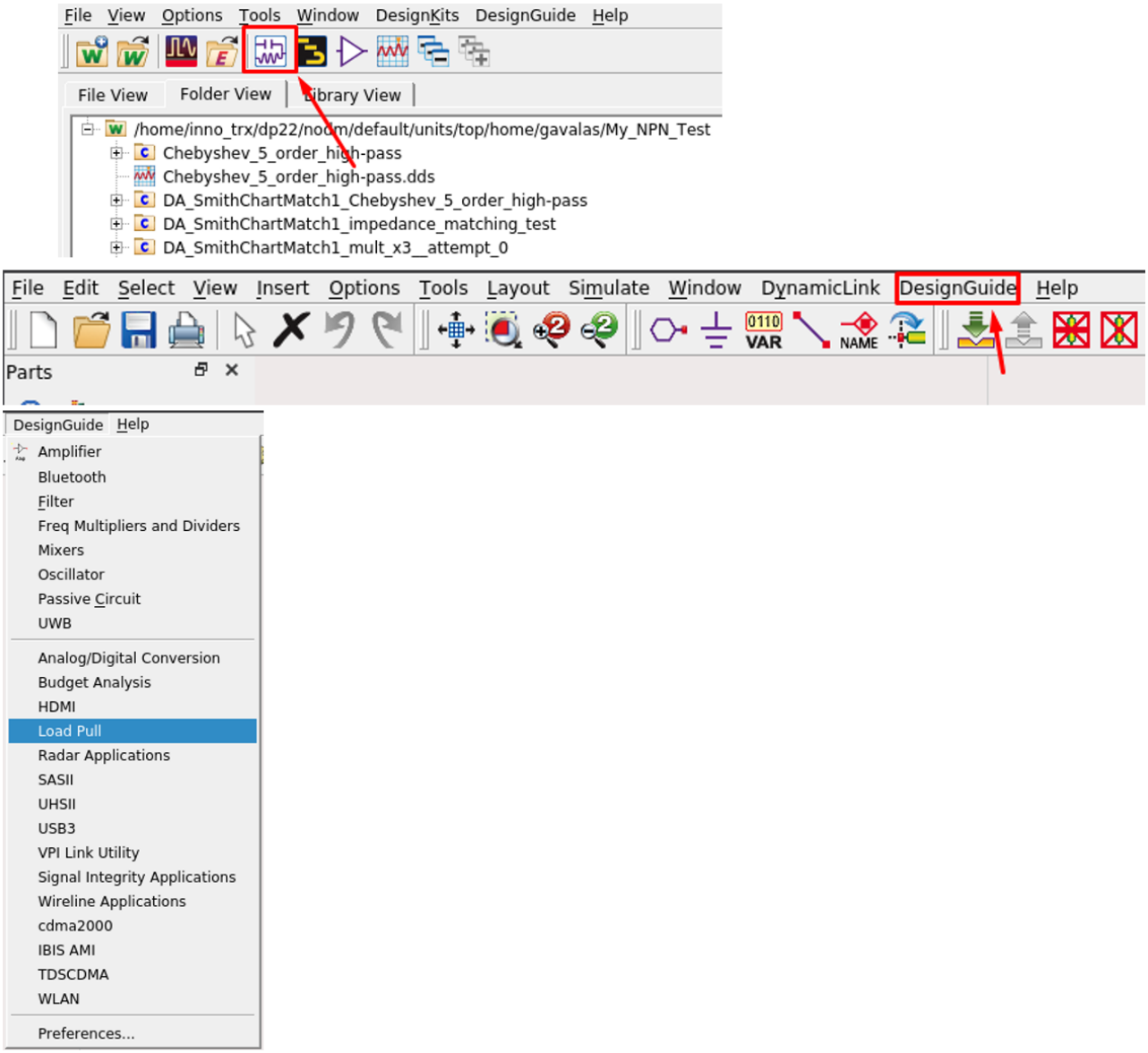

Figure 3. 31 - Options for using the ADS Load Pull tool

Within the Load Pull tool which was opened by the aforementioned procedure, we see the schematic of Figure 3.32. In it, we observe the Load Pull Instrument along with the characteristics that describe it, such as the supply and bias voltages, the frequency and power of the signal, the number of points of the contours for which the check will be performed, the maximum radius of the points under control from the center point, and others. In addition, we also see the symbol of the device under test (DUT) for which the Load Pull analysis is performed.

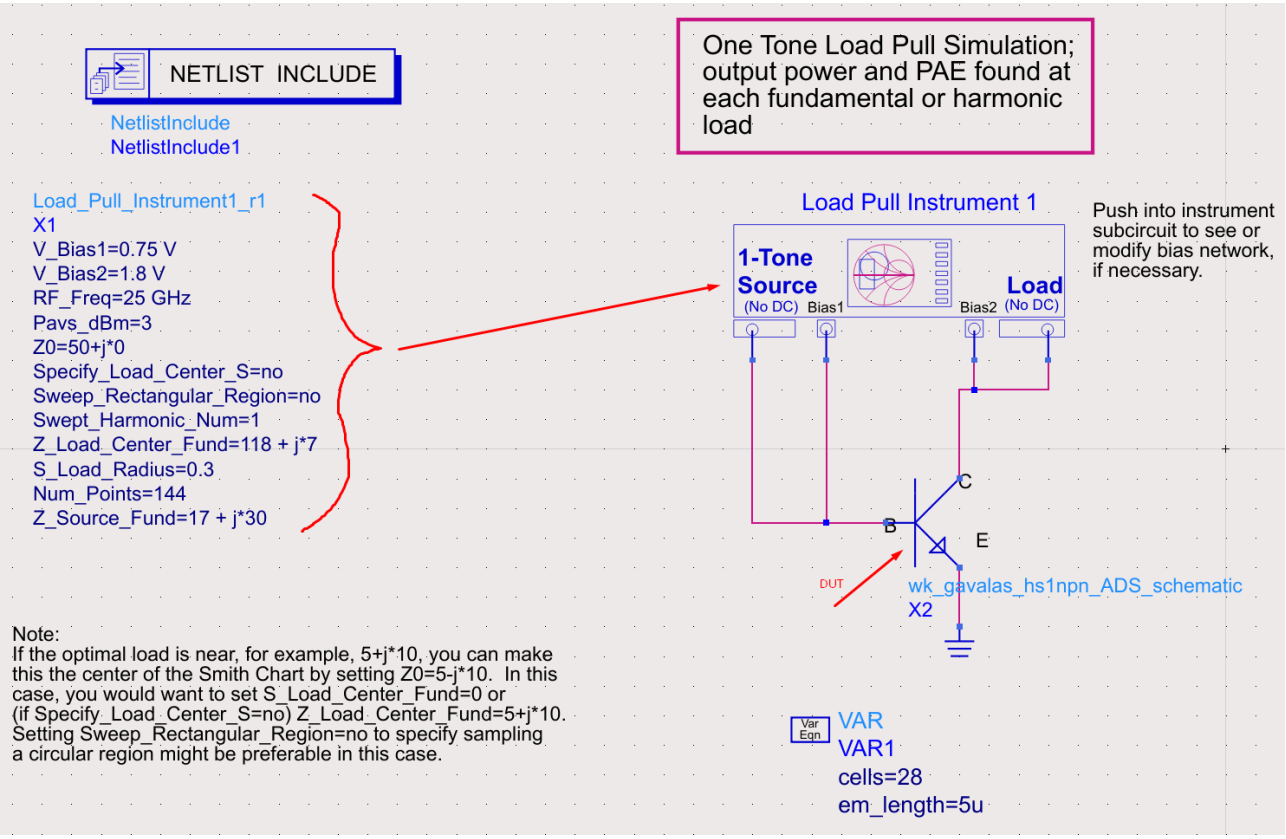

Figure 3. 32 - Schematic within the ADS Load Pull tool

Finally, by running the simulation, we get the requested contours, from which we see the maximum power that our device can deliver, with the given input signal, for each value of load impedance for which we checked. In addition, we are given the value of the impedance for which the maximum power is achieved overall, as well as the value for which the maximum efficiency is achieved when the gain is taken into account. The contours with this information are shown in Figure 3.33.

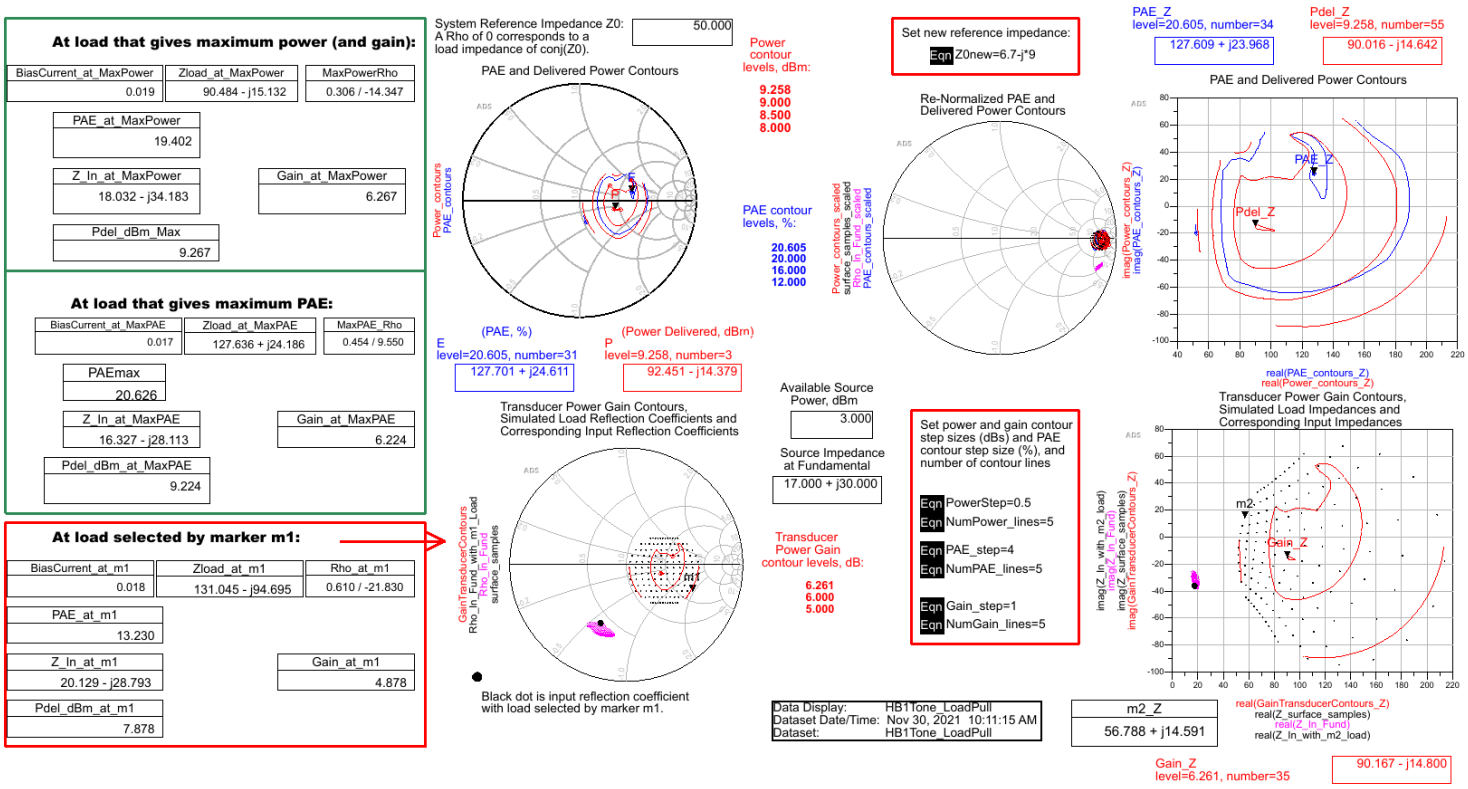

Figure 3. 33 - Load Pull descriptions of the device under test

Another option for Load Pull available from ADS is simulation with the input signal strength as a parameter. Doing so offers the advantage of identifying the output power for a multitude of input power values, as well as the impedance of the load and the input power to achieve the maximum gain and/or the lowest power consumption.

Below, Figures 3.34 - 3.36 show the contours obtained from the Load Pull analysis with input power parameter scanning. In particular, Figure 3.34 shows the input power and load impedance for maximum gain, maximum efficiency with gain included, and minimum gain compression. Figure 3.35 shows the contour and parameters for minimum power consumption. Finally, in Figure 3.36 we see the maximum output power and the value of the load impedance for each value of the input power.

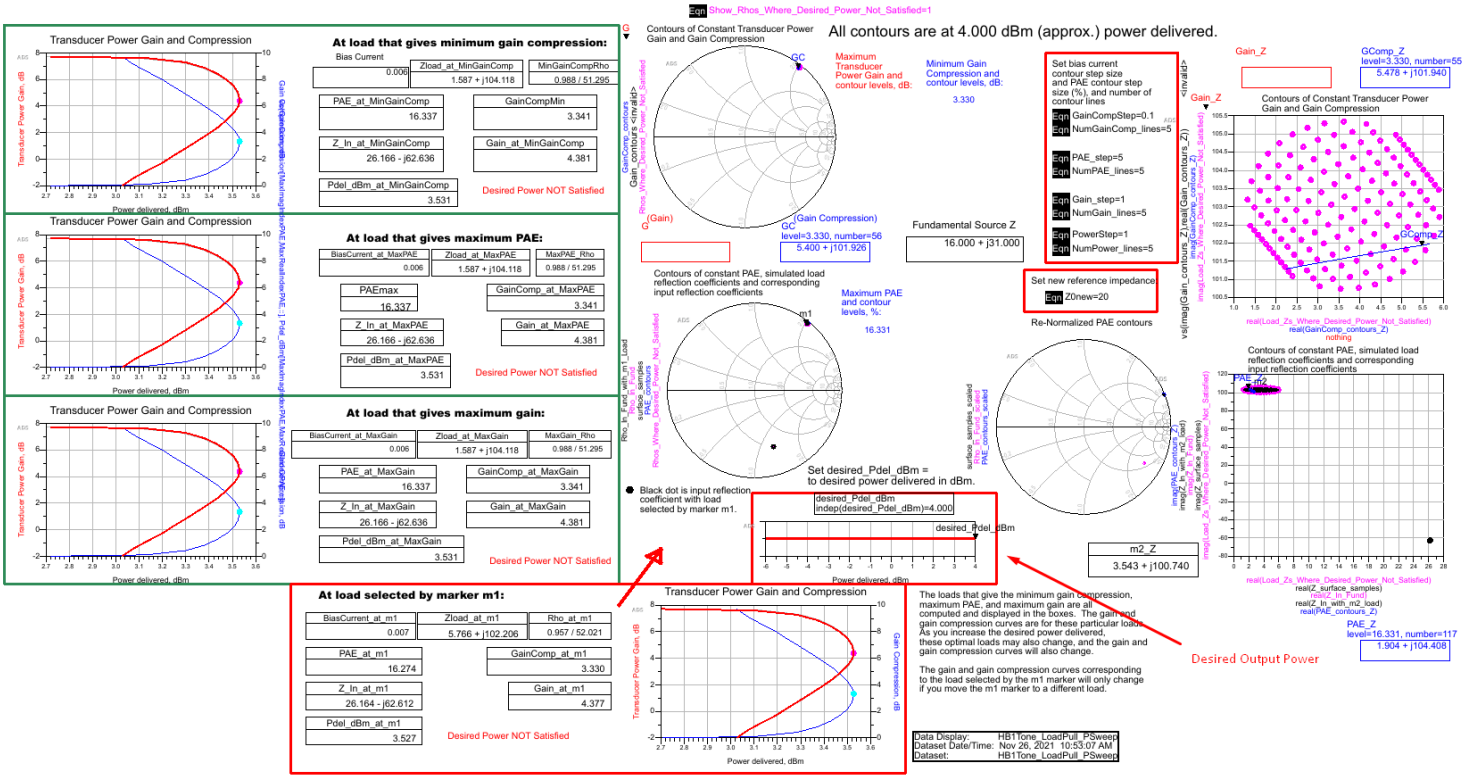

Figure 3. 34 - Load Pull Contours under parametric input power (1)

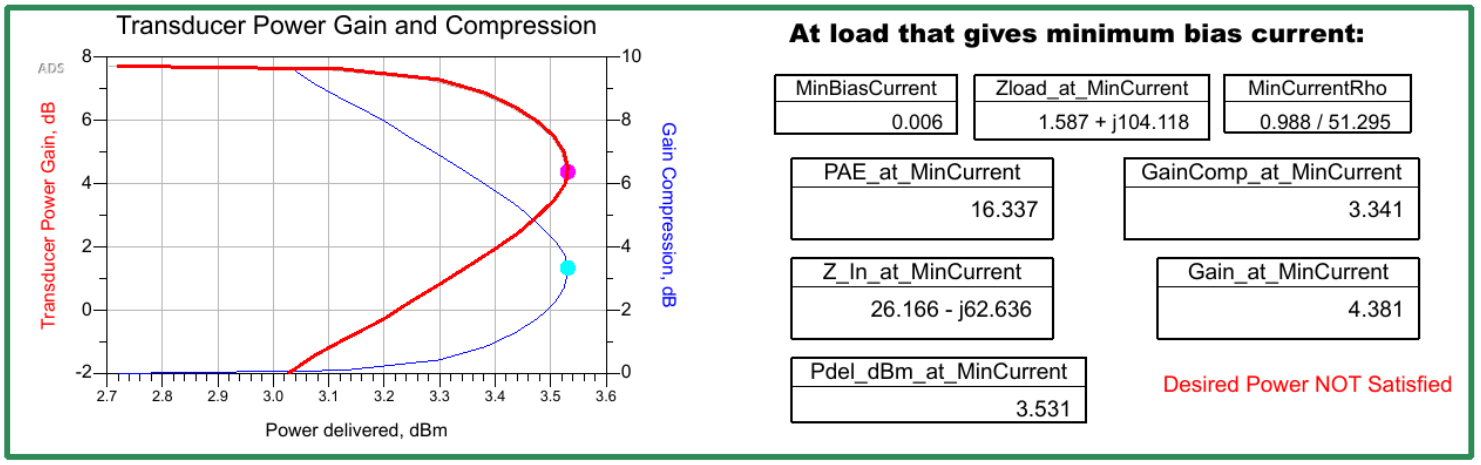

Figure 3. 35 - Load Pull Contours under parametric input power (2)

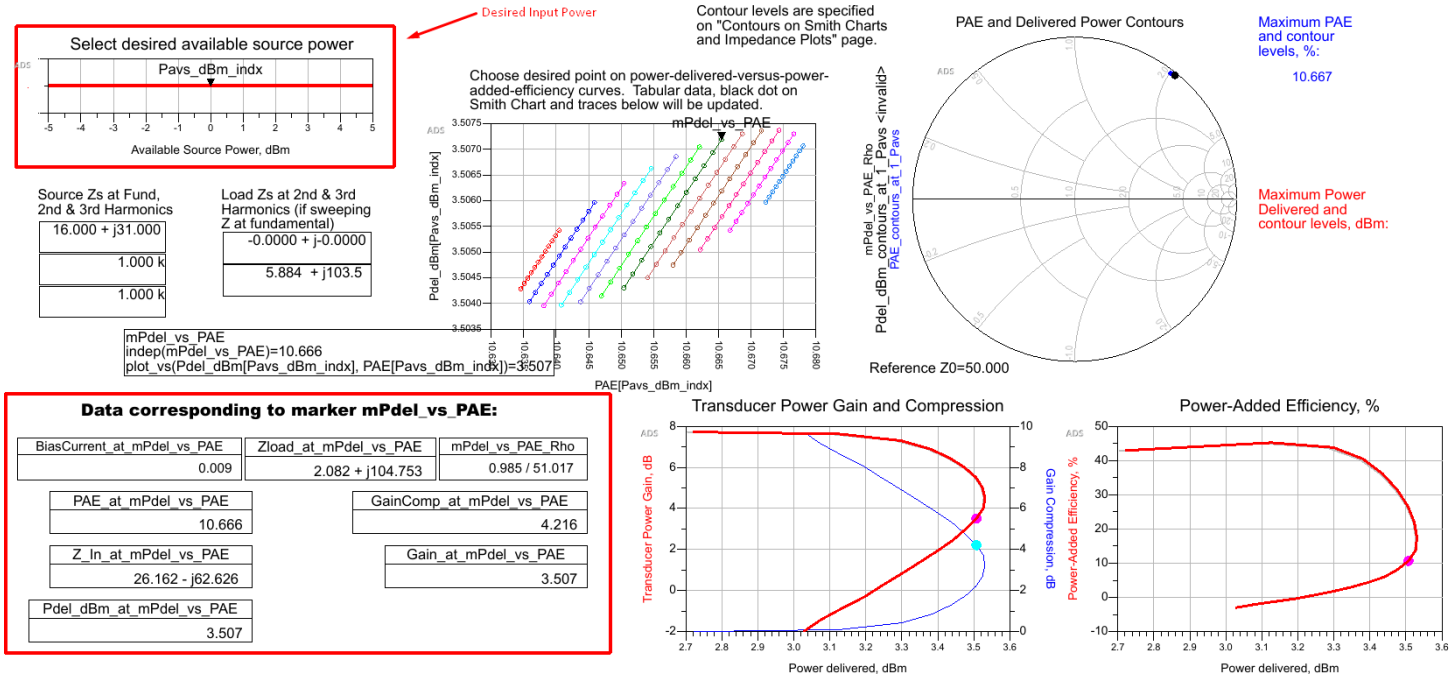

Figure 3. 36 - Load Pull Contours under parametric input power (3)

3.5.5 3rd Stage – Power Amplifier Block

The third and final stage of the Power Amplifier Block, aims to deliver the maximum power value at the output of the frequency multiplier. For this purpose, given the signal provided at its input, from the output of the second stage, the Load Pull analysis is performed, as described in the previous subsection. The result of the contour for this third stage device is shown in Figure 3.37.

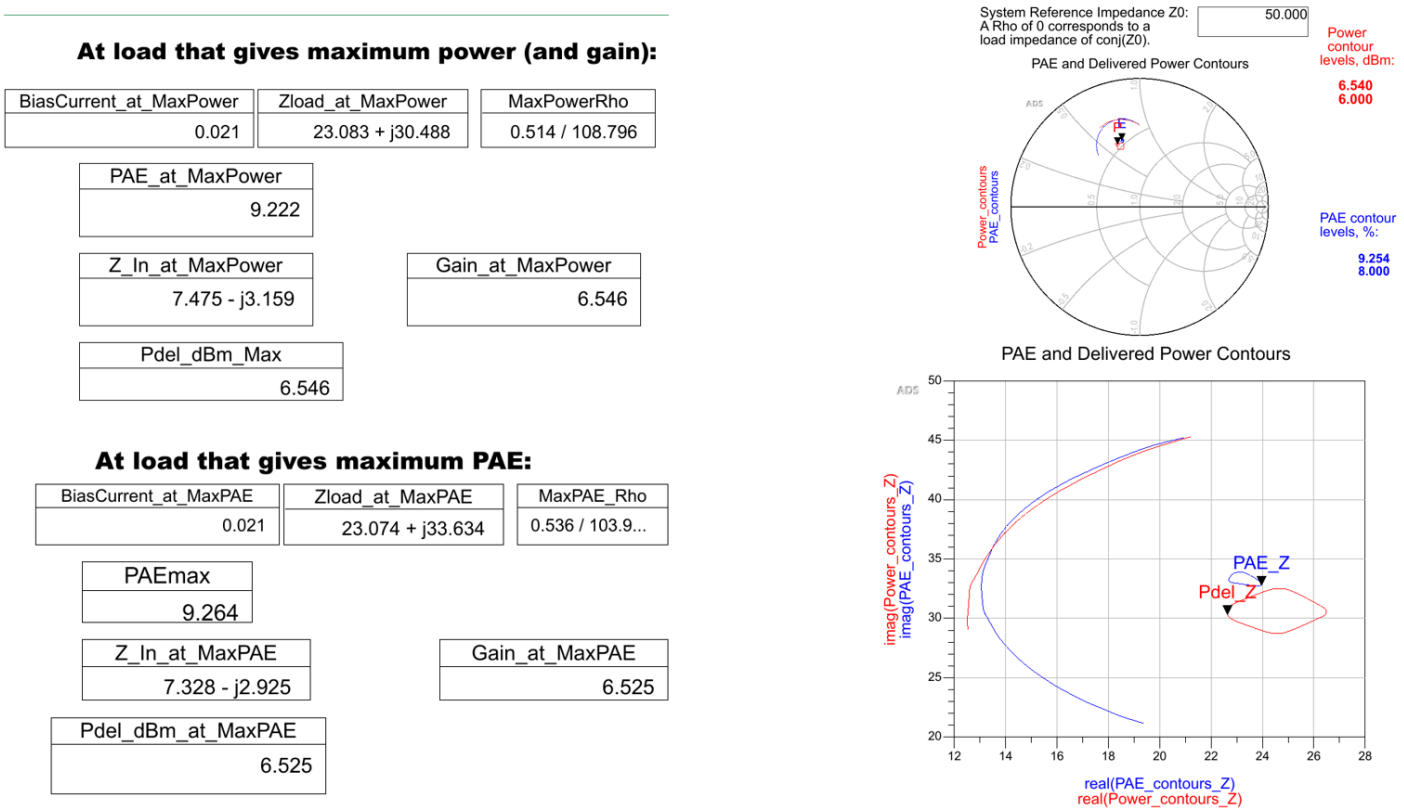

Figure 3. 37 - Load Pull diagram for the 3rd stage of the PA Block

Having therefore analyzed and listed the simulations for each active device to be used in the individual stages of the overall frequency multiplier, we have the results for their parameter values in the following Table 3.2:

Parameter	HBT1	HBT2	HBT3	HBT4	HBT5
Supply	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
Size	8μm	8μm	10μm	10μm	10μm
Bias	0.87 V	0.47 V	0.875 V	0.875 V	0.875 V

Table 3. 2 - Parameters and characteristics of active devices

3.6 Design of matching networks

Having selected the active devices of our circuit, based on what was discussed in the previous section, the next part is the design of the matching networks located between the active devices. The role of these networks is to pass the desired signal, at its frequency and power, as best as possible, by synchronously adjusting the impedances that the active devices wish to "see".

The matching networks that are therefore called upon to be designed are, for the Tripler Block, the input matching network and the intermediate two-stage matching network. For the Power Amplifier Block, we design the two intermediate matching networks as well as the output matching network, based on the load impedance found through the Load Pull technique. Of course, the intermediate matching network that connects these two blocks must also be designed, in order to finally synthesize the entire frequency multiplier.

To design these matching networks, some elements are used which help us to observe the impedance that each transistor "sees" in its base and collector. Next, use is made of a tool called Smith Chart Utility that is built into the ADS. More about this tool can be found in the following subsection.

3.6.1 Smith Chart utility and matching network design

The ADS Smith Chart utility provides full Smith chart and mesh fitting capabilities, allowing for complex impedance fitting. The Smith Chart tool is set up by the following steps, followed by the corresponding Figures:

1) Open the desired schematic
2) Find the "Smith Chart Matching" option from the component libraries, as in Figure 3.38
3) Place the "Smith Chart Matching Network" element, as in Figure 3.39
4) Navigate to Tools → Smith Chart... , as in Figure 3.40

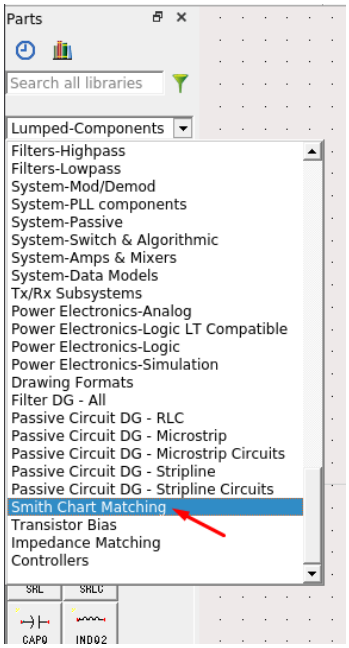

Figure 3. 38 - Smith Chart Matching library selection

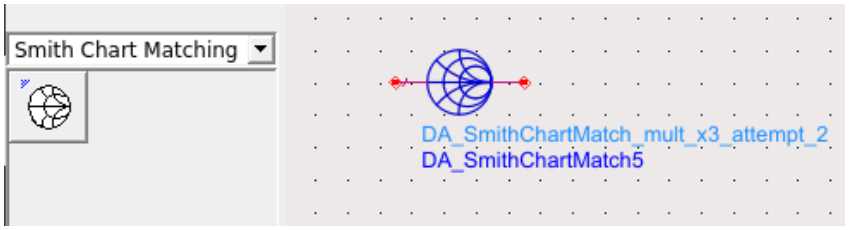

Figure 3. 39 - Smith Chart Matching Network element selection

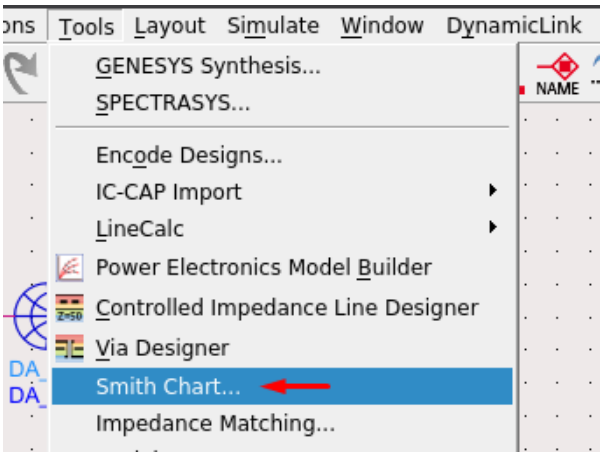

Figure 3. 40 - Navigate to Tools → Smith Chart...

The window that opens from which the design of the matching network is performed is shown in Figure 3.41. In it, we select the desired frequency for which we are designing the matching network. We set the impedances for which we want to perform the matching. Specifically, we fill in the corresponding fields, the conjugate impedance of the input and the impedance of the output. Having thus defined the characteristics of the desired design, we select the elements that will form the network from the options palette. The goal is to create a path between the two dots representing the two impedances. When the results of our network, whose S-Parameters are shown in the top and right corners of the window, are satisfying, we synthesize the network and can use it in our circuit.

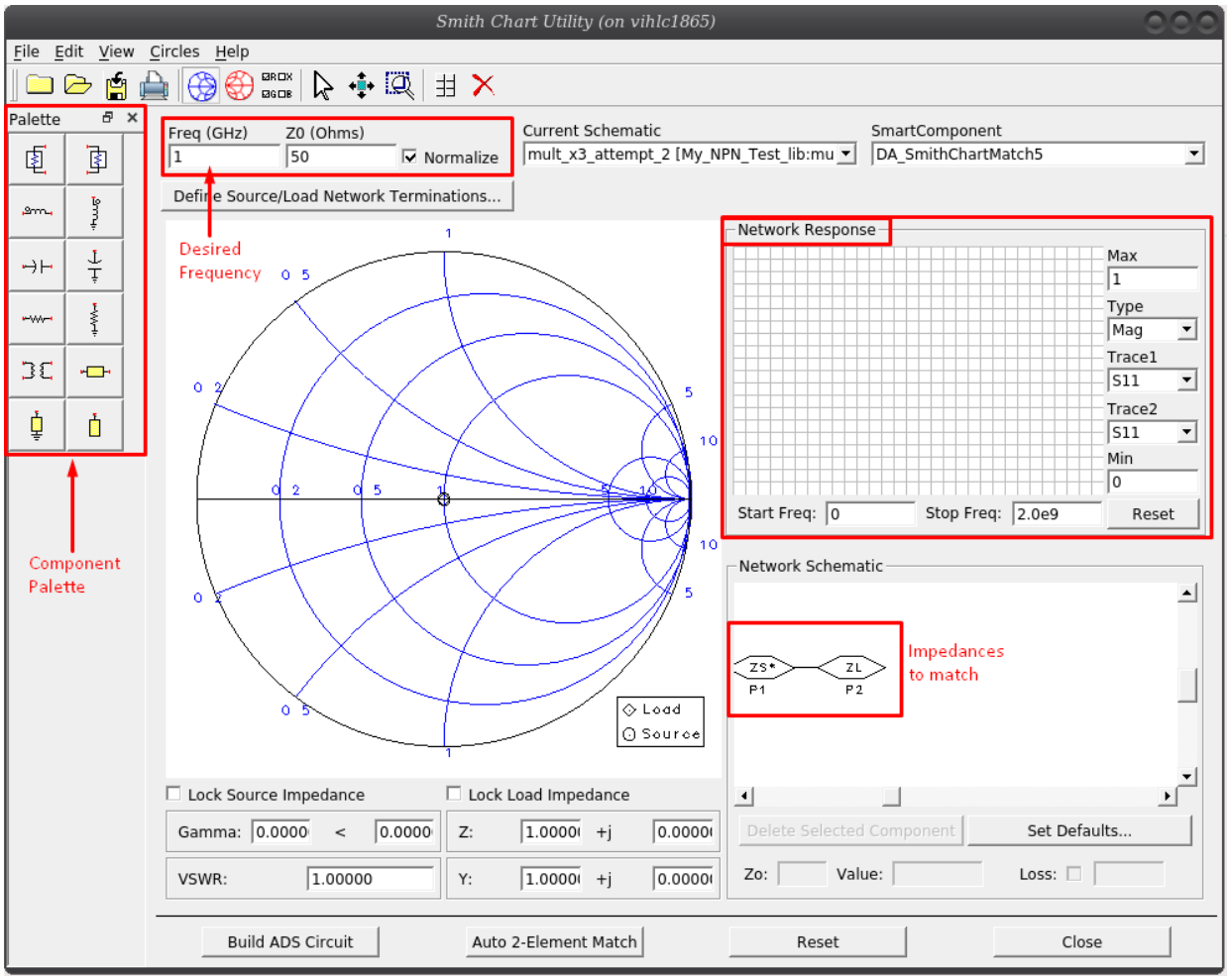

Figure 3. 41 - Smith Chart utility window

After creating the matching network, in the manner described, with the ideal elements of the Smith Chart utility, we create the corresponding adaptation network using the B11HFC technology elements. Subsequently, we run the necessary simulations, such as

for example S-parameter analysis, and compare the behavior between these two networks. Depending on the results, we make the necessary corrections to the network with the B11HFC elements and repeat our simulations. When now the results are satisfying, we can use the generated network in our frequency multiplier circuit.

3.6.2 Input matching network

In the input matching network, we seek matching between the 50+j·0 Ω source impedance and 9.88- j·16.8 Ω impedance that the active device base of the first stage Tripler Block "sees". This adjustment is made at the centered at 48 GHz which is the signal at the input of the frequency multiplier. Finally, the resulting network using the ADS Smith Chart utility is shown in Figure 3.42 below:

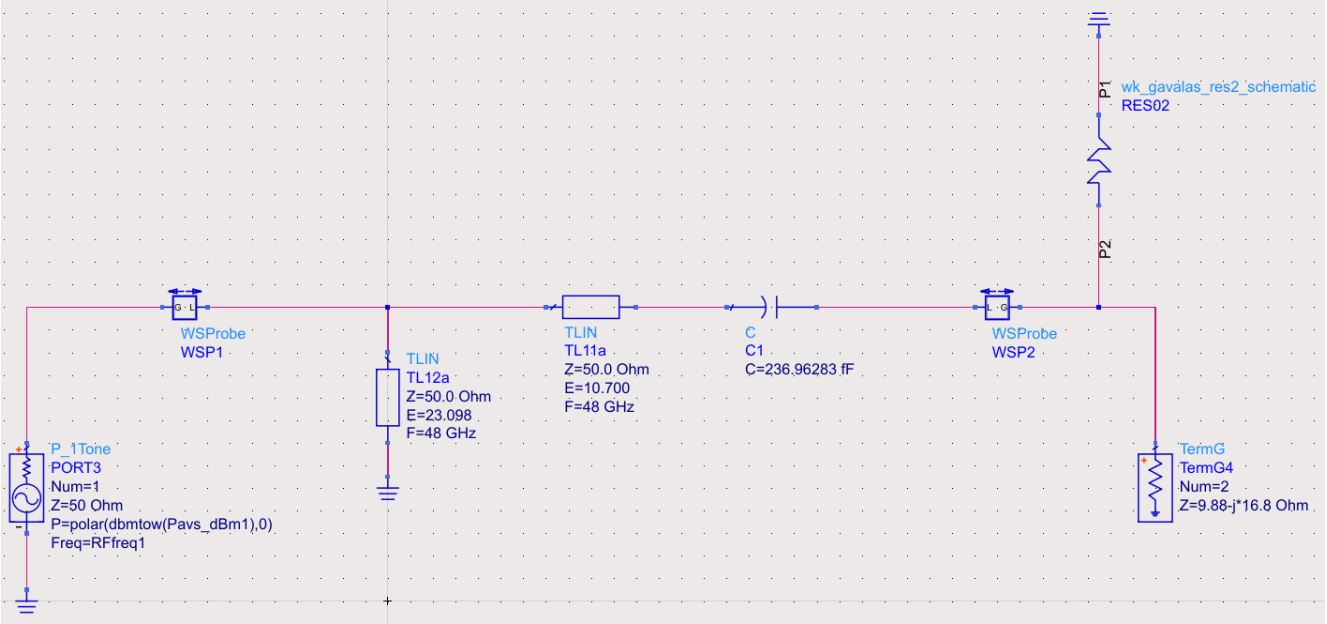

Figure 3. 42 - Input matching network with ideal elements

Next, as mentioned in the previous subsection, we replace the ideal network elements with the elements of the B11HFC models. To select the initial length of the B11HFC transmission lines, at 48GHz which is the central input frequency, we have:

$$l = 8.68 \cdot (\theta°)\ \mu m \tag{3.6}$$

After the initial values, the required adjustments and changes in the values of the elements, based on the simulation comparison results, lead to the final matching network, as shown below in Figure 3.43:

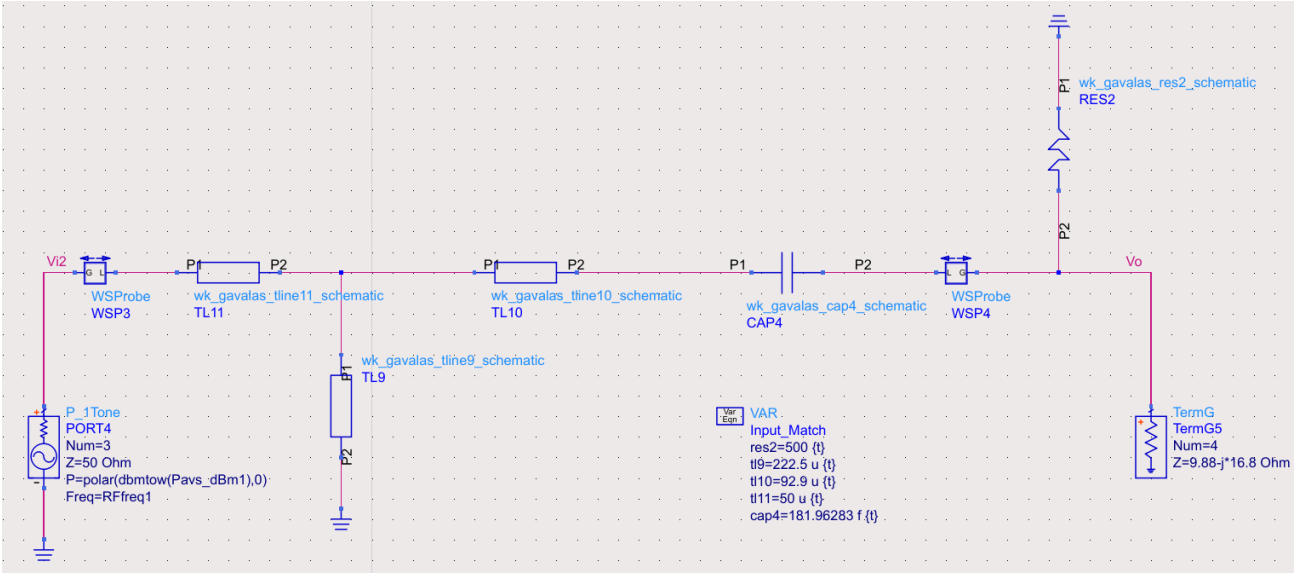

Figure 3. 43 - Input matching network with B11HFC elements

Finally, we check by simulation the S-parameters of the network, having replaced all the elements with those of the technology models. The results of this simulation, for the four S-Parameters, are shown in Figure 3.44.

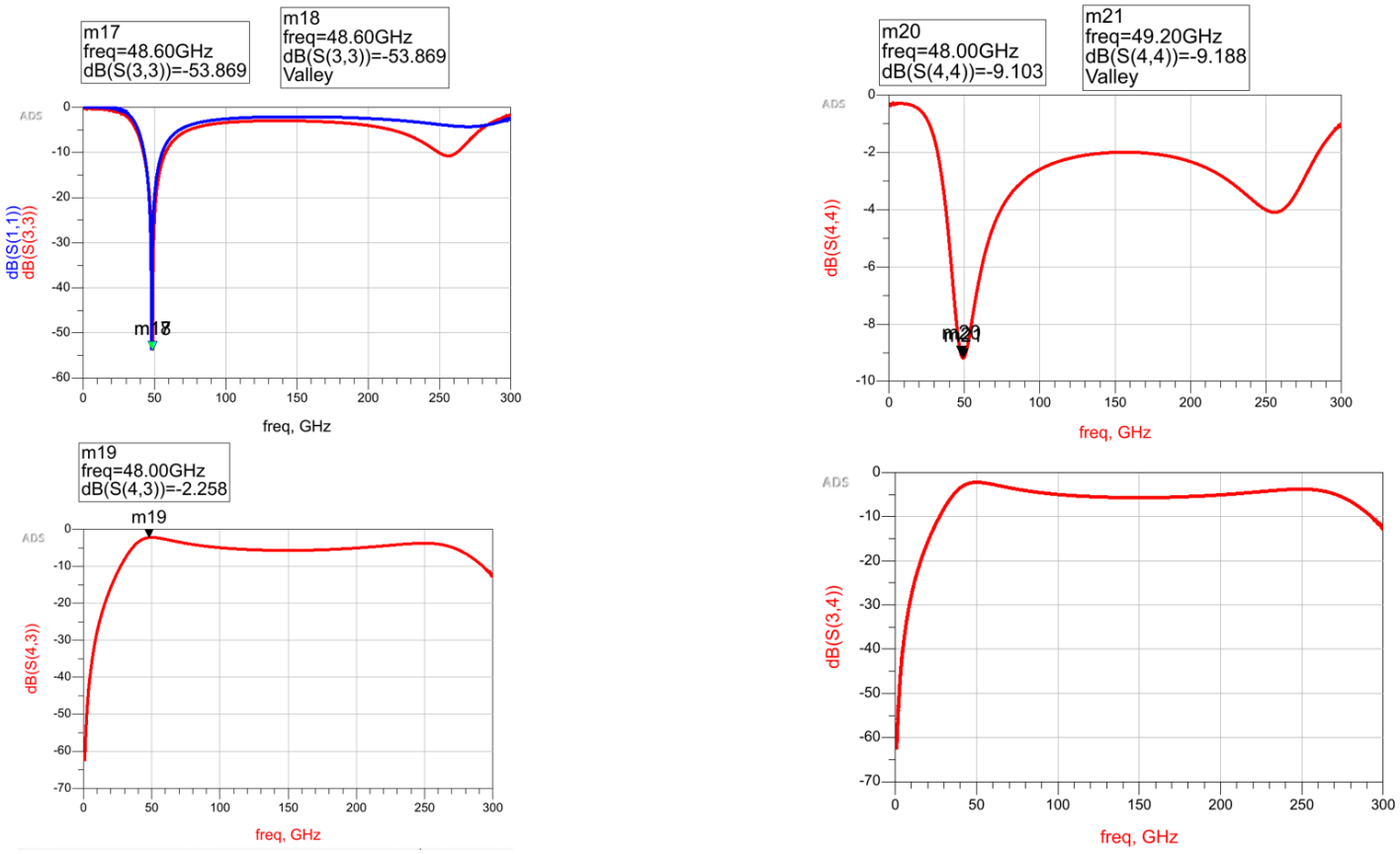

Figure 3. 44 - S-Parameters of the input matching network

3.6.3 Intermediate Tripler Block matching network

In the intermediate matching network of the Tripler Block, we seek to match between the composite loads of 33.4-j·58.1 Ω of the collector of the first stage active device and 9.6-j·105.5 Ω "seen" by the base of the second stage active device of the Tripler Block. This adjustment is centered at 48 GHz, which is the signal at the output of the first stage and at the input of the second stage frequency multiplier. Finally, the resulting network is shown in Figure 3.45 below:

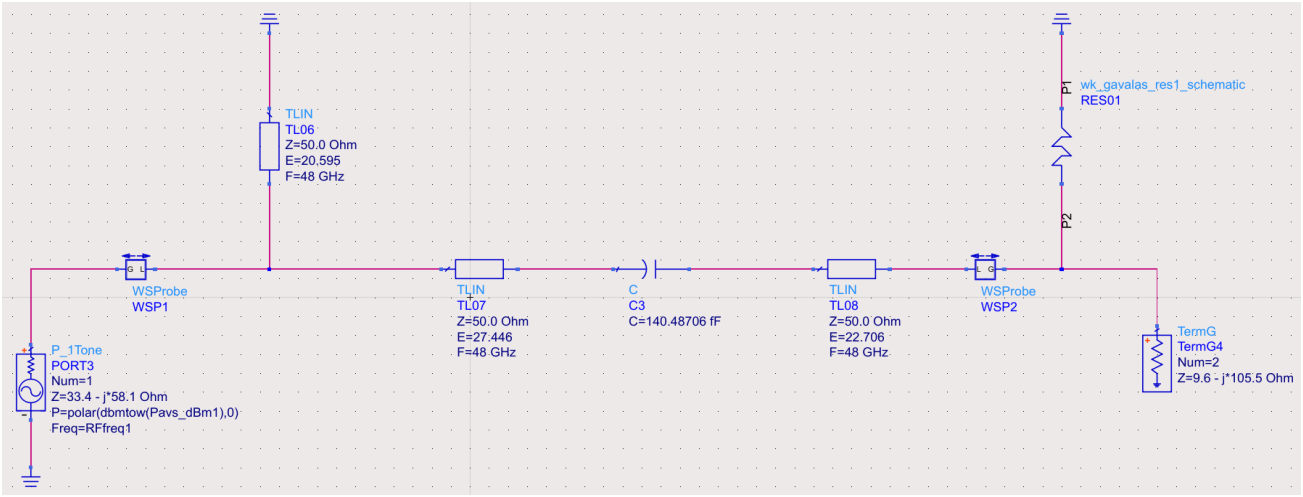

Figure 3. 45 - Intermediate Tripler Block matching network with ideal elements

Next, we replace the ideal network elements with the elements of the B11HFC technology models. Again, in order to select the initial length of the B11HFC transmission lines, at 48 GHz, we make use of equation (3.6).

After the initial values, the required adjustments and changes in the element values, based on the comparison results through simulations, lead to the final Matching Network, as shown below in Figure 3.46:

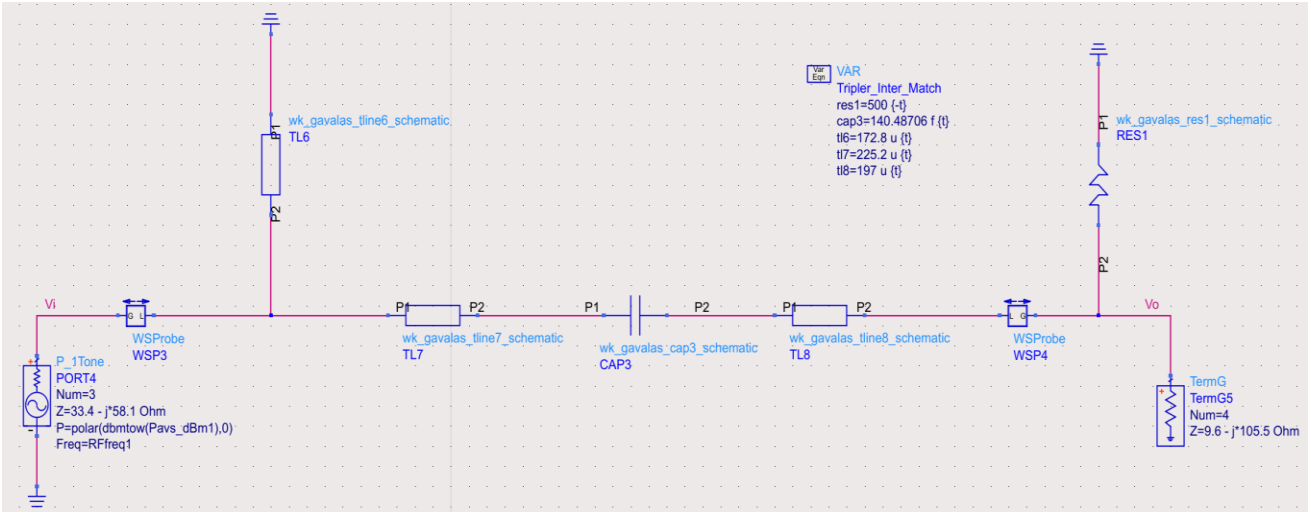

Figure 3. 46 - Intermediate Tripler Block matching network with B11HFC elements

In this case, a difficulty of accurate matching occurred, as indicated by Figure 3.47, for the following reason. The value of the imaginary part of the impedance at 48GHz for ideal elements, is approximately equal to 58 Ω. At the same time, however, the maximum value of the imaginary part of the impedance at 48GHz for

B11HFC elements is approximately equal to 36.7 Ω. This obviously indicates that an exact match between the ideal elements and the technology models is impossible.

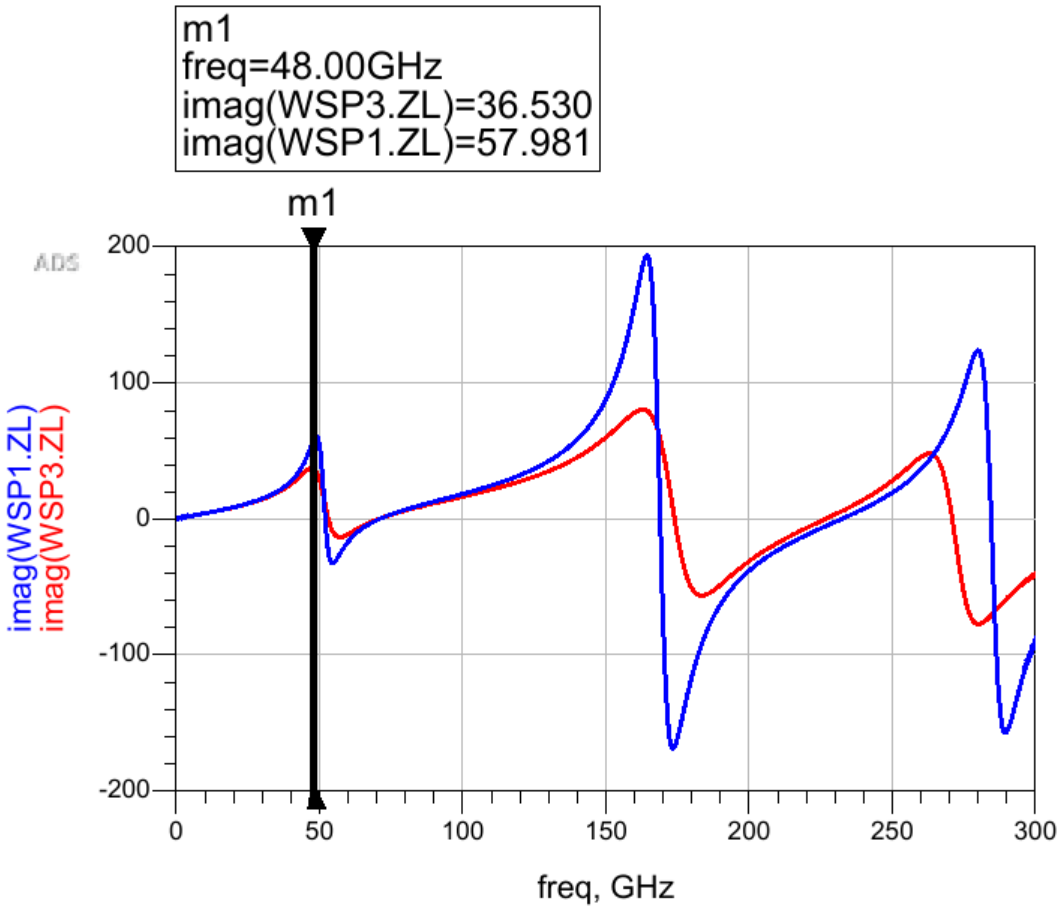

Figure 3. 47 - Mapping the imaginary part of ideals to B11HFC elements

Finally, we check by simulation the S-parameters of the network, having replaced all the elements with those of the technology models. The results of this simulation, for the four S-Parameters, are shown in Figure 3.48.

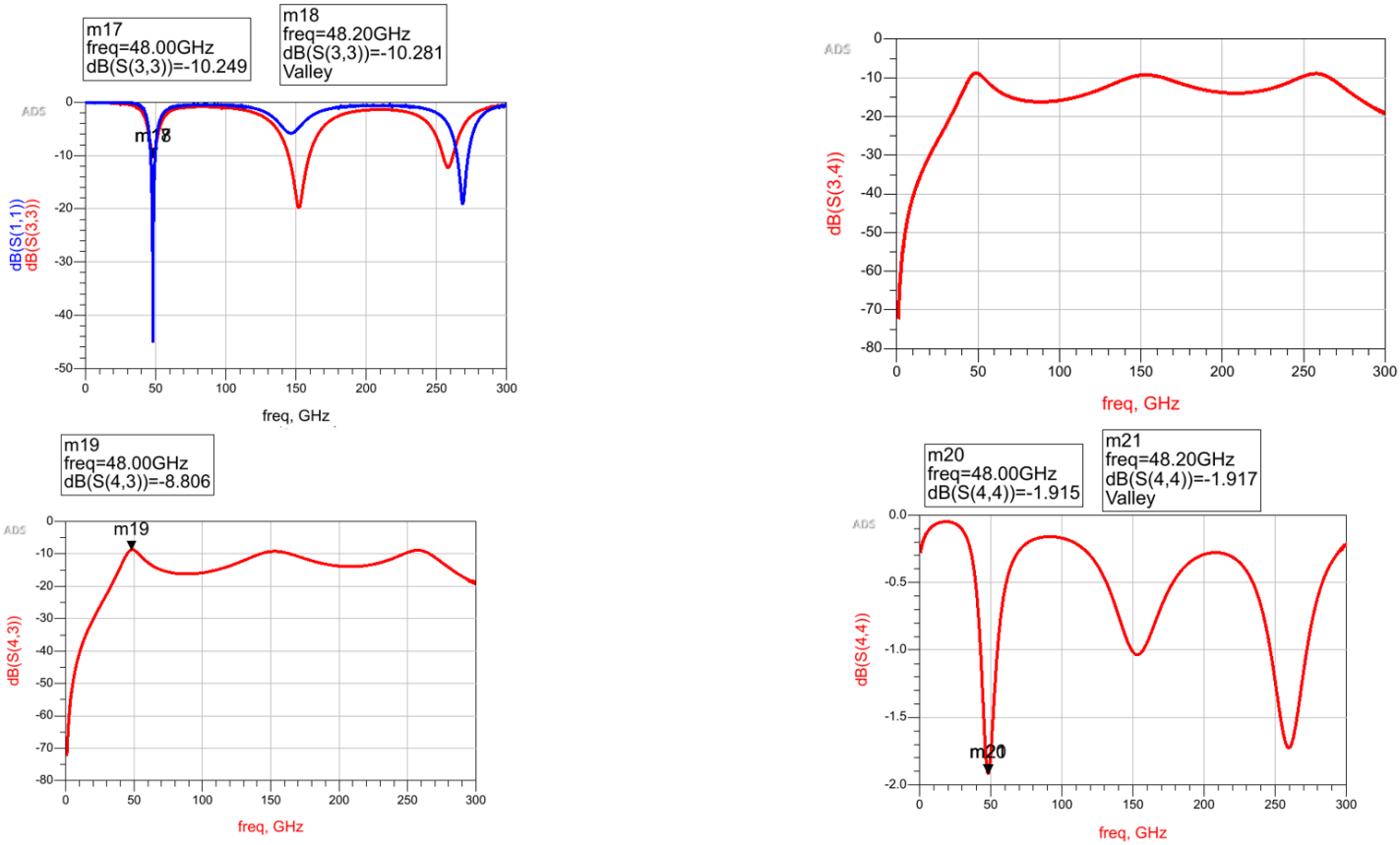

Figure 3. 48 - S-Parameters of the Tripler Block Matching Intermediate Network

3.6.4 Matching network between Tripler Block & PA Block

In the matching network between the two Blocks that make up the frequency multiplier, we seek to match the impedance loads of 13.45-j·74.56 Ω of the output of the Tripler Block and 7.2-j·3.7 Ω of the input of the Power Amplifier Block. This adjustment is done at the centered 145 GHz which is the signal at the output of the Tripler Block, i.e. the signal we want to amplify the Power Amplifier and ultimately drive it to the output of the Frequency Multiplier Block.

Finally, we synthesize the network using the Smith Chart utility of ADS. Then, using the already known procedure described previously, the ideal elements are replaced by those of the B11HFC technology. The selection of the initial length of the transmission lines, at 145 GHz which is the center frequency here, is based on equation:

$$l = \frac{50}{3} \cdot (\theta°)\ \mu m \qquad (3.7)$$

After the initial values, the required adjustments and changes to the data values, based on the simulation comparison results, lead to the final matching network, as shown below in Figure 3.49:

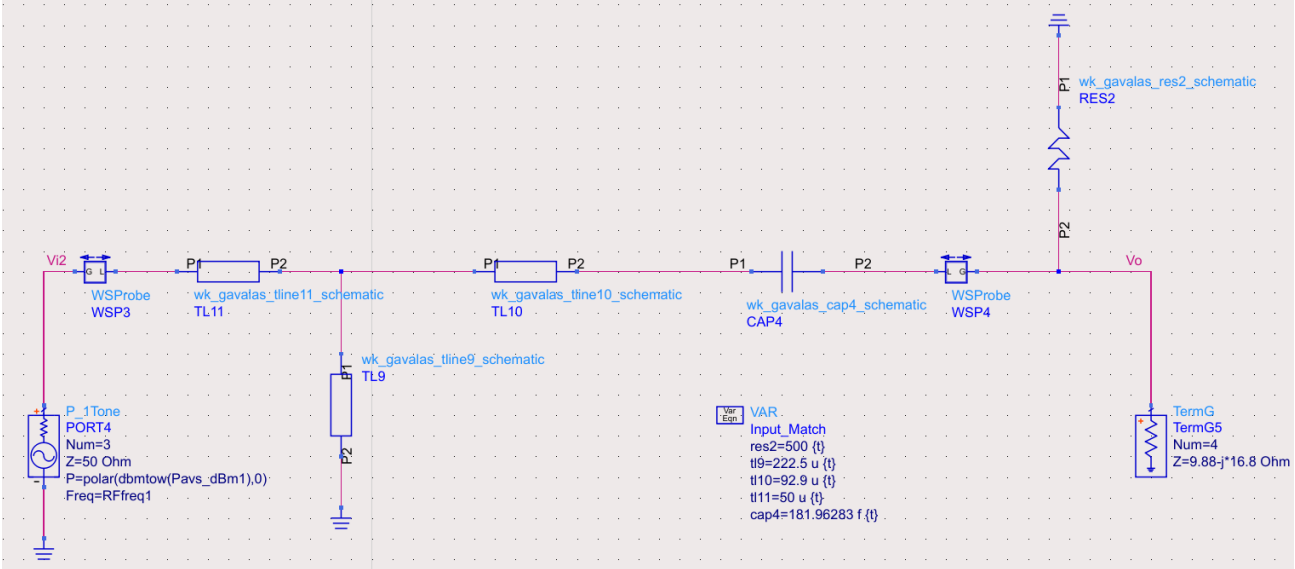

Figure 3. 49 - Adaptation network between Tripler Block & PA Block with B1HFC elements

Finally, we check by simulation the S-parameters of the network, having replaced all the elements with those of the technology models. The results of this simulation, for the four S-Parameters, are shown below, in Figure 3.50:

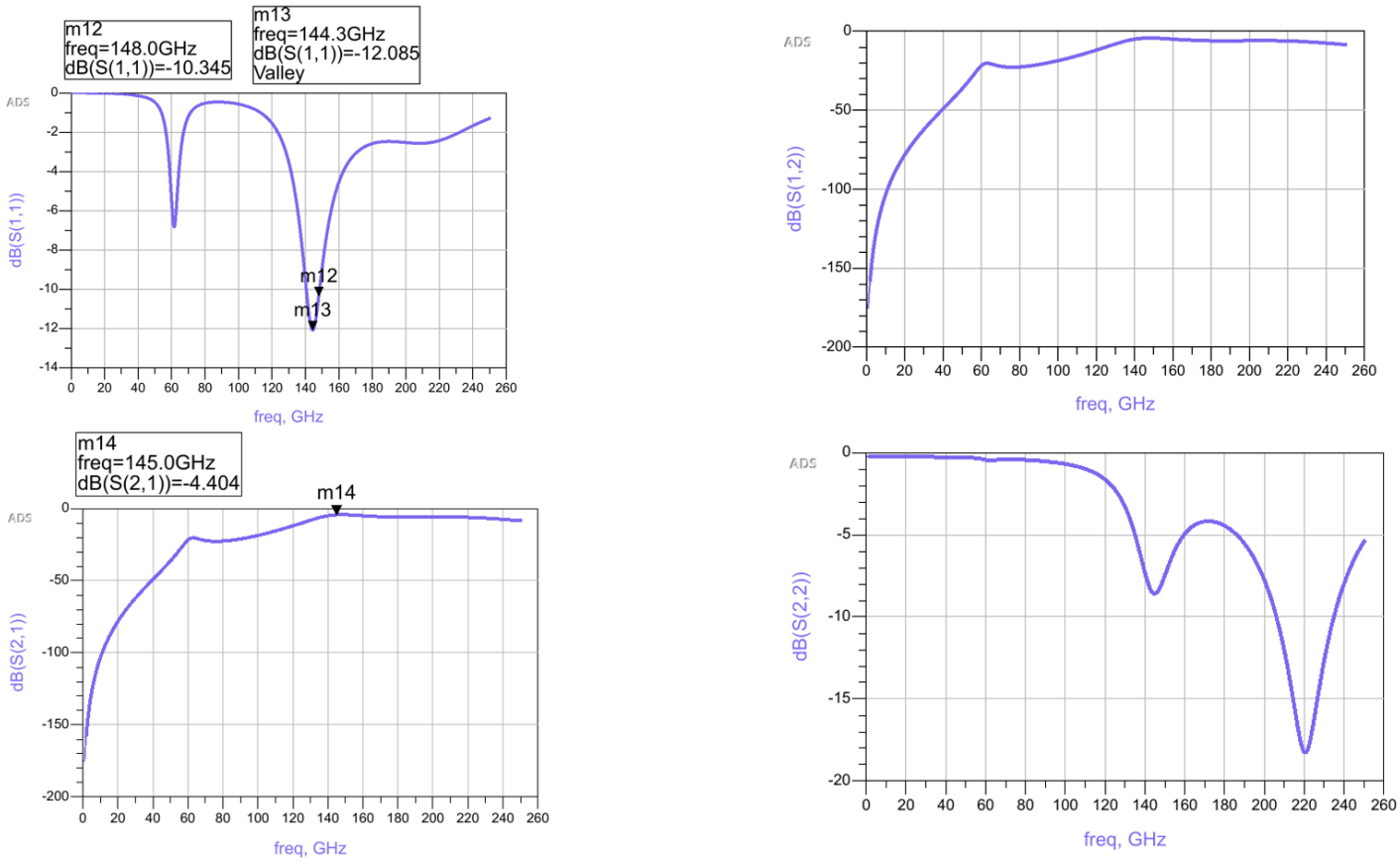

Figure 3. 50 - S-Parameters of the matching network between Tripler Block & PA Block

3.6.5 PA Block intermediate matching network

In the matching network between the first to the second as well as the second to the third active device of the Power Amplifier Block, we seek to match the impedance loads of 27.3-j·32.4 Ω of the collector of the first and second active device and 7.15-j·3.66 Ω of the base of the second and third active device of the Power Amplifier Block respectively. This adjustment is made at the centered 145 GHz, which is the signal we want the power amplifier to amplify and eventually drive to the output of the circuit.

First, we synthesize the network using the ADS Smith Chart utility and the network shown in Figure 3.51 is obtained:

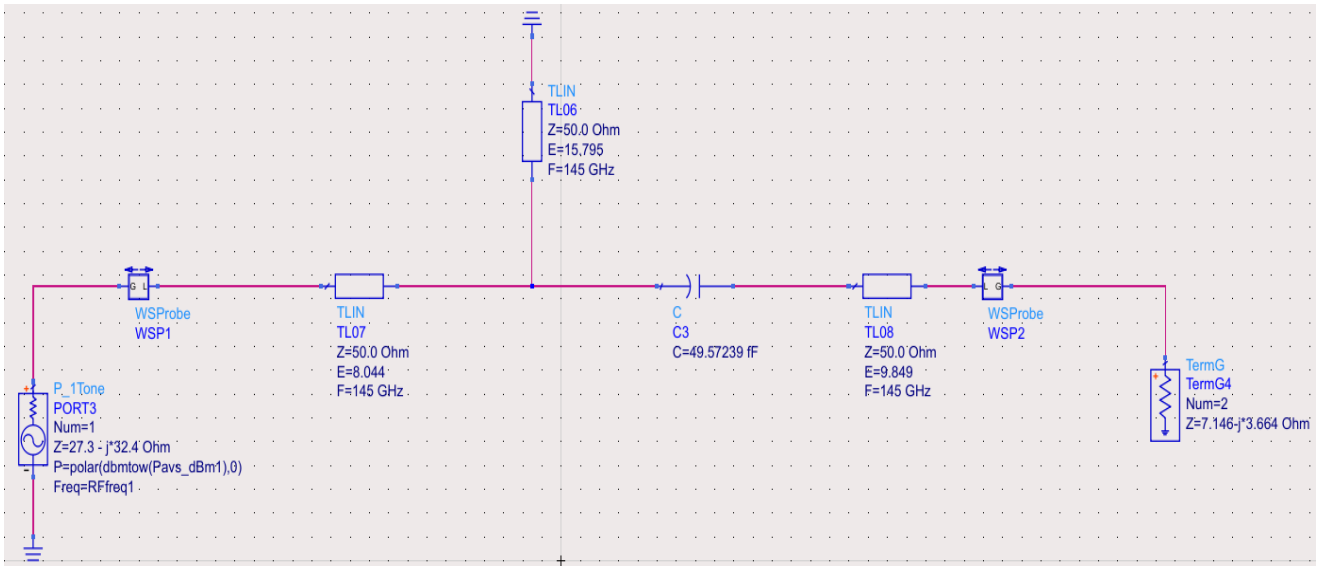

Figure 3. 51 - Power Amplifier Block Intermediate Matching Network with Ideal Elements

The ideal elements are then replaced by those of the B11HFC technology. The selection of the initial length of the transmission lines, at 145 GHz which is the center frequency here, is based on equation (3.7).

After the initial values, the required adjustments and changes in the element values, based on the comparison results through simulations, lead to the final matching network, as shown below in Figure 3.52:

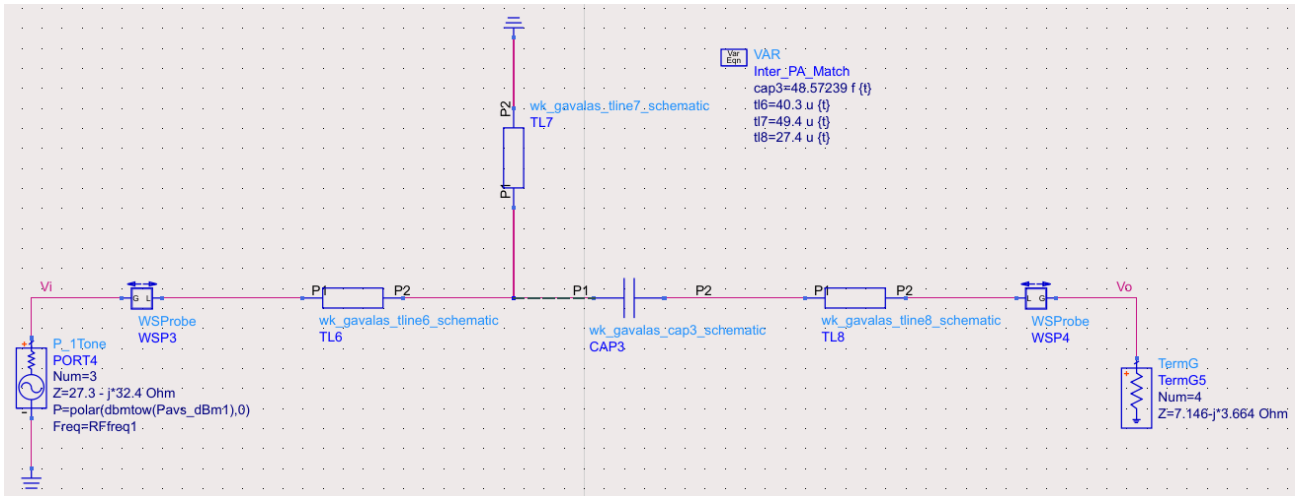

Figure 3. 52 - Intermediate Power Amplifier Block Matching Network with B1HFC components

Finally, we check by simulation the S-parameters of the network, having replaced all the elements with those of the technology models. The results of this simulation, for the four S-Parameters, are shown below, in Figure 3.53:

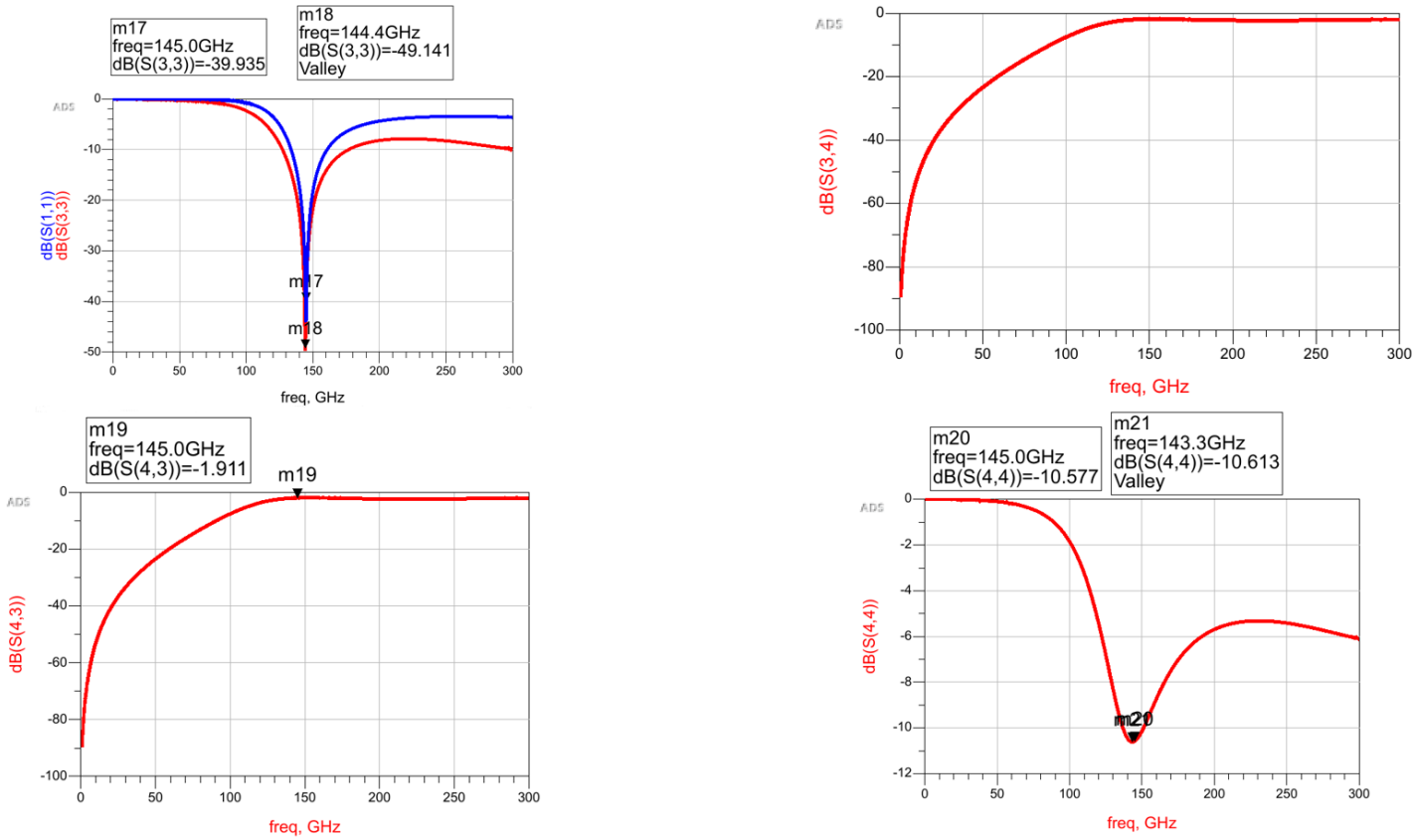

Figure 3. 53 - S-Parameters of the Power Amplifier Block Matching Intermediate Networks

3.6.6 Output matching network

In the output matching network, we seek matching between the impedance of 22-j·29.5 Ω which is the load impedance obtained from the Load Pull analysis we performed and 50+j·0 Ω which is the load at the output of the circuit. This adjustment is done at the centered 145 GHz which is the signal at the input of the frequency multiplier. Finally, the resulting network using the ADS Smith Chart utility is shown in Figure 3.54 below:

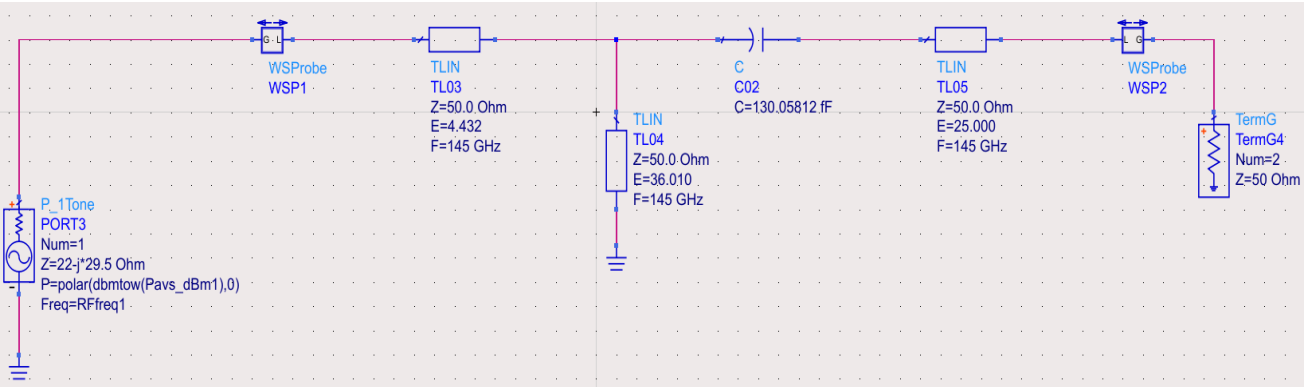

Figure 3. 54 - Output matching network with ideal elements

Next, we replace the ideal network elements with the elements of the B11HFC technology models. To select the initial length of the B11HFC transmission lines, at 145GHz which is the central input frequency, we make use of equation (3.7).

After the initial values, the required adjustments and changes to the data values, based on the simulation comparison results, lead to the final matching network for the output, as shown below in Figure 3.55:

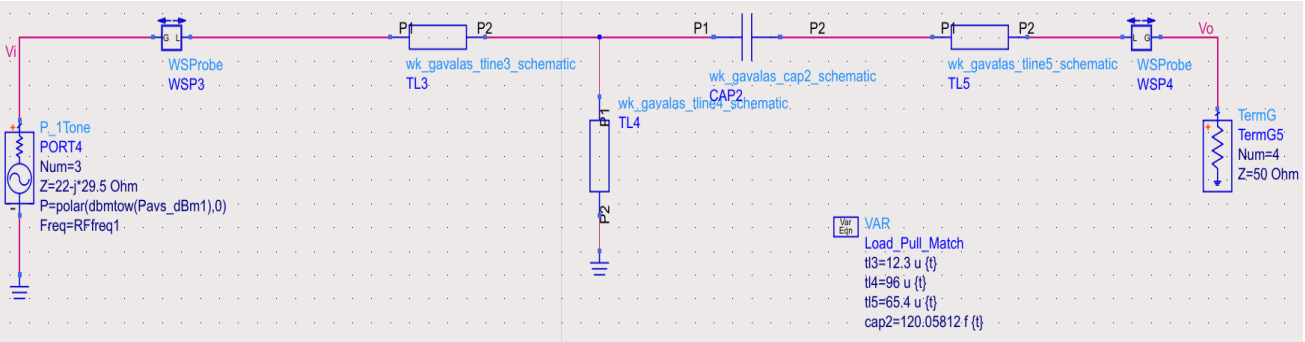

Figure 3. 55 - Output matching network with B11HFC elements

Finally, we check by simulation the S-parameters of the network, having replaced all the elements with those of the technology models. The results of this simulation, for the four S-Parameters, are shown in Figure 3.56.

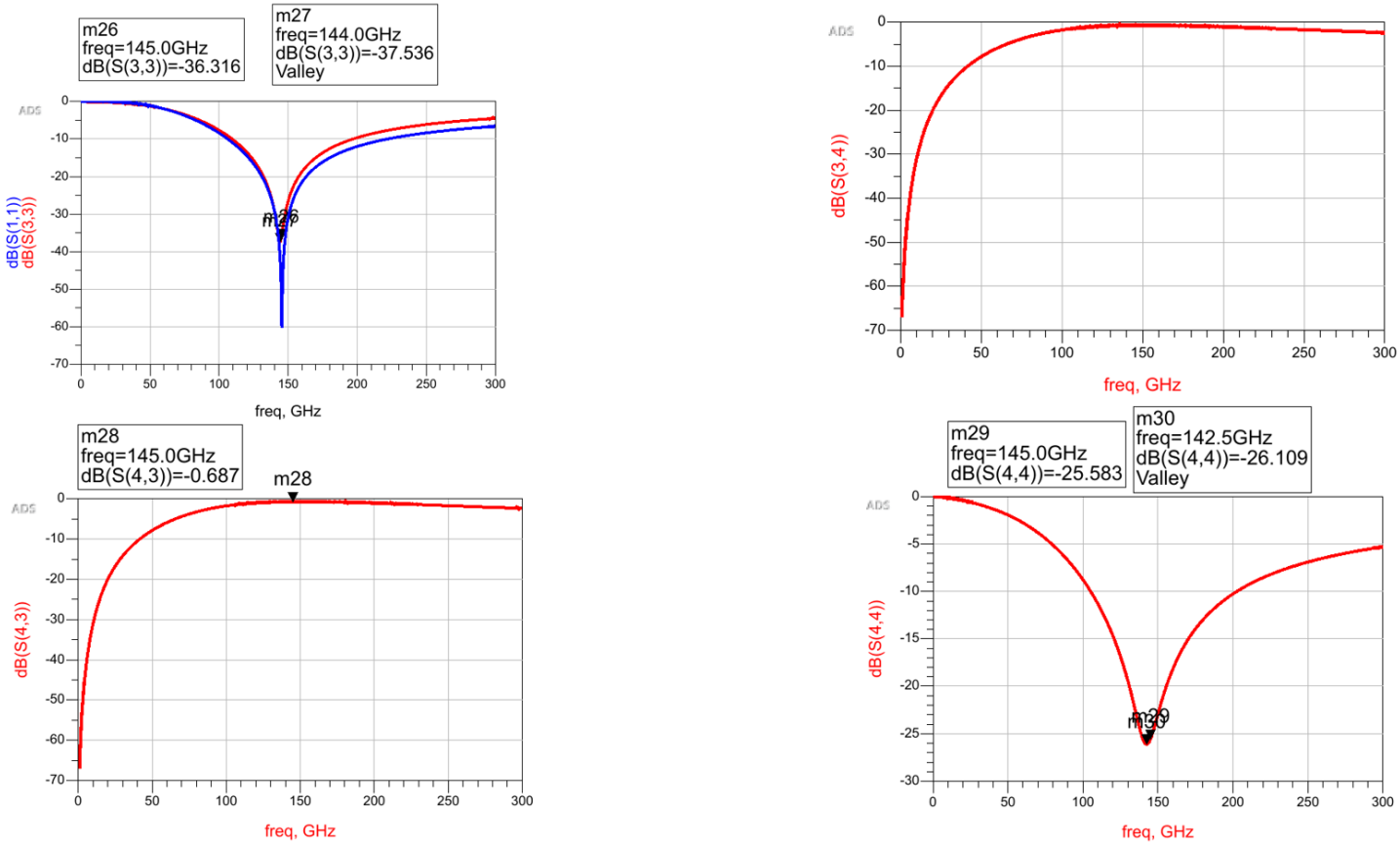

Figure 3. 56 - S-Parameters of the output matching network

3.7 Complete schematic of the frequency multiplier

With the completion of the selection of the characteristics and parameters of the active devices of the circuit and the design of all the matching networks, we arrive at the complete schematic of the circuit. Below, this is shown in Figures 3.57 and 3.58 while Table 3.3 shows the values of all the B11HFC technology components used in the design of the matching networks.

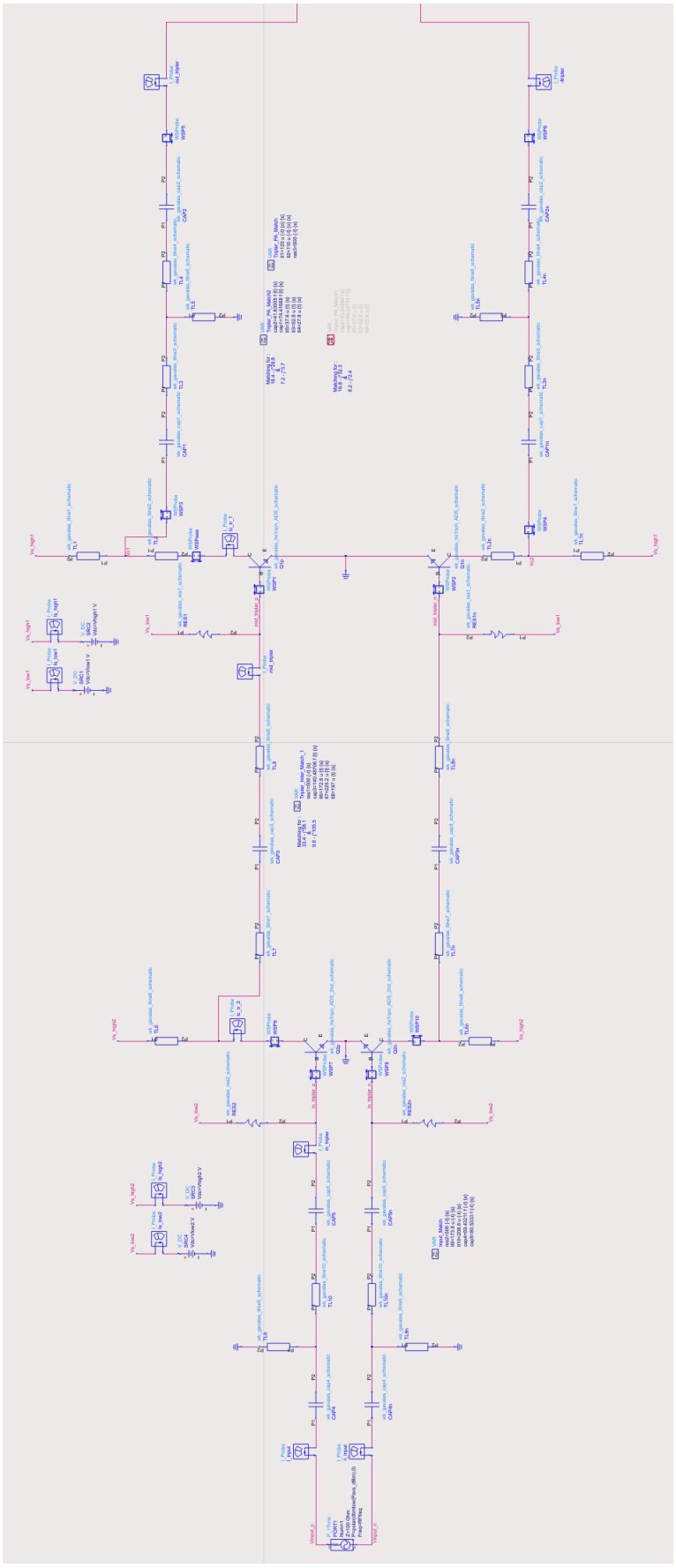

Figure 3. 57 - Complete schematic of the frequency multiplier (1)

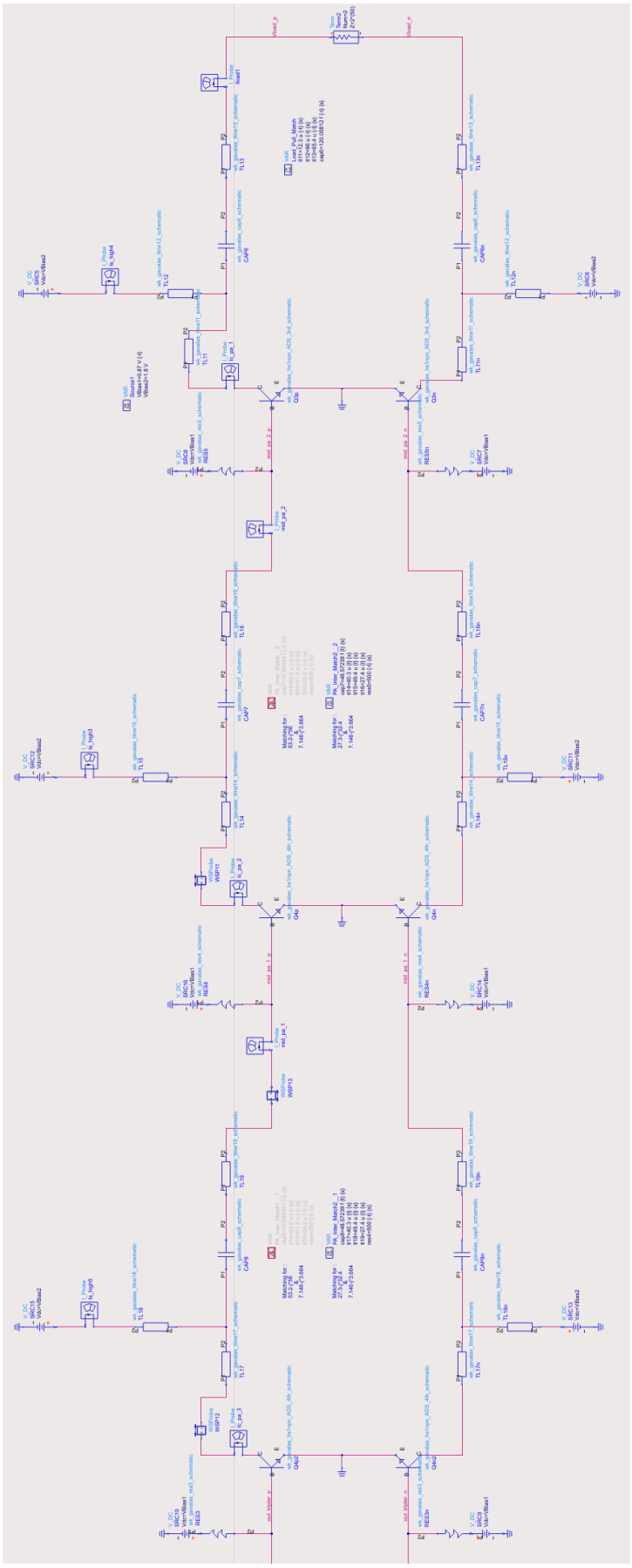

Figure 3. 58 - Complete schematic of the frequency multiplier (2)

Component Type	Name	Value
Transmission Line	tl1	120.0 µm
Transmission Line	tl2	110.0 µm
Transmission Line	tl3	27.8 µm
Transmission Line	tl4	52.8 µm
Transmission Line	tl5	37.6 µm
Transmission Line	tl6	172.8 µm
Transmission Line	tl7	225.2 µm
Transmission Line	tl8	197.9 µm
Transmission Line	tl9	173.8 µm
Transmission Line	tl10	208.8 µm
Transmission Line	tl11	12.3 µm
Transmission Line	tl12	96.0 µm
Transmission Line	tl13	65.4 µm
Transmission Line	tl14	40.3 µm
Transmission Line	tl15	49.4 µm
Transmission Line	tl16	27.4 µm
Transmission Line	tl17	40.3 µm
Transmission Line	tl18	49.4 µm
Transmission Line	tl19	27.4 µm

Capacitor	cap1	74.42 fF
Capacitor	cap2	41.63 fF
Capacitor	cap3	140.49 fF
Capacitor	cap4	69.43 fF
Capacitor	cap5	80.53 fF
Capacitor	cap6	120.06 fF
Capacitor	cap7	48.57 fF
Capacitor	cap8	48.57 fF
Resistance	res1	500.0 Ω
Resistance	res2	500.0 Ω
Resistance	res3	500.0 Ω
Resistance	res4	500.0 Ω
Resistance	res5	500.0 Ω

Table 3. 3 - B1HFC element values for the composition of the complete schematic

3.8 Complete schematic simulation results

In this section, the results of the simulations carried out at the level of a complete schematic circuit are presented. Specifically, below, in Figures 3.59 - 3.65, are the graphical representations of the four S-Parameters, the signal power at the output of the multiplier versus the signal power at the input, the power levels of the various harmonic components at the input and output of the circuit, and the first and third harmonic components of the output in the time domain.

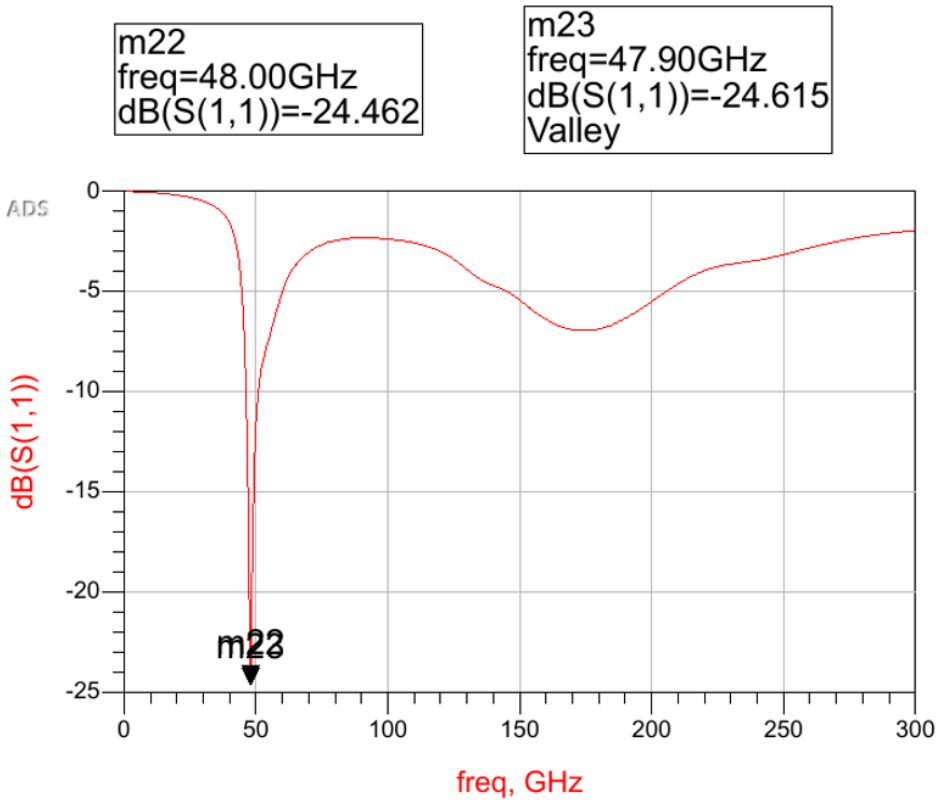

Figure 3. 59 – S_{11} Parameter at schematic level

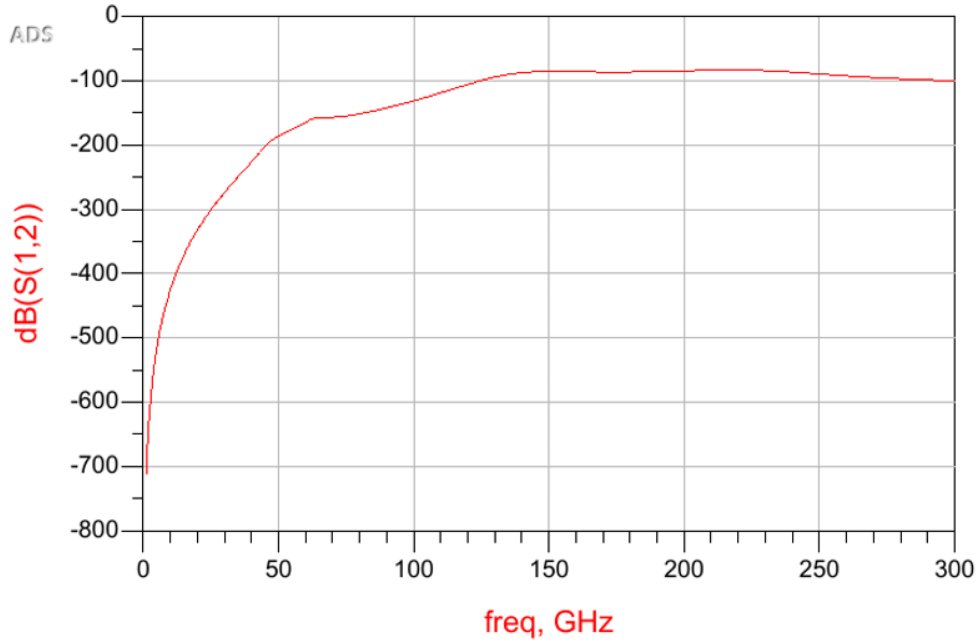

Figure 3. 60 – S_{12} Parameter at schematic level

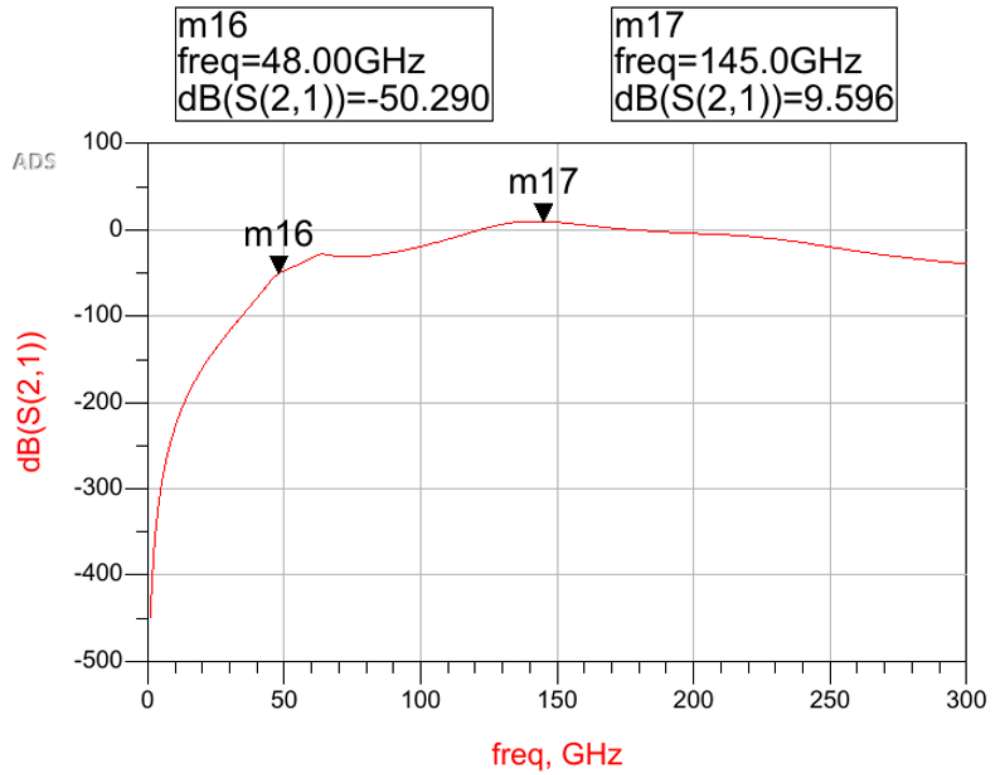

Figure 3. 61 – S_{21} Parameter at schematic level

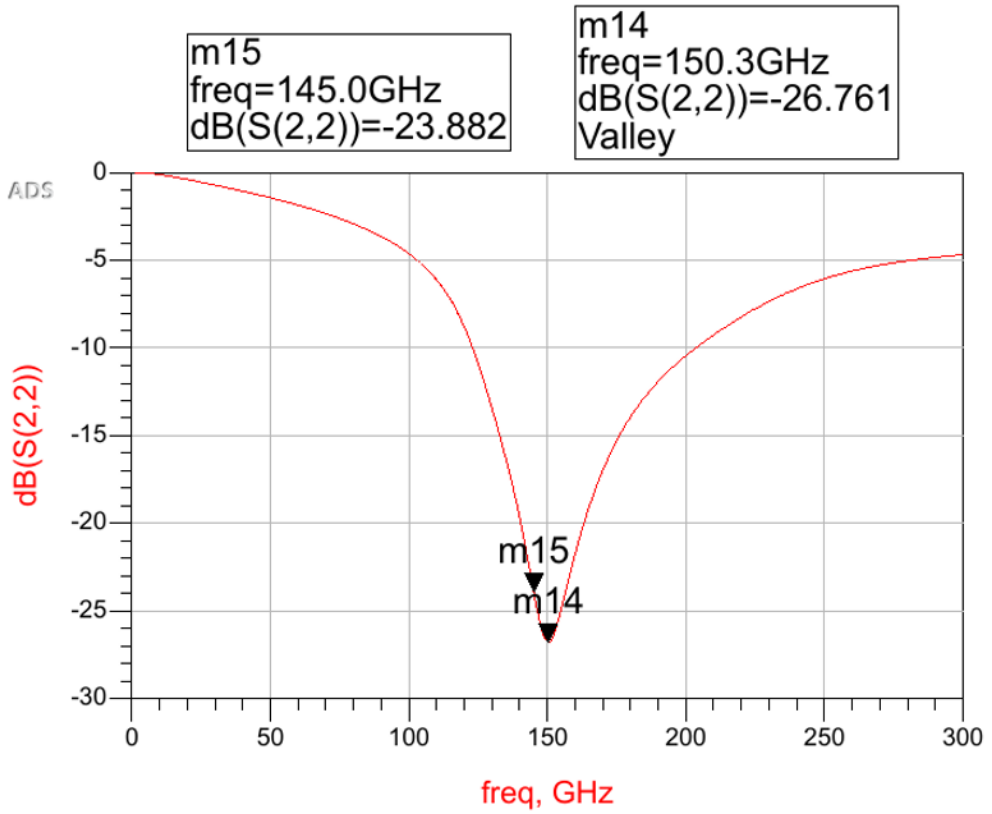

Figure 3. 62 – S_{22} Parameter at schematic level

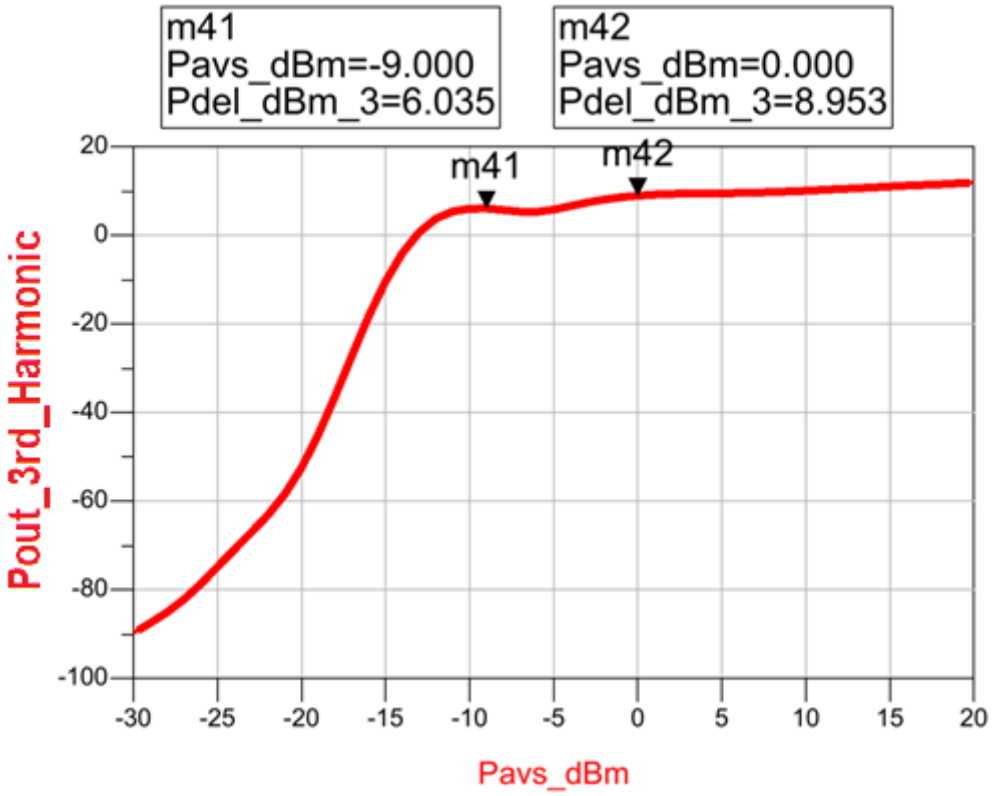

Figure 3. 63 - Output power over input power at schematic level

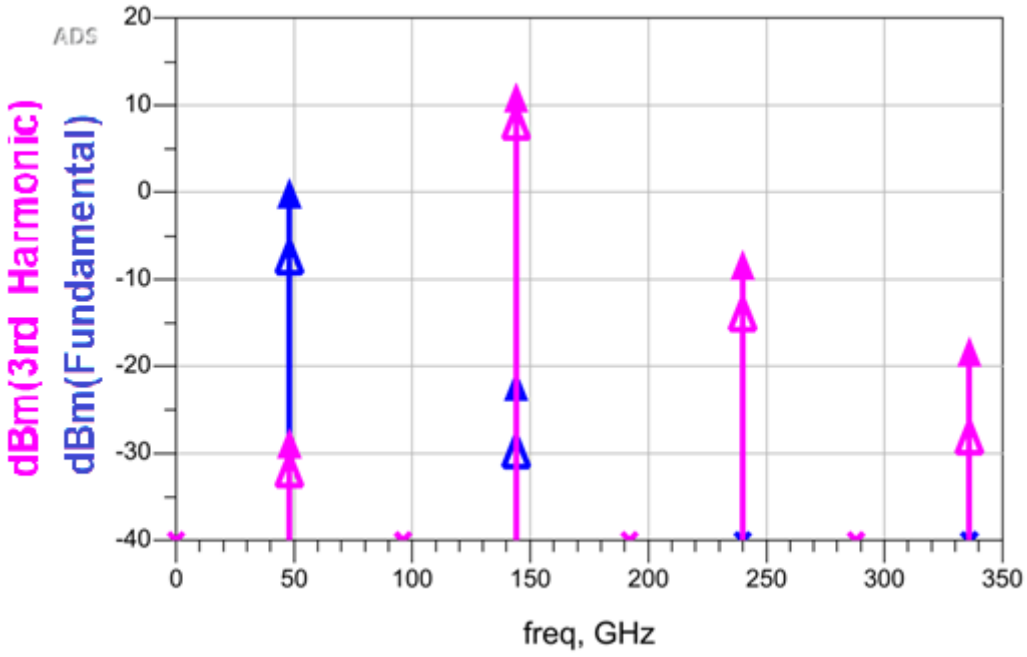

Figure 3. 64 - Power of harmonic components at input and output in schematic plane

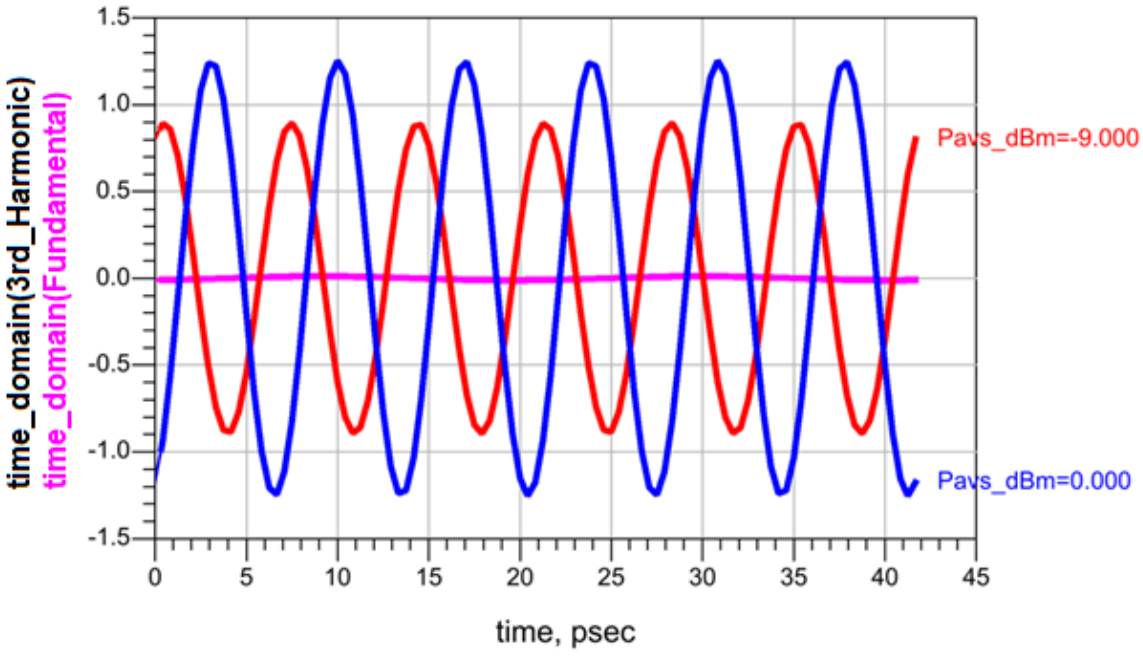

Figure 3. 65 - Power of the 1st and 3rd harmonic components at the output versus time in the schematic plane

Chapter 4 - Frequency Multiplier of class N = 3 at Layout level

This chapter describes the process of designing the frequency multiplier at the Layout level. It shows the transition of the design from the schematic level seen in the last chapter to the Layout level. Each part of the multiplier, at the Layout level, is studied separately, and the different ways of simulations to extract the parasitic elements of all passive networks are presented. At the end of the chapter, the final design with all necessary additions at Layout level is presented, which was given for implementation at the factory of Infineon Technologies AG.

4.1 General Information of the Technology

The metal stack used in the given 130nm technology is shown in Figure 4.1. The substrate is high-strength, which is desirable when it comes to RF applications. The high strength substrate will not have a significant effect on the magnetic field which flows through the top metal coating.

Figure 4. 1 - Metal stack

The technology used provides six layers of metal. The top metal is the thickest and is mainly used for designing passive elements on the chip. In addition, it is used for routing on critical paths.

4.2 QRC extraction and electromagnetic simulations

In this section, the methods used for the detailed analysis of the circuit, taking into account all parasitic effects, will be discussed, which was carried out in parallel with the layout design. These methods involve the QRC

extraction for the active devices as well as the electromagnetic simulations for the adaptation networks, which, as we have seen, are entirely composed of passive elements.

QRC extraction, or Quantus QRC Extraction Solution, is the best technology for extracting and analyzing parasitic data for analog, digital and AMS SoCs using current node technologies. The main purpose of parasitic data extraction is to create an accurate model of the circuit so that detailed simulations can mimic the actual digital and analog circuit responses. To extract the parasitics, we therefore use the RC Extraction feature provided by the Cadence design program. To continue the analysis and conduct the simulations, we replace the fully ideal model of the technology with the model of the active device obtained after extracting the parasitics.

As far as the electromagnetic simulations are concerned, a tool was needed to convert the physical design data into n-ports of S-parameters, in order to be able to participate in determining the results of the schematic simulations. This conversion was done by the Momentum ADS tool, which was used for all the transmission lines, capacitors and routing metals, the elements that make up the adaptation networks that connect the active devices of the different stages to each other.

Below, for the input adaptation network, the physical design for which the electromagnetic simulation was performed and the analysis for matching it with the network composed of the elements of the B11HFC models is presented as an example. During the comparison process, any necessary corrections to the physical design and the repetition of its electromagnetic simulations were followed each time. The two fitting networks being compared, namely the B11HFC element network and the physical design network, are shown in Figures 4.2 and 4.3 respectively. Next, Figure 4.4 shows the graphical representation of the S11 parameter of both networks, in a common axis system.

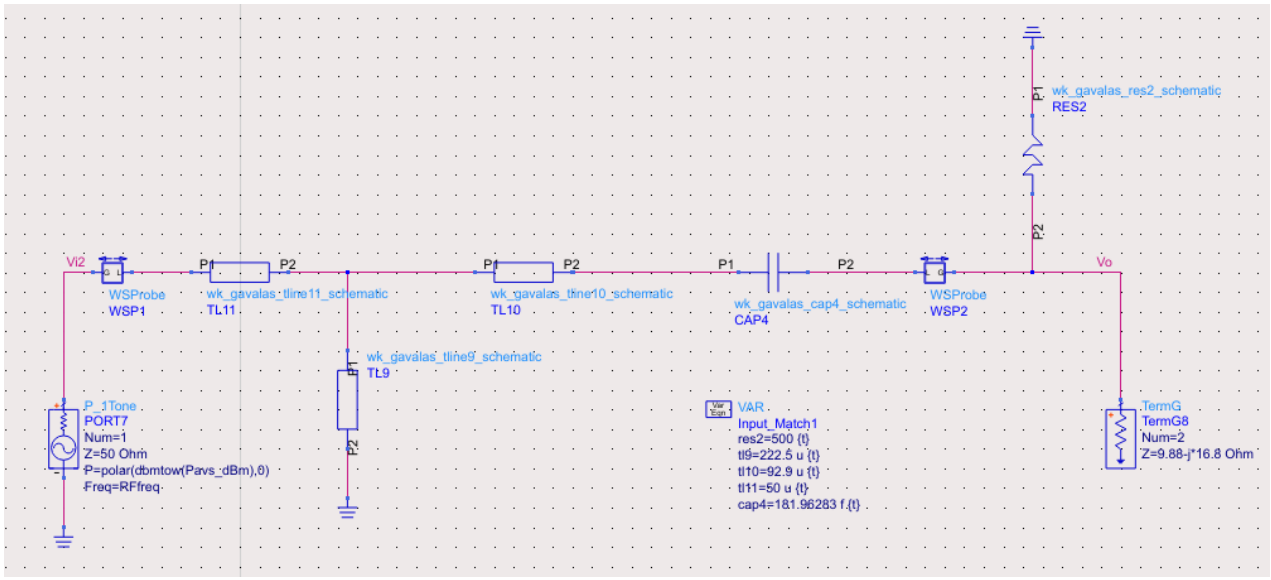

Figure 4. 2 - Input matching network with technology models

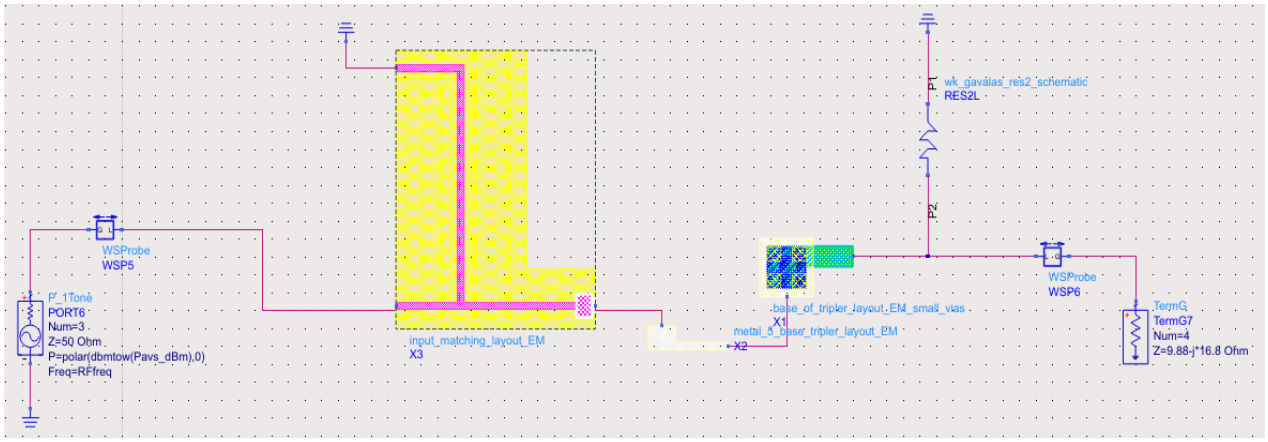

Figure 4. 3 - Input matching network in physical design

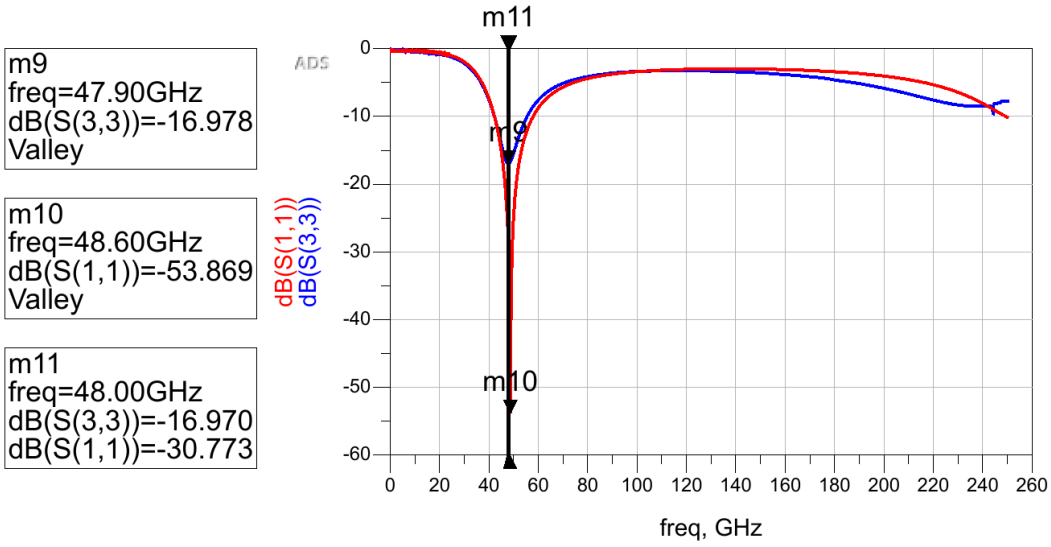

Figure 4. 4 - Parameter S_{11} of input matching networks Figures 4.2 and 4.3

In a corresponding manner, the physical design is compared and integrated for each frequency multiplier adaptation network. Figures 4.5 - 4.9 below show the correspondence of Figure 4.4 for each of the remaining matching networks.

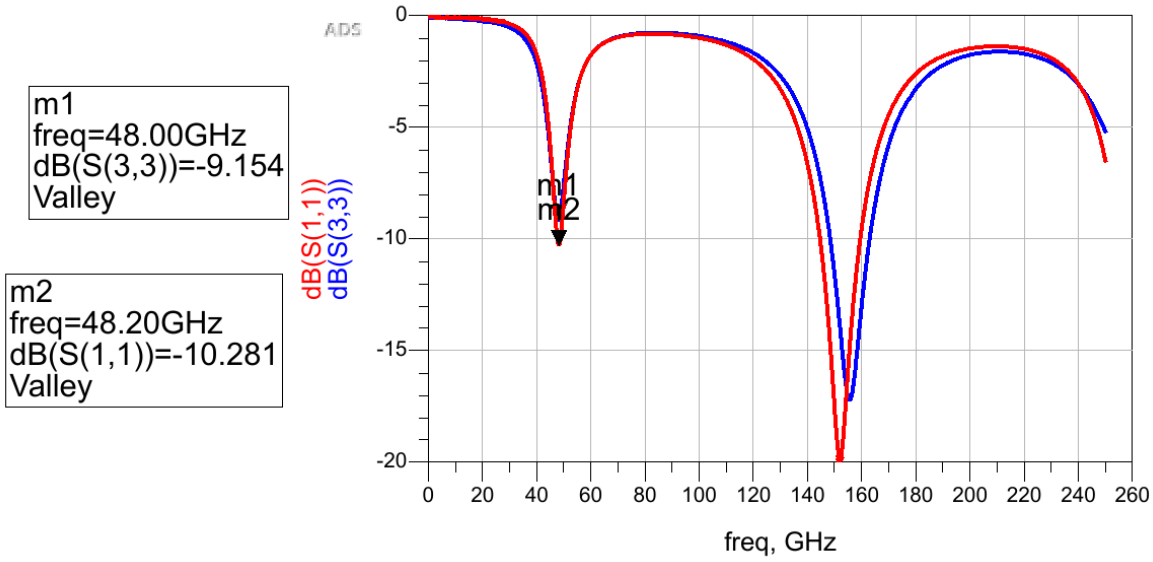

Figure 4. 5 - Comparison of parameter S_{11} of the intermediate Tripler Block matching network

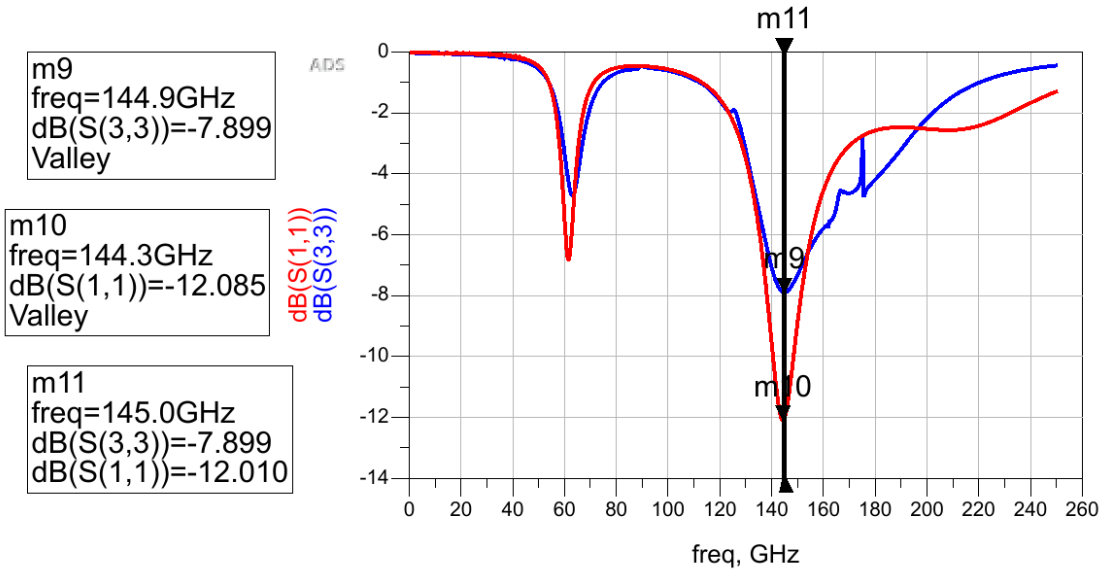

Figure 4. 6 - Comparison of S_{11} parameter of Tripler Block & PA Block matching networks

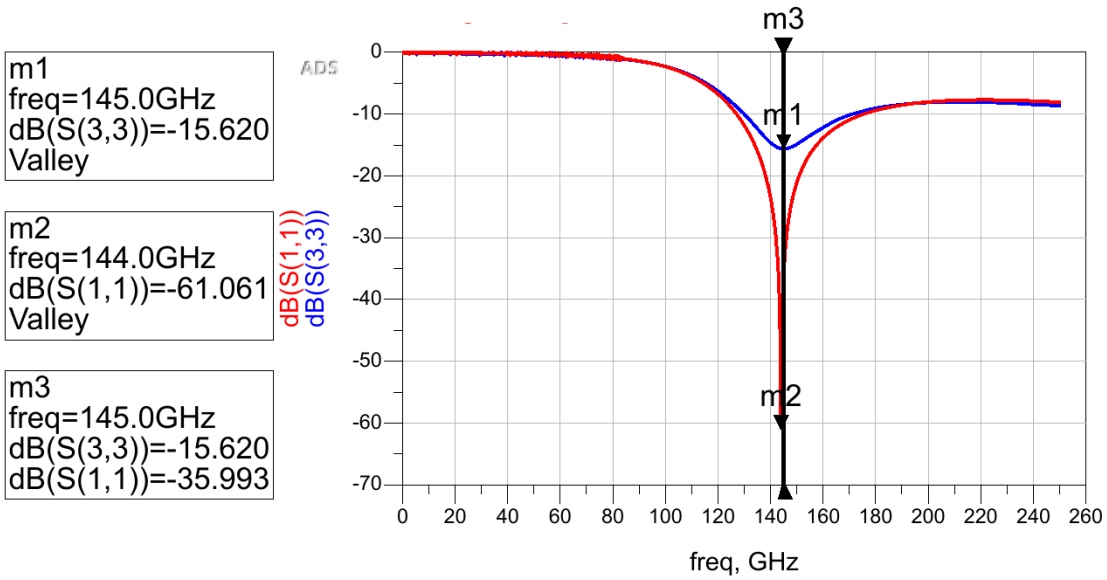

Figure 4. 7 - Comparison of parameter S_{11} of the 1st PA Block intermediate matching network

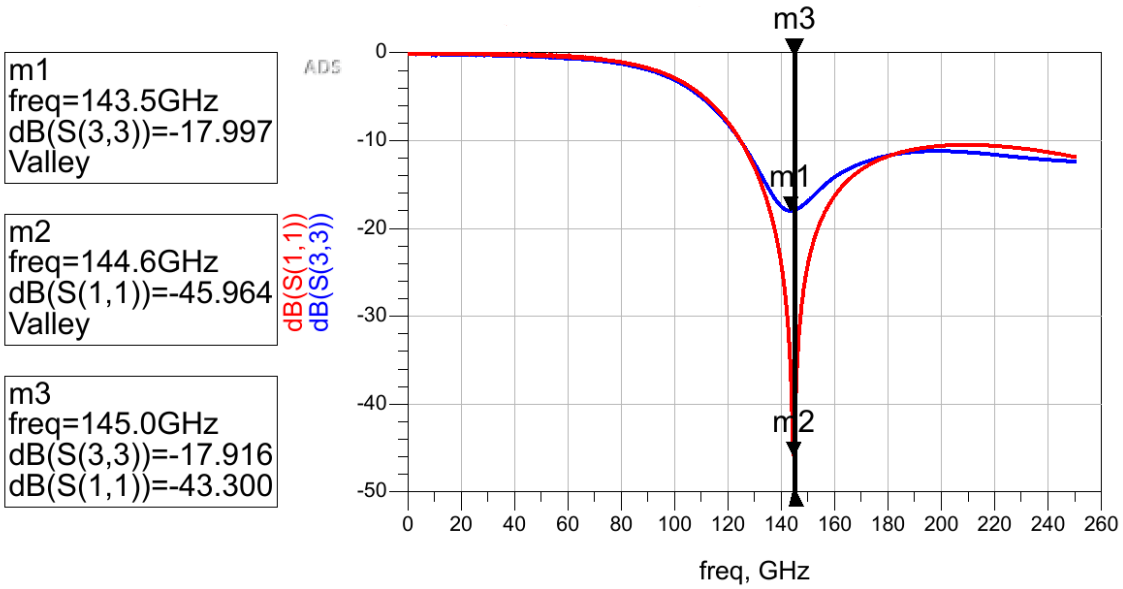

Figure 4. 8 - Comparison of parameter S_{11} of the 2nd PA Block intermediate matching network

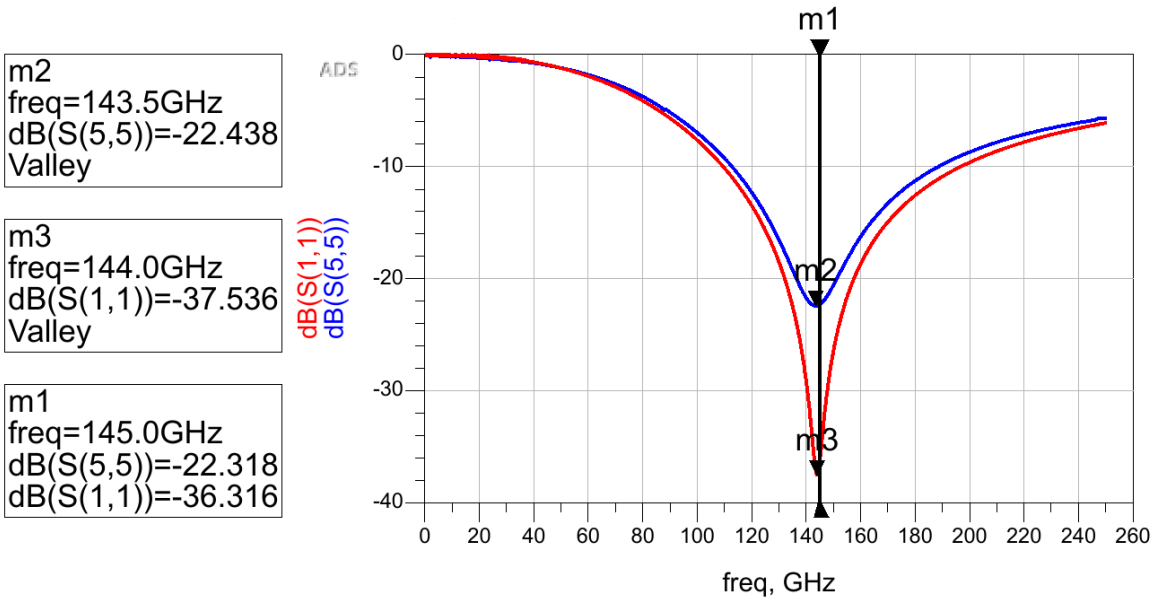

Figure 4. 9 - Comparison of the S_{11} parameter of output matching network

4.3 QRC - Layout Schematic & Final Layout

Having therefore replaced the models for each active device and having created the physical layouts for the matching networks of the circuit, based on what was discussed in the previous subsection, we obtain the schematic of Figure 4.10, consisting of the QRC extracted active devices and the Layout blocks of all matching networks, from which we obtain the final results of the simulations presented in the following section.

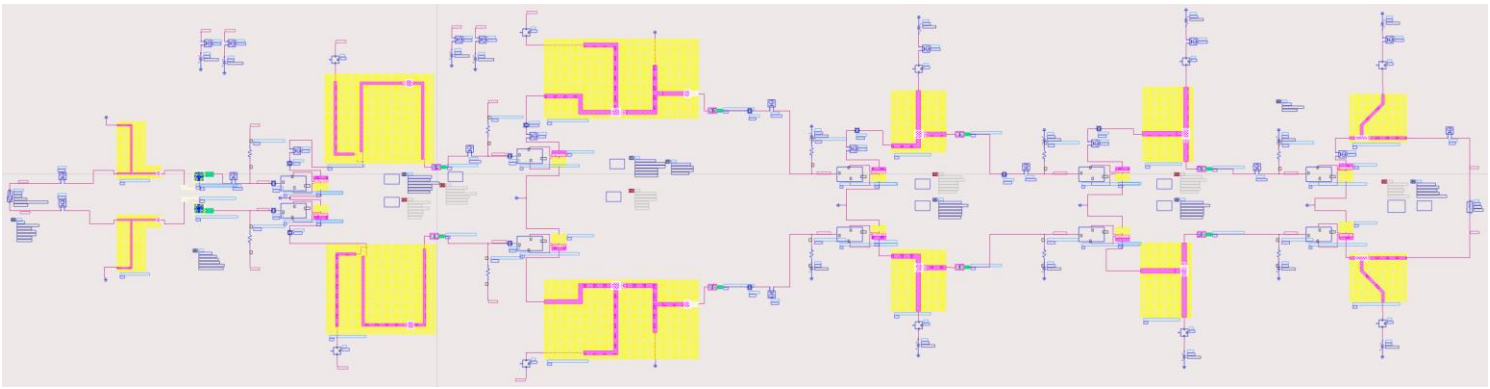

Figure 4. 10 - Final schematic with QRC extraction and Layout blocks

In addition, Figure 4.11 shows the final design of the frequency multiplier layout as delivered for implementation. With the scale of Figure 4.11,

it is not possible to see the filling and cheesing that was required in order for the design to be accepted for implementation. However, it would be reasonable to point out that in the areas of the design where no metal was present, small areas of metal were introduced so that the necessary requirements in terms of percentage of sufficiency of all metals were met for the entire test-chip surface. Similarly, we defined critical areas of M6 and M5 metals in which we wished to avoid cheesing.

In addition, as we can see from the final layout drawing, for the possibility of supply, taking measurements or even packaging a realized IC, it is necessary to introduce contact pads at all the inputs and outputs of the circuit, whether we refer to the dc power supply or to the input and output of the RF signals. By contact pads we refer to the contacts of the integrated circuit which are used to connect it to the external environment, whether this is a connection to the power supply cable, or a connection of a small bondwire cable to a previous or next integrated circuit in the chain of a system.

The contact pads used in the implementation of the frequency multiplier in this thesis are aluminum pads. Specifically, all contacts of the circuit consist of a stack of shorted metals the highest of which is aluminum. In this way, any connection of the integrated circuit to its external environment is made through the aforementioned pads, the highest metal of which is aluminum, while the lowest metal shorted to aluminum may vary depending on the function and connection of the particular contact.

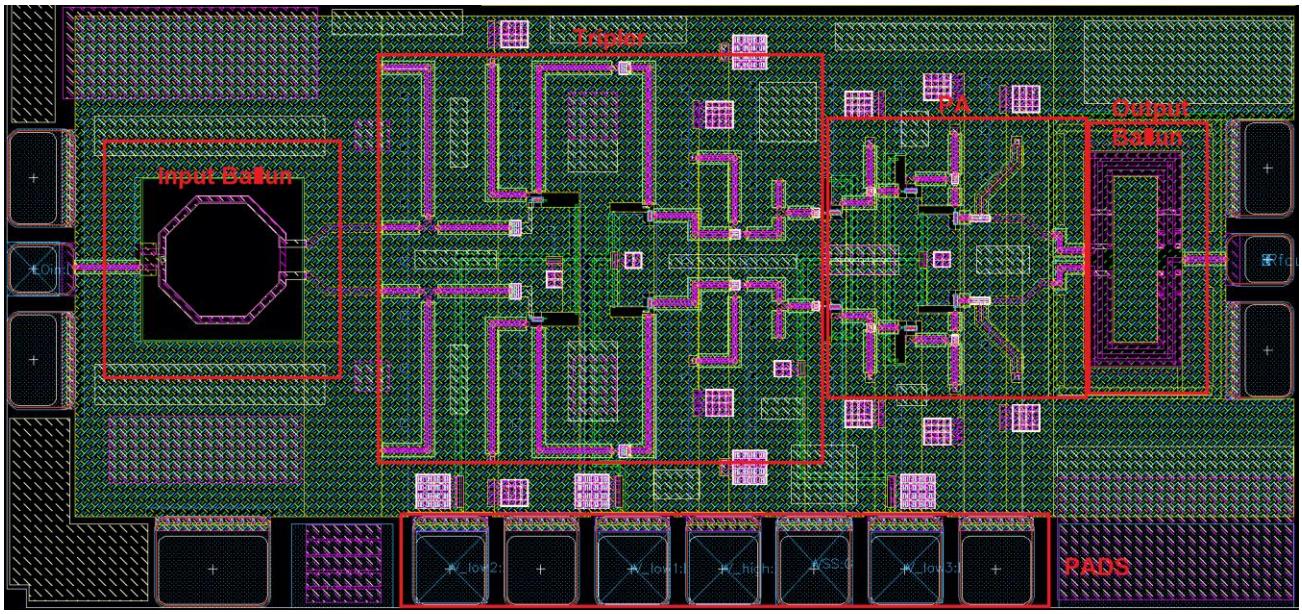

Figure 4. 11 – Complete Layout of the N=3 frequency multiplier

Finally, for both input and output, as noted in Figure 4.11, baluns are used. A balun is a transformation block between a single-ended stage and a differential pair. For the input, the aforementioned transformation is performed while for the output, the opposite is done, i.e., the transformation from the differential to the single signal. More specifically, a balun transforms a signal

from a single-ended stage to a differential pair by splitting a single signal into a pair of differential signals with the same magnitude but a phase difference of 180°. This is done at the input of our frequency multiplier as the differential input is required, while the opposite is done at the output of the PA to drive a single-ended signal to the output of the IC.

4.4 Final simulation results

In this section, the results of the simulations performed at the level of the final physical design of the frequency multiplier circuit are presented. Specifically, below, Figures 4.12 - 4.15 present the graphical representations of the four S-Parameters; Figure 4.16 shows the signal power at the output of the multiplier in relation to the signal power at the input; Figure 4.17 shows the power levels of the various harmonic components at the input and output of the circuit. Continuing, Figure 4.18 lists the first and third harmonic components of the output in the time domain. Figure 4.19 shows the current consumption of the entire circuit. This, as can be seen from the figure, comes out to be equal to 167mA, which multiplied by the supply voltage of 1.8V gives us the total power consumption, equal to 300.6mW. Finally, in Figure 4.20, we see the power of the signal at the output of the frequency multiplier over the frequency of that signal, which is three times the frequency of the input signal, from which we get the final bandwidth of our integrated circuit.

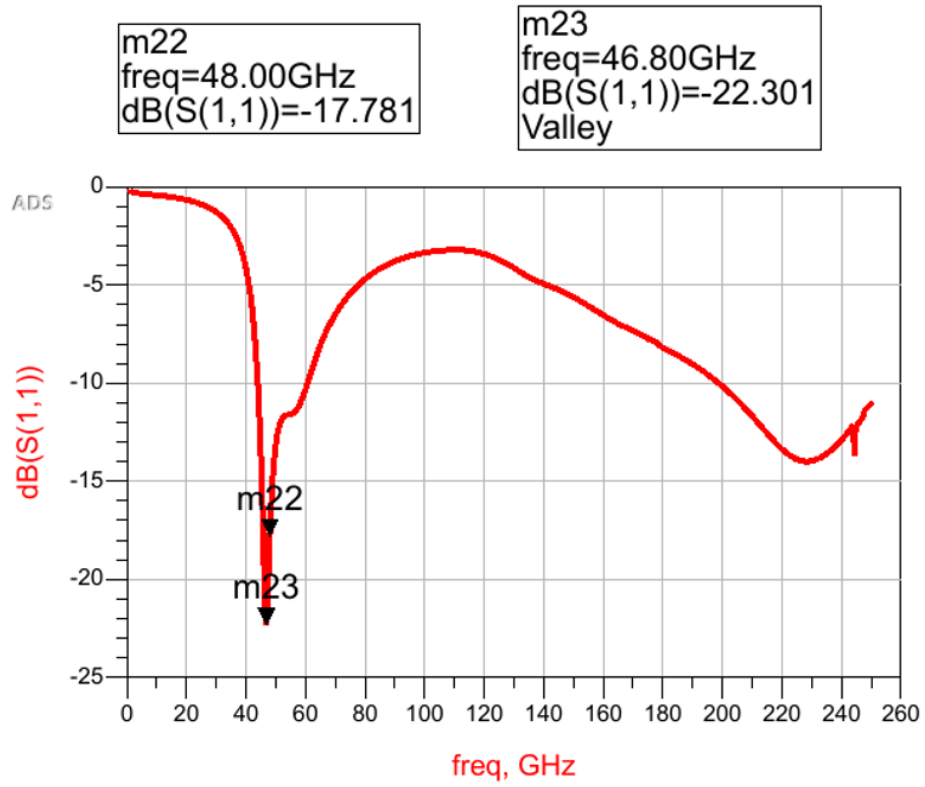

Figure 4. 12 – S_{11} final physical design parameter

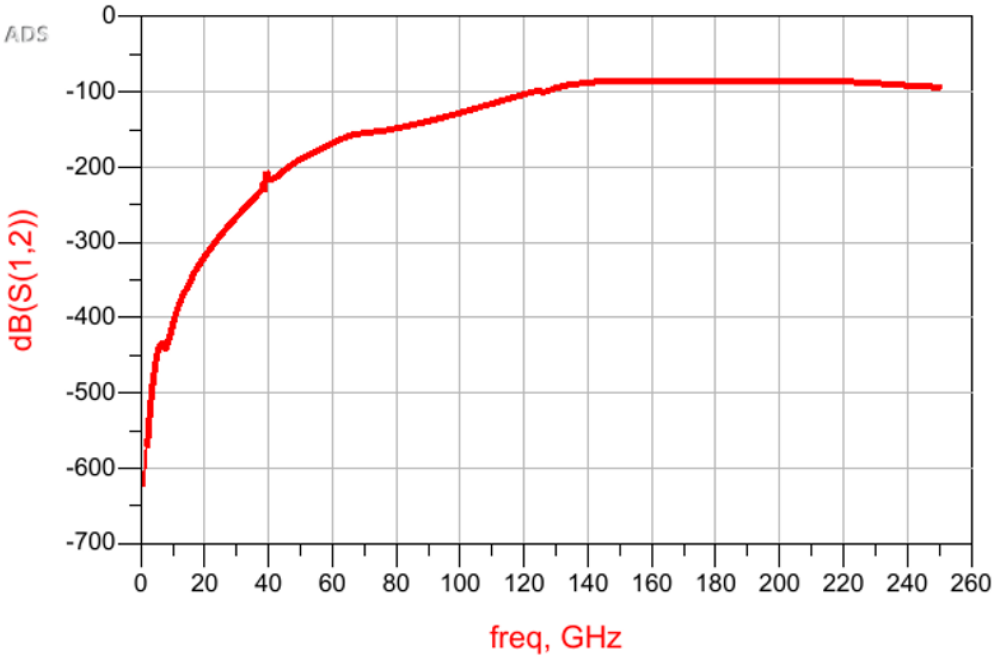

Figure 4. 13 – S_{12} final physical design parameter

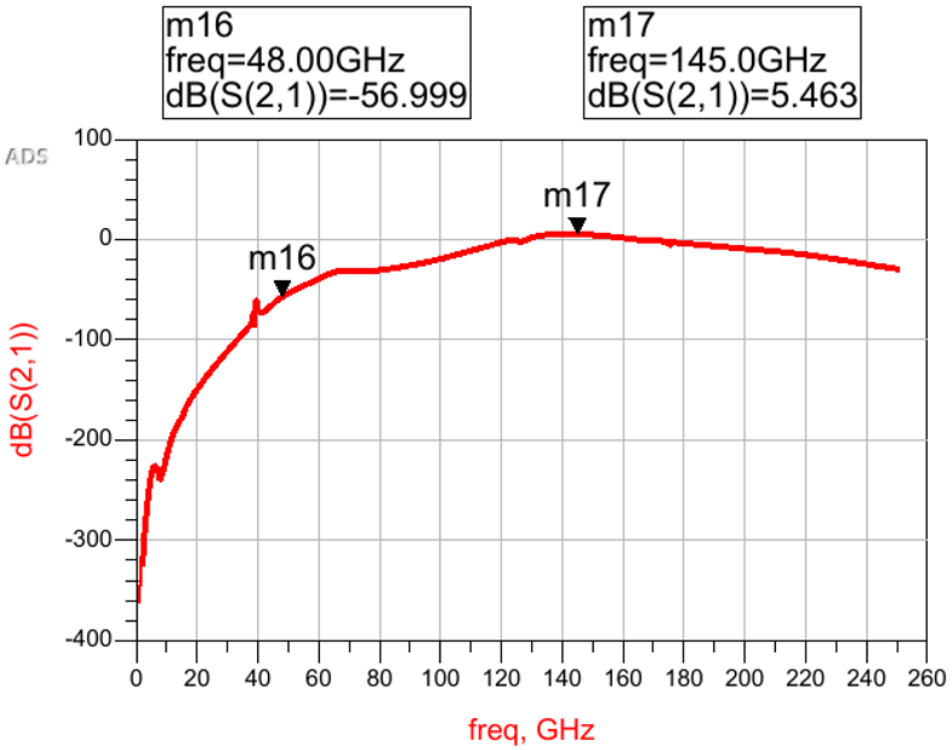

Figure 4. 14 – S_{21} final physical design parameter

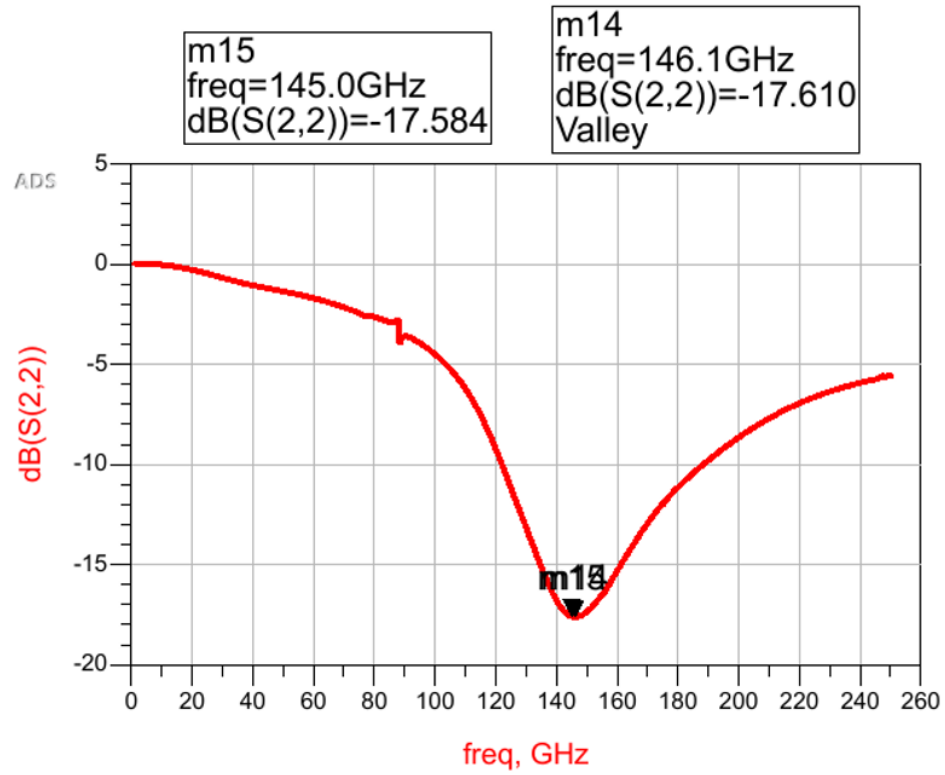

Figure 4. 15 – S_{22} final physical design parameter

For the parameter S_{11} we see that the minimum of **S_{11} = -22.30 dB** is reached at the frequency of 46.80 GHz, while at our center frequency of 46 GHz we have **S_{11} = -17.78 dB.** Similarly, for the parameter S_{22} we see that a minimum of **S_{22} = -17.61 dB** is achieved at the frequency of 146.10 GHz, while at our center frequency of 145 GHz we have that **S_{22} = -17.58 dB.** What is observed is that the dip in the S_{22} parameter is more broadband than that of the S_{11} parameter, which makes perfect sense as a 1 GHz difference in the input signal corresponds to a 3 GHz difference in the output of the frequency multiplier.

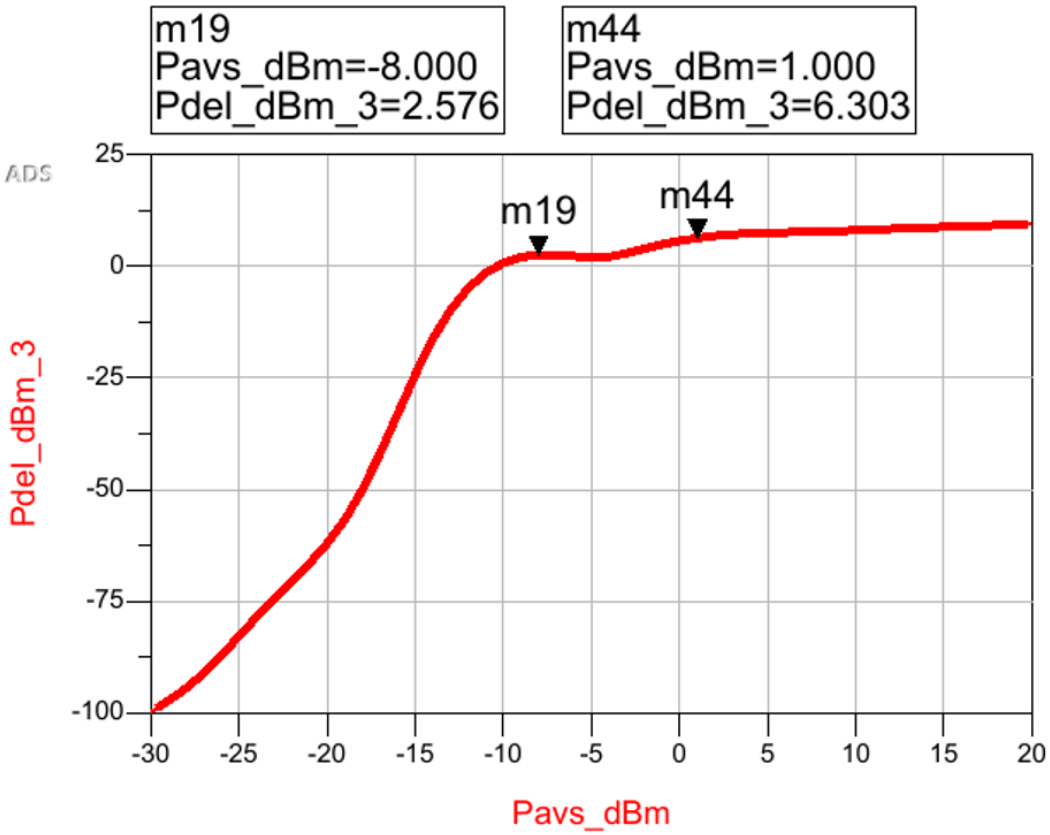

Figure 4. 16 - Output power over input power at the physical design level

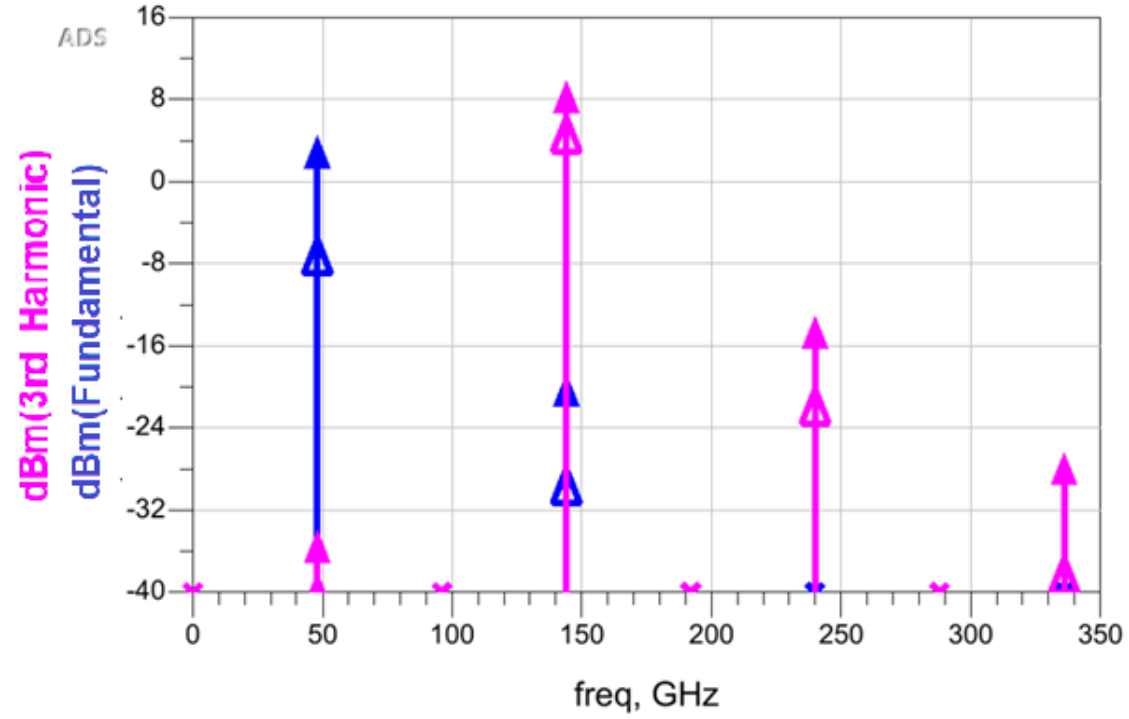

Figure 4. 17 - Power of harmonic components at the input and output at the physical design level

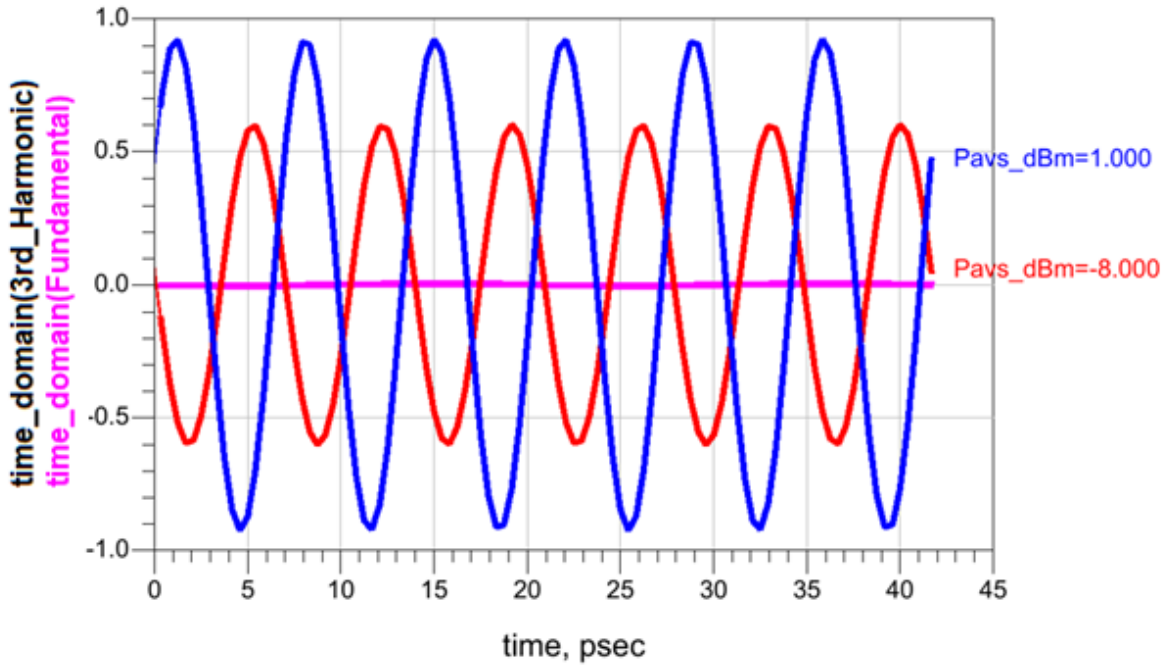

Figure 4. 18 - Power of 1st and 3rd harmonic components at the output versus time at the physical design level

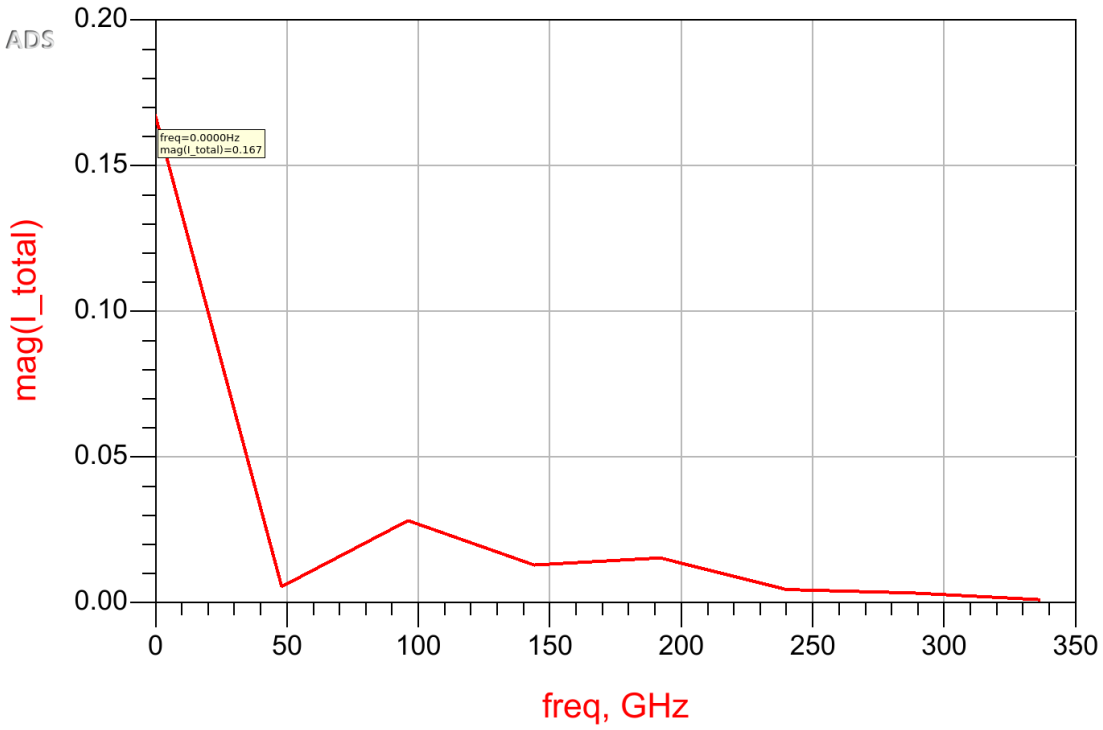

Figure 4. 19 - Current consumption of the overall circuit at the physical design level

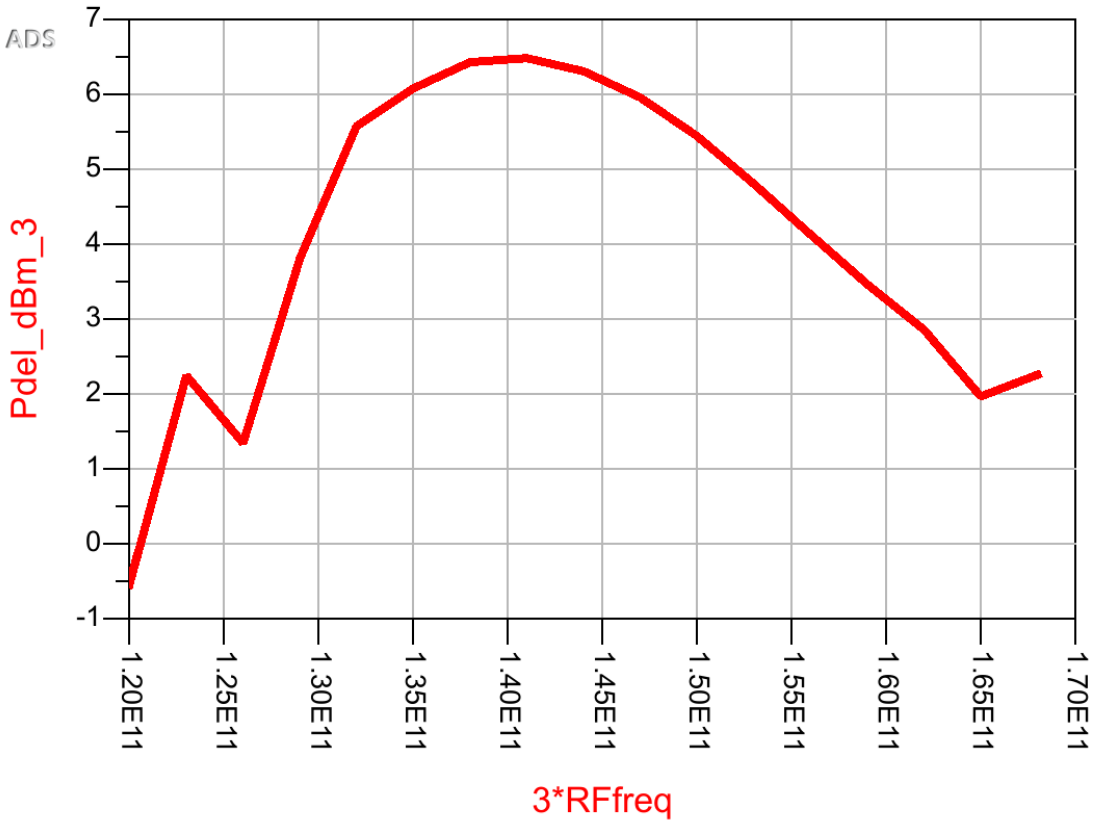

Figure 4. 20 - Power of the output signal versus its frequency

Below, in Table 6.1, we collect the results of all the simulations performed in order to get a macro view of the designed frequency multiplier of this paper. In addition, the results of the simulations performed for the circuit at the schematic level, as they were analyzed and presented in Section 3.8, are listed in the same Table. In the immediately following Table 4.2, we present a comparison of the performance of our IC with some of the corresponding frequency multipliers in the bibliography.

Specification	Goal	Result Schematic		Result Extracted	
Input Power	-	-9 dBm	0 dBm	-8 dBm	1 dBm
Central Frequency	145GHz	143.7 GHz	146 GHz	143 GHz	145 GHz
Bandwidth	130 – 160GHz	134 – 153.3 GHz	129.5 – 162.5 GHz	130.5 – 155 GHz	129 – 160 GHz
Output Power	> 0 dBm	6.0 dBm	8.9 dBm	2.5 dBm	6.3 dBm
Conversion Gain	> 0 dBm	15.0 dBm	8.9 dBm	10.5 dBm	5.3 dBm
Power dissipation	< 300mW	243.0 mW	306.0 mW	235.8 mW	300.6mW

Table 4. 1 - Collection of simulation results of the frequency multiplier at schematic and physical design level

	Out Freq. (GHz)	**Out Power** (dBm)	**Conv. Gain** (dB)	**×N**	**P_{DC}** (mW)	**Area** (mm^2)
This work	129-160	6.3	5.3	**×3**	300	0.93
[46]	129-171	2.2	5.0	**×4**	100	0.61
[43]	110-125	-3.5	-10.5	**×6**	20	0.46

[45]	121-137	-2.4	0.6	×4	35.2	0.27
[47]	109.5-146.5	4.5	0.2	×6	310	0.55

Table 4. 2 – Performance comparison table with the bibliography

After presenting the final results, it is clear that the designed frequency multiplier at the Layout level has achieved the objectives set. The achievement of these objectives indicates that the present design of this frequency multiplier is clearly competitive and very close to existing published circuits, at least at the simulation level.

Chapter 5 - Conclusions and future work

This chapter provides a brief summary of the design attempted in this paper and its main features. A brief review of the results obtained is also given. Finally, possible future extensions of the work are presented.

This thesis was carried out at Infineon Technologies AG, which provided the technology through which the design was made possible. Its purpose was the study, design and implementation of a frequency multiplier. As a central objective, operation at a central output frequency of 145 GHz, with a bandwidth ranging at plus and minus 15 GHz from the central frequency, was set as the central objective. At the same time, it is sought to drive, at the output, a high power signal, specifically at least 0 dBm, in order to generate a strong LO signal. To achieve these goals, first this circuit was implemented at the schematic level and then at the physical design level, while the necessary measurements, through simulations, were carried out throughout the design process.

As a future extension, the construction of a suitable PCB board is considered, in order to realize the desired measurements in the physical state now of the integrated circuit. With these measurements, any possible deviation of the actual measurements compared to the results of the simulations can be determined. Conclusions will also be drawn with respect to the success of the design techniques and decisions taken.

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