National Technical University of Athens
School of Electrical & Computer Engineering
Division of Communication, Electronic & Information Engineering

Distortion Estimation Methodologies and Architectures for High Linearity and Efficiency Power Amplifiers in CMOS Technologies

Ph.D. Thesis

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Μεθοδολογίες Εκτίμησης Παραμόρφωσης και Αρχιτεκτονικές Ενισχυτών Ισχύος για Υψηλή Γραμμικότητα και Απόδοση σε Τεχνολογίες CMOS

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Abstract

This thesis deals with two different topics, both of which relate to the broader aspect of the linear behavior of circuits. The first part of the thesis presents methodologies for the estimation of harmonic distortion and intermodulation distortion that are applicable to linear CMOS circuits, while the second part presents a power stage architecture characterized by high linearity and efficiency.

Harmonic and intermodulation distortion are two of the most important quantities that characterize the behavior of electronic circuits, and their estimation often proves to be a challenging task. Towards this direction, in the first thematic axis of the thesis, two systematic methods for the estimation of the aforementioned distortion types are presented. The proposed methods can be easily implemented in numerical computing environments and programming languages, are applicable to a wide variety of CMOS circuit topologies that exhibit weak nonlinear behavior, and offer high accuracy alongside with a fast computational profile. The methods rely on modeling a circuit as a structure of interconnected G_m–stages, where each one accurately captures the behavior of its corresponding circuit stage by means of an output current function dependent on its input, output voltages and cross–products of them. The distortion estimation is performed in the time–domain through two approximation steps, reducing the computational complexity and requiring only the solution of two systems of linear equations. The proposed methods are applied to various CMOS integrated circuit implementations in simulation environment, where their estimation accuracy and fast computational profile are validated.

In the second thematic axis of the thesis, a power stage architecture characterized by high linearity and high efficiency is presented. The proposed architecture combines the excellent linearity of Class–A power stages with two continuously tracking supply rails that reduce power losses on the output devices while further improving the stage's linearity. The dynamic supply rails are generated by two DC–DC converters capable of producing tracking supply voltages of frequencies up to a few tens of kHz, making the topology suitable for audio applications or low–frequency signal measurements. The theoretical analysis of the proposed power stage architecture is accompanied by a proof–of–concept integrated CMOS implementation in simulation environment, where the characteristics and advantages of the architecture are illustrated.

Keywords

Amplifier, buck–converter, Class–A, Class–CTA, Class–H, CMOS, efficiency, estimation, G_m–stage, harmonic distortion, intermodulation distortion, linear circuits, linearity, power stage, push–pull, weak nonlinearities.

Περίληψη

Η εν λόγω διατριβή καταπιάνεται με δύο διαφορετικά θέματα, τα οποία σχετίζονται αμφότερα με την ευρύτερη πτυχή της γραμμικής συμπεριφοράς κυκλωματικών διατάξεων. Το πρώτο μέρος της διατριβής αφορά στην ανάπτυξη και υλοποίηση μεθόδων εκτίμησης αρμονικής παραμόρφωσης και παραμόρφωσης ενδοδιαμόρφωσης σε γραμμικά κυκλώματα CMOS, ενώ το δεύτερο κομμάτι αφορά στην ανάπτυξη και υλοποίηση μίας αρχιτεκτονικής σταδίου ισχύος υψηλής γραμμικότητας και απόδοσης.

Η αρμονική παραμόρφωση (harmonic distortion) και η παραμόρφωση ενδοδιαμόρφωσης (intermodulation distortion) αποτελούν δύο από τα σημαντικότερα μεγέθη που χαρακτηρίζουν την συμπεριφορά ηλεκτρονικών διατάξεων, με την εκτίμησή τους πολλές φορές να αποδεικνύεται πολύπλοκο εγχείρημα. Προς αυτή την κατεύθυνση, στον πρώτο θεματικό άξονα της διατριβής παρουσιάζονται δύο συστηματικές μέθοδοι εκτίμησης των προαναφερθέντων ειδών παραμόρφωσης. Οι προτεινόμενες μέθοδοι μπορούν να υλοποιηθούν εύκολα σε αριθμητικά υπολογιστικά περιβάλλοντα και γλώσσες προγραμματισμού, εφαρμόζονται σε πληθώρα CMOS κυκλωματικών τοπολογιών που παρουσιάζουν ασθενή μη–γραμμική συμπεριφορά και προσφέρουν μεγάλη ακρίβεια εκτίμησης παράλληλα με υψηλή ταχύτητα εκτέλεσης. Οι μέθοδοι βασίζονται στην μοντελοποίηση του κυκλώματος ενδιαφέροντος ως μίας δομής διασυνδεδεμένων σταδίων διαγωγιμότητας (G_m–stages), τα οποία αποδίδουν με ακρίβεια την συμπεριφορά των αντίστοιχων τμημάτων που μοντελοποιούν μέσω μίας συνάρτησης ρεύματος εξαρτώμενης από τις τάσεις εισόδου, εξόδου και γινομένων τους. Η διαδικασία εκτίμησης της παραμόρφωσης γίνεται στο πεδίο του χρόνου μέσω δύο προσεγγιστικών βημάτων, όπου μειώνεται η υπολογιστική πολυπλοκότητα και απαιτείται απλά η επίλυση δύο συστημάτων γραμμικών εξισώσεων. Οι προτεινόμενες μέθοδοι εφαρμόζονται σε διάφορες διατάξεις ολοκληρωμένων κυκλωμάτων CMOS σε περιβάλλον προσομοίωσης, όπου επιβεβαιώνεται η ακρίβεια και ταχύτητά τους.

Στον δεύτερο θεματικό άξονα της διατριβής παρουσιάζεται μία αρχιτεκτονική σταδίου ισχύος η οποία χαρακτηρίζεται από υψηλή γραμμικότητα και ταυτόχρονα υψηλή απόδοση. Η προτεινόμενη αρχιτεκτονική συνδυάζει την άριστη γραμμικότητα των σταδίων ισχύος τάξης–A (Class–A power stages) με ένα σύστημα συνεχούς

δυναμικής τροφοδοσίας για μείωση των απωλειών ισχύος στα τρανζίστορ εξόδου και επιπρόσθετη βελτίωση της συνολικής γραμμικότητας. Το σύστημα δυναμικής τροφοδοσίας αποτελείται από δύο DC–DC μετατροπείς (DC–DC converters) ικανών να παράξουν τάσεις τροφοδοσίας συχνοτήτων έως μερικές δεκάδες kHz, με στόχο την χρήση της τοπολογίας σε εφαρμογές αναπαραγωγής ήχου (audio) ή μετρήσεων χαμηλόσυχνων σημάτων. Η θεωρητική ανάλυση της προτεινόμενης αρχιτεκτονικής σταδίου ισχύος ακολουθείται από μία proof–of–concept υλοποίησή της σε τεχνολογία ολοκληρωμένων κυκλωμάτων CMOS σε περιβάλλον προσομοίωσης, όπου αναδεικνύονται τα χαρακτηριστικά και πλεονεκτήματα της αρχιτεκτονικής.

Λέξεις–Κλειδιά

Amplifier, buck–converter, Class–A, Class–CTA, Class–H, CMOS, efficiency, estimation, G_m–stage, harmonic distortion, intermodulation distortion, linear circuits, linearity, power stage, push–pull, weak nonlinearities.

Εκτεταμένη Περίληψη

Η εν λόγω διατριβή καταπιάνεται με δύο διαφορετικά θέματα, τα οποία σχετίζονται αμφότερα με την ευρύτερη πτυχή της γραμμικής συμπεριφοράς κυκλωματικών διατάξεων. Το πρώτο μέρος της διατριβής αφορά στην ανάπτυξη και υλοποίηση μεθόδων εκτίμησης αρμονικής παραμόρφωσης και παραμόρφωσης ενδοδιαμόρφωσης σε γραμμικά κυκλώματα CMOS που χαρακτηρίζονται από ασθενή μη–γραμμική συμπεριφορά, ενώ το δεύτερο κομμάτι αφορά στην ανάπτυξη και υλοποίηση μίας αρχιτεκτονικής σταδίου ισχύος υψηλής γραμμικότητας και απόδοσης.

Μέρος Ι: Μεθοδολογίες Εκτίμησης Αρμονικής Παραμόρφωσης και Παραμόρφωσης Ενδοδιαμόρφωσης για Γραμμικά Κυκλώματα CMOS

Η αρμονική παραμόρφωση (harmonic distortion) και η παραμόρφωση ενδοδιαμόρφωσης (intermodulation distortion) αποτελούν δύο από τα σημαντικότερα μεγέθη που χαρακτηρίζουν την συμπεριφορά ηλεκτρονικών διατάξεων, με την εκτίμησή τους πολλές φορές να αποδεικνύεται πολύπλοκο εγχείρημα. Συνήθως, η εκτίμηση της παραμόρφωσης γίνεται μέσω προσομοίωσης, όπου χρησιμοποιούνται μέθοδοι όπως η harmonic balance και το shooting. Η διαδικασία μπορεί να είναι αρκετά χρονοβόρα μιας και τέτοιες μέθοδοι είναι επαναληπτικές, ειδικά για πυκνό εύρος συχνοτήτων, ενώ ο χρήστης δεν είναι βέβαιο ότι αποκομίζει βαθύτερη γνώση των αιτίων της συμπεριφοράς του κυκλώματος.

Για τον λόγο αυτό, έχει υπάρξει δραστηριότητα προς την δημιουργία αφοσιωμένων μεθόδων εκτίμησης των ειδών παραμόρφωσης. Η πιο δημοφιλής επιλογή είναι η χρήση σειρών Volterra, όπου τα αποτελέσματα χαρακτηρίζονται από πολύ υψηλή ακρίβεια. Το μειονέκτημα που παρουσιάζουν οι σειρές Volterra είναι η αυξημένη πολυπλοκότητα: καθώς αυξάνεται ο αριθμός των στοιχείων του κυκλώματος προς διερεύνηση, ο αριθμός των απαιτούμενων όρων για τον υπολογισμό γίνεται μη διαχειρίσιμος. Εκτός των σειρών Volterra έχουν αναπτυχθεί διάφορες άλλες μέθοδοι εκτίμησης παραμόρφωσης, με βασικό στόχο την μεγαλύτερη απλότητα και ευκολία χρήσης τους. Ωστόσο, τις περισσότερες φορές μπορούν να εφαρμοστούν μόνο σε συγκεκριμένες (και δημοφιλείς) τοπολογίες, ενώ παράλληλα μπορεί να παρουσιάσουν σημαντικές αποκλίσεις από την πραγματικότητα.

Οι προτεινόμενες μέθοδοι εκτίμησης αρμονικής παραμόρφωσης και παραμόρφωσης ενδοδιαμόρφωσης της διατριβής έχουν γενικό χαρακτήρα και συστηματική, κλειστή μορφή. Μπορούν να εφαρμοστούν σε μεγάλη πληθώρα κυκλωμάτων που παρουσιάζουν ασθενή μη–γραμμική συμπεριφορά, με αόριστο αριθμό σταδίων, και χαρακτηρίζονται από υψηλή ακρίβεια εκτίμησης και μικρό χρόνο εκτέλεσης. Ως εκ τούτου, θα μπορούσαν να ενσωματωθούν σε προγράμματα προσομοίωσης κυκλωμάτων ως ρουτίνες εκτίμησης των δύο ειδών παραμόρφωσης για να επιταχύνουν την ροή σχεδίασης.

Οι μέθοδοι βασίζονται στην μοντελοποίηση και αναπαράσταση του κυκλώματος ενδιαφέροντος σε ένα ισοδύναμο αποτελούμενο από στάδια διαγωγιμότητας (G_m–stages), με χαρακτηριστική εξίσωση ρεύματος εξόδου. Αν και η συγκεκριμένη τακτική υιοθετείται από διάφορες άλλες μεθόδους εκτίμησης παραμόρφωσης, η συνάρτηση που χρησιμοποιούν για το ρεύμα εξόδου των σταδίων διαγωγιμότητας συνήθως αποτελείται από μία δυναμοσειρά $3^{\eta\varsigma}$ τάξης, εξαρτώμενη μόνο από την τάση εισόδου του σταδίου, ή από το άθροισμα δύο δυναμοσειρών $3^{\eta\varsigma}$ τάξης, μίας εξαρτώμενης από την τάση εισόδου του σταδίου και μίας εξαρτώμενης από την τάση εξόδου. Και οι δύο επιλογές δύναται να μην μπορέσουν να αποτυπώσουν με την απαιτούμενη ακρίβεια την συμπεριφορά ρεύματος του κυκλωματικού σταδίου που μοντελοποιούν. Εδώ, το μοντέλο των σταδίων διαγωγιμότητας πέραν των ανεξάρτητων όρων λαμβάνει υπόψιν και όρους γινομένου των τάσεων εισόδου–εξόδου (cross–product terms). Έτσι, επιτυγχάνεται πολύ πιστή αναπαράσταση της συμπεριφοράς ρεύματος του πραγματικού σταδίου. Η μέγιστη δύναμη επιλέγεται ίση με την 3^{η}, που αποτελεί μία επιλογή καλής ισορροπίας μεταξύ ακρίβειας στην εκτίμηση και ευκολίας υπολογισμού.

Ο μετασχηματισμός του κυκλώματος σε ένα ισοδύναμο μοντέλο–δίκτυο σταδίων διαγωγιμότητας επιτυγχάνεται από τον διαχωρισμό του κυκλώματος σε διακριτές βαθμίδες σταδίων. Πρακτικά, όλες οι κυκλωματικές διατάξεις είναι αλυσίδες γνωστών μικρότερων τοπολογιών, οπότε η αναγνώριση των επιμέρους τμημάτων είναι μία διαδικασία αρκετά εύκολη και γνώριμη σε έναν σχεδιαστή. Το στάδιο διαγωγιμότητας που χρησιμοποιείται αποτελεί ένα αρκετά ευέλικτο στοιχείο μοντελοποίησης. Η μοντελοποίηση των περισσότερων θεμελιακών σταδίων σχεδίασης, όπως τα στάδια κοινής–πηγής (common–source), κοινής–πύλης (common–gate), ακολούθου–πηγής (source–follower), είναι άμεση, όπως είναι και η αναπαράσταση πλήρως–διαφορικών (fully–diferential) τμημάτων. Αναλυτικά παραδείγματα μετασχηματισμού δίνονται σε διάφορα τμήματα του κειμένου.

Μόλις ολοκληρωθεί το ισοδύναμο μοντέλο του κυκλώματος, πραγματοποιείται η εξαγωγή των συντελεστών της συνάρτησης ρεύματος κάθε σταδίου διαγωγιμότητας. Η εξαγωγή γίνεται μέσω μίας διαδικασίας τριών βημάτων. Αρχικά, διενεργείται μία ανάλυση μικρού σήματος (ac–analysis) πάνω στο κύκλωμα, η οποία σηματοδοτεί το μέγιστο πλάτος σήματος που μπορεί να αντιμετωπίσει κάθε τμήμα της τοπολογίας.

Στην συνέχεια ακολουθεί μία δισδιάστατη (2–dimensional) DC προσομοίωση σε κάθε διακριτό στάδιο με παραμέτρους τις τάσεις εισόδου και εξόδου του, έως τις μέγιστες τιμές που βρέθηκαν στο προηγούμενο βήμα, και αποθηκεύεται η συμπεριφορά του ρεύματος εξόδου. Με την ολοκλήρωση των δύο αυτών βημάτων, ακολουθεί η επεξεργασία των δεδομένων όλων των ρευμάτων εξόδου των επιμέρους σταδίων, από την οποία και εξάγονται οι συντελεστές της συνάρτησης των μοντέλων διαγωγιμότητας μέσω curve–fitting και επίλυσης ενός γραμμικού προβλήματος ελαχίστων τετραγώνων. Παράλληλα, ελέγχεται το κατά πόσον όλα τα στάδια συμπεριφέρονται ασθενώς μη-γραμμικά, το οποίο αποτελεί βασική προϋπόθεση για την επιτυχή εφαρμογή των προτεινόμενων μεθόδων, μέσω δύο κριτηρίων.

Δεδομένης της μοντελοποίησης του κυκλώματος υπό διερεύνηση με στάδια διαγωγιμότητας και της εξαγωγής των συντελεστών τους, η εκτίμηση της παραμόρφωσης πραγματοποιείται στο πεδίο του χρόνου, όπου τελικά απαλείφεται η χρονική εξάρτηση και παραμένουν ως άγνωστοι σταθεροί συντελεστές σε κάθε κόμβο του ισοδύναμου μοντέλου. Η διαδικασία και τα βήματα εκτίμησης της παραμόρφωσης παρουσιάζονται θεωρώντας μία γενική τοπολογία αποτελούμενη από n το πλήθος στάδια διαγωγιμότητας, οπότε η εφαρμογή των μεθόδων καθίσταται αρκετά φιλική στον πιθανό χρήστη.

Για την περίπτωση της αρμονικής παραμόρφωσης, γίνεται εκτίμηση της θεμελιώδους συχνότητας και των αρμονικών τόνων $2^{ης}$ και $3^{ης}$ τάξης σε δύο βήματα. Αρχικά, λαμβάνεται υπόψιν μόνο η επίδραση που έχει η θεμελιώδης συχνότητα και μέσω της επίλυσης ενός συστήματος γραμμικών εξισώσεων εκτιμούνται οι συντελεστές της σε κάθε κόμβο του ισοδύναμου μοντέλου. Το σύστημα γραμμικών εξισώσεων που απαιτείται για αυτό το βήμα έχει συστηματική μορφή και δημιουργείται μέσω της κατασκευής σταθερών πινάκων. Στην συνέχεια, για τον υπολογισμό των συντελεστών των αρμονικών τόνων γίνεται μία εκτίμηση των προϊόντων που συνεισφέρουν στην παραγωγή τους μέσω της εξίσωσης του ρεύματος εξόδου των σταδίων, και επιλέγονται τα κυριότερα αυτών. Η μη χρήση όλων των προϊόντων που γεννούνται από την συνάρτηση των ρευμάτων εξόδου των σταδίων–μοντέλων γίνεται αποσκοπώντας στην επίλυση του απλούστερου δυνατού προβλήματος χωρίς πρακτική απόκλιση στην ακρίβεια των αποτελεσμάτων της μεθόδου.

Δεδομένης της γνώσης των συντελεστών της θεμελιώδους συχνότητας από το πρώτο βήμα και με μία λογική προσέγγιση, προκύπτει το ότι οι συντελεστές ισχύος των αρμονικών τόνων μπορούν να εκτιμηθούν μέσω της επίλυσης ενός δεύτερου συστήματος γραμμικών εξισώσεων. Έτσι, μειώνεται δραματικά η απαιτούμενη υπολογιστική πολυπλοκότητα και η μέθοδος χαρακτηρίζεται από ταχύ προφίλ εκτέλεσης. Το σύστημα γραμμικών εξισώσεων για την εκτίμηση των αρμονικών τόνων χαρακτηρίζεται και αυτό από συστηματική μορφή, στενά συνδεδεμένη με την δομή του συστήματος της θεμελιώδους, η οποία περιλαμβάνει

και την κατασκευή πρόσθετων πινάκων. Η επίλυση του δεύτερου συστήματος γραμμικών εξισώσεων ολοκληρώνει την διαδικασία υπολογισμού των συντελεστών των ζητούμενων σημάτων, και καθίσταται άμεσα δυνατή η εκτίμηση της αρμονικής παραμόρφωσης μέσω των λόγων HD_2 και HD_3 σε κάθε κόμβο του κυκλώματος.

Παράλληλα, παρουσιάζεται μία διαδικασία εκτίμησης του σφάλματος που προκύπτει από την εξαίρεση προϊόντων που συνεισφέρουν στην παραγωγή της $2^{\eta\varsigma}$ και $3^{\eta\varsigma}$ αρμονικής. Η εξαίρεση αυτή κατέστησε δυνατή την εκτίμηση της αρμονικής παραμόρφωσης μέσω μία πρακτικά διπλής γραμμικοποίησης, ωστόσο πρέπει να επιβεβαιωθεί το ότι δεν επιφέρει ουσιαστικό σφάλμα και τα αποτελέσματα της μεθόδου είναι έγκυρα. Η μέθοδος εφαρμόζεται αναλυτικά σε αρκετά παραδείγματα διατάξεων ολοκληρωμένων κυκλωμάτων CMOS σε περιβάλλον προσομοίωσης, όπου και διαπιστώνεται η ακρίβειά της συγκρινόμενη με αποτελέσματα παραμετρικών PSS (periodic steady–state) αναλύσεων.

Στην συνέχεια, ο πυρήνας της μεθόδου για την αρμονική παραμόρφωση χρησιμοποιείται για την υλοποίηση της μεθόδου εκτίμησης παραμόρφωσης ενδοδιαμόρφωσης. Το συγκεκριμένο εγχείρημα αποτελεί ένα πολυπλοκότερο πρόβλημα από αυτό της περίπτωσης της αρμονικής παραμόρφωσης. Ενώ στην περίπτωση της αρμονικής παραμόρφωσης η θεώρηση μόνο των τόνων ενδιαφέροντος (θεμελιώδης, 2^{η} και 3^{η} αρμονική) ήταν αρκετή για την ακριβή εκτίμησή τους, στην παραμόρφωση ενδοδιαμόρφωσης είναι αναγκαία η θεώρηση επιπλέον συχνοτήτων για ακριβή αποτελέσματα. Με την προσθήκη των απαραίτητων συχνοτήτων, η εκτίμηση του λόγου IM_3 πραγματοποιείται αντίστοιχα, μέσω της επίλυσης δύο συστημάτων γραμμικών εξισώσεων, προσδίδοντας μεγάλη ταχύτητα εκτέλεσης στην προτεινόμενη μέθοδο. Το πλήθος των εμπλεκόμενων όρων είναι μεγαλύτερο σε σχέση με την μέθοδο της αρμονικής παραμόρφωσης, παραμένει ωστόσο σε πλήρως διαχειρίσιμη μορφή. Η επιβεβαίωση της ακρίβεια της μεθόδου εκτίμησης παραμόρφωσης ενδοδιαμόρφωσης γίνεται και αυτή σε σύγκριση με τα αποτελέσματα παραμετρικών PSS αναλύσεων σε τοπολογίες ολοκληρωμένων κυκλωμάτων CMOS.

Μέρος ΙΙ: **Αρχιτεκτονική Σταδίου Εξόδου Υψηλής Γραμμικότητας και Απόδοσης**

Οι ενισχυτές ισχύος αποτελούν ένα από τα πιο συχνά χρησιμοποιούμενα κυκλώματα, με το στάδιο εξόδου τους να διαδραματίζει καίριο ρόλο στην γραμμικότητα και κατανάλωση ισχύος της διάταξης της οποίας αποτελούν μέρος. Τα δύο χαρακτηριστικά, γραμμικότητα και απόδοση, συνήθως έρχονται σε αντιδιαστολή (trade–off), ενώ ταυτόχρονα είναι επιθυμητά στον μέγιστο δυνατό βαθμό κατά τη διάρκεια σχεδίασης ενός σταδίου εξόδου.

Προς αυτή την κατεύθυνση, διάφορες τάξεις σταδίων εξόδου προσπαθούν να παρουσιάσουν μία βέλτιστη συμπεριφορά σε ένα από τα δύο αυτά μεγέθη, ή

ιδανικά και στα δύο. Στην γραμμική οικογένεια σταδίων εξόδου, αυτά της τάξης–A χαρακτηρίζονται από πολύ υψηλή γραμμικότητα αλλά χαμηλή απόδοση, η τάξη–B βελτιώνει την απόδοση αλλά παρουσιάζει παραμόρφωση crossover (crossover distortion), ενώ στάδια τάξης–AB βρίσκονται ανάμεσα στις προαναφερθείσες κατηγορίες όσων αφορά στην απόδοση. Στον αντίποδα, οι τοπολογίες διακοπτόμενων σταδίων εξόδου, όπως η τάξη–D, χαρακτηρίζονται από υψηλά νούμερα απόδοσης, αλλά υστερούν στο κομμάτι της γραμμικότητας.

Μία προσπάθεια διατήρησης των καλών χαρακτηριστικών γραμμικότητας της πρώτης οικογένειας σταδίων εξόδου και βελτίωσης της απόδοσής τους απαντάται στις τοπολογίες τάξης–G και τάξης–H. Οι συγκεκριμένες τάξεις λειτουργούν κατά κανόνα σε πόλωση τάξης–AB, αλλά χρησιμοποιούν είτε πολλαπλά διακριτά επίπεδα τάσεων τροφοδοσίας (τάξη–G), είτε τροφοδοσία που χαρακτηρίζεται από δυναμική συμπεριφορά κάποιας μορφής (τάξη–H).

Η προτεινόμενη αρχιτεκτονική σταδίου εξόδου χρησιμοποιεί ένα push–pull στάδιο εξόδου πολωμένο σε τάξη–A και ένα σύστημα συνεχούς δυναμικής τροφοδοσίας το οποίο ακολουθεί (tracks) ως αναφορά την έξοδο με ένα περιθώριο τάσης κατάλληλου προσήμου, δημιουργώντας δύο μετατοπισμένα αντίγραφά της ως γραμμές τροφοδοσίας. Με αυτό τον τρόπο μειώνεται η απώλεια ισχύος στα τρανζίστορ εξόδου και αυξάνεται σημαντικά η απόδοση της διάταξης, ενώ παράλληλα βελτιώνεται ακόμα περισσότερο η γραμμικότητα του σταδίου στις συχνότητες για τις οποίες προορίζεται η χρήση του. Το σύστημα δυναμικής τροφοδοσίας αποτελείται από δύο DC–DC buck μετατροπείς (DC–DC buck–converters) ικανούς να παράξουν τάσεις τροφοδοσίας συχνοτήτων έως μερικές δεκάδες kHz, με στόχο την χρήση της τοπολογίας σε εφαρμογές αναπαραγωγής ήχου (audio) ή μετρήσεων χαμηλόσυχνων σημάτων.

Αρχικά, γίνεται ανάλυση και εξαγωγή των συνθηκών πόλωσης του push–pull πυρήνα της αρχιτεκτονικής, ώστε να λειτουργεί σε καθαρή τάξη–A κάτω από όλες τις συνθήκες σήματος εισόδου για τις οποίες προδιαγράφεται. Η τοπολογία εξετάζεται σαν μία CMOS υλοποίηση, χωρίς φυσικά να αποκλείεται η χρήση διπολικών τρανζίστορ (BJT) ή και συνδυασμός τους. Στην συνέχεια, με τα στοιχεία πόλωσης και τις εκφράσεις των ρευμάτων του σταδίου εξόδου γνωστά, γίνεται ανάλυση του συστήματος των δύο DC–DC buck μετατροπέων σε χώρο–κατάστασης (state–space). Η φιλοσοφία της προτεινόμενης αρχιτεκτονικής επιτρέπει την χρήση time–averaging στα συστήματα εξισώσεων που αντιστοιχούν στις δύο διακριτές μορφές συνδεσμολογίας των μετατροπέων, απλοποιώντας την ανάλυση. Τα προκύπτοντα συστήματα εξισώσεων είναι διγραμμικά (bilinear). Ωστόσο, μία λογική σχεδιαστική επιλογή για τα διακοπτικά στοιχεία των μετατροπέων καθιστά προσεγγιστικά δυνατή την εξάλειψη των διγραμμικών όρων, επιτρέποντας έτσι την χρήση γραμμικών, χρονικά–αμετάβλητων (LTI) συστημάτων.

Δεδομένων των συστημάτων εξισώσεων των μετατροπέων, ακολουθεί διαστασιολόγηση του πηνίου (L) και του πυκνωτή (C) τους βάσει μέγιστων επιτρεπτών τιμών στην διακύμανση του ρεύματος και της τάσης εξόδου τους. Παράλληλα, δίνεται μία εκτίμηση άνω φράγματος του γινομένου LC ώστε το tracking της τάσης αναφοράς για την δημιουργία των γραμμών τροφοδοσίας να παραμένει σε ικανοποιητικά επίπεδα. Στην συνέχεια, προτείνεται ένα σχήμα ελέγχου ανατροφοδότησης (feedback control scheme) για την αρχιτεκτονική, κάνοντας χρήση των γραμμικών, χρονικά–αμετάβλητων συστημάτων. Κλείνοντας το κομμάτι της θεωρητικής ανάλυσης, το συγκεκριμένο σχήμα ελέγχου εξετάζεται ως προς την ευρωστία (robustness) του στην περίπτωση που δεν ισχύει η συνθήκη για τα διακοπτικά στοιχεία των μετατροπέων και τα συστήματα εξισώσεων έχουν την αρχική, διγραμμική τους μορφή.

Ακολουθεί μία proof–of–concept υλοποίηση της προτεινόμενης αρχιτεκτονικής σταδίου εξόδου, με αναλυτική παρουσίαση όλων των τμημάτων της, σε τεχνολογία ολοκληρωμένων κυκλωμάτων CMOS σε περιβάλλον προσομοίωσης. Τα αποτελέσματα σκιαγραφούν την συμπεριφορά και τα χαρακτηριστικά της αρχιτεκτονικής, ενώ μία σύγκριση με ένα στάδιο εξόδου τάξης–A αναδεικνύει τα πλεονεκτήματά της, ολοκληρώνοντας την διατριβή.

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List of Author's Publications

International Peer–Reviewed Journals

1. **D. Baxevanakis** and P. P. Sotiriadis, "A General Time–Domain Method for Harmonic Distortion Estimation in CMOS Circuits," in *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, vol. 40, no. 1, pp. 157-170, Jan. 2021, doi: 10.1109/TCAD.2020.2988414

2. **Baxevanakis D.**, Alimisis V., and Sotiriadis P. P., "An intermodulation distortion estimation method for linear CMOS circuits", in *International Journal of Circuit Theory and Applications*, 2021; 49: 1244–1260, doi: 10.1002/cta.2961

3. **D. Baxevanakis**, P. G. Zarkos, C. G. Adamopoulos, I. Vassiliou, and P. P. Sotiriadis, "Design Optimization Guidelines for a Class of RF Switched–Capacitor Power Amplifiers", in *AEÜ – International Journal of Electronics and Communications*, Volume 138, August 2021, 153876, doi: 10.1016/j.aeue.2021.153876

4. P. P. Sotiriadis, C. G. Adamopoulos, **D. Baxevanakis**, P. G. Zarkos, and I. Vassiliou, "RF Switched–Capacitor Power Amplifier Modeling," in *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, vol. 40, no. 8, pp. 1525-1530, Aug. 2021, doi: 10.1109/TCAD.2020.3025207

5. Voudoukis, N.; Dimas, C.; Asimakopoulos, K.; **Baxevanakis, D.**; Papafotis, K.; Oustoglou, K.; Sotiriadis, P.P. The Importance of Introducing the OCTC Method to Undergraduate Students as a Tool for Circuit Analysis and Amplifier Design. *Technologies* 2020, 8, 7, doi: 10.3390/technologies8010007

International Peer–Reviewed Conferences

1. **D. Baxevanakis** and P. P. Sotiriadis, "Accurate Harmonic Distortion Estimation in CMOS Circuits using a Cross–Product Gm–Stage Modeling," *2020 IEEE International Symposium on Circuits and Systems*, Sevilla, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9181113

2. **D. Baxevanakis** and P. P. Sotiriadis, "A 1.8V CMOS chopper four–quadrant analog multiplier," *2017 6th International Conference on Modern Circuits and Systems Technologies*, Thessaloniki, 2017, pp. 1-4, doi: 10.1109/MOCAST.2017.7937649

3. S. Pokamisas, **D. Baxevanakis**, and P. P. Sotiriadis, "A 0.6V, 700nW Chopper Capacitively–Coupled Instrumentation Amplifier for Biomedical Applications," *2019 8th International Conference on Modern Circuits and Systems Technologies*, Thessaloniki, 2019, pp. 1-4, doi: 10.1109/MOCAST.2019.8741847

4. N. F. Voudoukis, **D. Baxevanakis**, K. Papafotis, C. Dimas, C. Oustoglou, and P. P. Sotiriadis, "Introducing Senior Undergraduate Students to the Open–Circuit Time–Constant Method for Circuit Analysis," *2019 8th International Conference on Modern Circuits and Systems Technologies*, Thessaloniki, 2019, pp. 1-4, doi: 10.1109/MOCAST.2019.8741560

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Abbreviations

2D	2–Dimensional
ac	Alternating Current
BIBO	Bounded–Input, Bounded–Output
BJT	Bipolar Junction Transistor
CG	Common–Gate
CMOS	Complementary MOS
CS	Common-Source
CTA	Continuously Tracking A
DC	Direct Current
EDA	Electronic Design Automation
HD_2	2^{nd} Harmonic Distortion Factor
HD_3	3^{rd} Harmonic Distortion Factor
IM_3	3^{rd}–Order Intermodulation Product
LMIs	Linear Matrix Inequalities
LTI	Linear, Time–Invariant
MOS	Metal–Oxide–Semiconductor
MOSFET	MOS Field–Effect Transistor
NMOS	N–Type MOS
OTA	Operational Transconductance Amplifier
PI	Proportional–Integral
PID	Proportional–Integral–Derivative
PMOS	P–Type MOS
PSS	Periodic Steady–State
PVT	Process, Voltage, Temperature

PWM	Pulse–Width Modulation
RF	Radio Frequency
SF	Source–Follower
THD	Total Harmonic Distortion

Thesis Outline

The thesis is divided in two parts. In the first part, the developed methodologies for the estimation of harmonic and intermodulation distortion are presented, while the second part demonstrates the proposed power stage architecture.

More specifically, Chapter 1 illustrates the harmonic distortion estimation method. A thorough modeling of CMOS stages is initially given, and is followed by the derivation of the required G_m–stage model coefficients, while some criteria on whether a circuit is exhibiting weak nonlinear behavior (and thus, whether the proposed distortion estimation is meaningful) are also introduced. With these at hand, the general harmonic distortion estimation method is presented alongside with examples and additional remarks on its application. Simulation results validate the method's accuracy.

Chapter 2 adopts the principles introduced in Chapter 1 for the estimation of harmonic distortion, and presents the intermodulation distortion estimation method as a standalone part. A shorter outline of the G_m–stage modeling of CMOS stages and the acquisition of its coefficients is firstly described, with the estimation of the intermodulation distortion coming afterwards. Finally, the method is evaluated on circuit examples by comparison with simulation.

Closing the thesis, Chapter 3 demonstrates the proposed high–linearity and high–efficiency power stage architecture. A complete theoretical analysis of the topology and a feedback control scheme are presented, able to serve as a design guide, while an investigation on the control scheme robustness is also given. The behavior and advantages of the architecture are illustrated through a proof–of–concept CMOS technology implementation in simulation environment.

Στην Κατερίνα,
Δημήτρης

Part I

Harmonic & Intermodulation Distortion Estimation Methodologies for Linear CMOS Circuits

1 Harmonic Distortion Estimation in CMOS Circuits

This chapter presents a general, time–domain harmonic distortion estimation method, applicable to linear CMOS circuits characterized by weakly nonlinear behavior, ranging from amplifiers and transconductors to filters, with any number of stages. It offers a compact, fast and systematic way to model circuits as a structure of interconnected G_m–stages, and estimates the harmonic distortion at every circuit node, providing insight into the distortion contribution of every stage. The method uses a more involved model for each G_m–stage that also accounts for the dependence of its output current on cross–products of its input and output voltages, improving significantly the distortion estimation accuracy. The proposed method is easily implemented in MATLAB, and intends to be integrated as a tool in EDA suites to speed–up distortion estimation. A number of examples are presented, illustrating the application of the method and validating its accuracy via comparison with Cadence Spectre simulation.

1.1 Introduction

Harmonic distortion is an important aspect in characterizing a circuit's performance. Harmonic distortion and noise determine its dynamic range [1], whereas alongside with intermodulation distortion they dictate the circuit's overall linearity. As such, it is a quantity of major impact and interest in a plethora of applications, like audio and power amplifiers [2], radio–frequency amplifiers [3], low–noise amplifiers, filters and more.

Supposing that a circuit is being driven by a sinusoidal signal of fundamental frequency ω, the total harmonic distortion (THD) at its output is defined as the ratio

of the combined power of all generated harmonics to the power of the fundamental

$$\mathrm{THD} = \sqrt{\frac{\sum_{k=2}^{\infty} V_{h_k}^2}{V_f^2}} \cdot 100\%. \tag{1.1}$$

V_{h_k} is the (voltage) amplitude of the k–th harmonic, at frequency $k\omega$, and V_f is the amplitude of the fundamental tone.

Realistically, under weakly nonlinear circuit behavior, the harmonic amplitudes decrease rapidly as their order increases, which in turn significantly decreases the number of harmonics needed to have a good estimation of THD. Depending on the specific circuit topology, the dominant harmonic tones are the second and the third harmonic. This raises interest in determining the HD_2 and HD_3 distortion factors

$$\mathrm{HD}_2 = \left|\frac{V_{h_2}}{V_f}\right|, \quad \mathrm{HD}_3 = \left|\frac{V_{h_3}}{V_f}\right| \tag{1.2}$$

that are the estimation subjects of this work.

Accurate prediction of distortion is in general a complicated task. A possible way of estimating the distortion in a circuit is by simulation. A sinusoidal input results in sinusoidal currents and voltages of the same frequency (assuming no chaotic behavior or subharmonic generation), and so simulation methods like harmonic balance or shooting [4, 5], are most appropriate. Unfortunately, the estimation of distortion by such methods is usually time–consuming and computationally expensive [6], does not provide any insight [7], and does not aid with optimization or parameterization of the design.

Dedicated methods that predict the distortion behavior and are easy to use, while being open to parameterization and provide insight are sought after. A popular approach is by means of the Volterra series [8], where the circuit is decomposed into various order operators, each one characterized by a time– or frequency–domain Volterra kernel. Even though the use of Volterra series can yield quite accurate results, there are shortcomings; the operators' expression and manipulation becomes cumbersome when the number of circuit elements (and thus, distortion contributions) rises, which is almost always the case for practical circuits.

Recently, a methodology utilizing linear–centric circuit models to account for individual distortion contributions in a circuit was reported [9]. Systematic, time–domain state–space harmonic distortion estimation approaches for weakly nonlinear G_m–C filters of any order [10, 11, 12], and a distortion contribution analysis that uses the best linear approximation [13] were also proposed; the latter methodology deviates from the classical distortion point of view and adopts a noise–like analysis, being also capable of handling strong nonlinearities.

Several other methods describe the dominant distortion terms in the frequency–

domain [14, 15], where many use algebraic manipulation of simplified amplifier models [16, 17, 18, 19, 20, 21, 22, 23, 24]. The analysis is mainly focused on the most frequently used amplifier topologies, with one, two, or three stages, employing negative feedback and Miller compensation. Even though some share similarities with the Volterra series approach [25], or adopt them [3, 15], they provide a set of equations ready to be used. However, most works are usually tailored for specific topologies, and may require extensive algebraic manipulation to be applied to more general cases. Additionally, the models used in many of these approaches could fail to capture faithfully the current-characteristic of a CMOS stage, as will be demonstrated in the sections to follow.

This chapter extends [26] and proposes a general, time–domain harmonic distortion estimation method for CMOS circuits that exhibit weak nonlinearities. It offers a compact and systematic approach that can be applied to circuit structures ranging from simple transconductors to cascaded amplifiers and filter designs, with any number of stages. It provides a fast and highly accurate estimation of distortion factors HD_2 and HD_3 by manipulating the circuit under consideration as a structure of interconnected G_m–stages. Each G_m–stage is characterized by a more involved model of its current-characteristic, whose parameters are extracted via curve–fitting. The method is easily implemented in numerical computing environments like MATLAB, and intends to serve as an integrated tool in dedicated EDA software (like Cadence Spectre) to speed–up distortion estimation.

This chapter is organized as follows. Section 1.2 presents the modeling of CMOS stages, and Section 1.3 outlines the derivation of the G_m–stage model coefficients. Section 1.4 introduces the proposed method alongside with examples of its application, while the method's accuracy is validated through simulation results in Section 1.5. Finally, a summary is given in Section 1.6.

1.2 G_m–Stage Modeling

A MOS transistor eventually constitutes a voltage–controlled current source. In the same vein, a CMOS gain stage producing an output current in response to an input voltage can be thought of as a G_m–stage, a representation of which is depicted in Figure 1.1.

Throughout this work, the following notation is used; $G^m_{i,t,j}$ is the G_m–stage with positive input, u_i, at node i; negative input, $k_{itj}u_t$, from node t, with k_{itj} a real feedback factor[1]; and output current, i_{itj}, at node j. The stage's differential input voltage is then

$$\widetilde{u}_{itj} = u_i - k_{itj}u_t. \tag{1.3}$$

[1]This particular notation is adopted to capture a range of popular topologies.

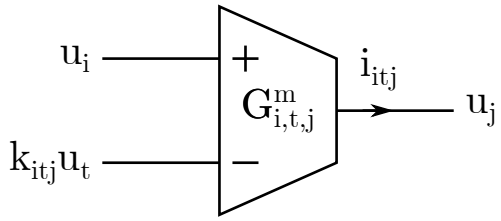

Figure 1.1: G_m–stage representation.

The *itj*–triplet[2] is included in all of the characteristics of a G_m–stage. The ac–ground is marked as r (reference potential).

For keeping the expressions and notation as simple as possible, single–ended output G_m–stages were preferred. This however does not limit the application of the proposed method, as fully–differential circuits can be easily modeled by single–ended output G_m–stages, as described later in Section 1.2.4.

A stage's output current is in general a nonlinear function of its input and output voltages

$$i_{itj} = f_{i,t,j}\left(\widetilde{u}_{itj}, u_j\right), \quad f_{i,t,j} : \mathbb{R}^2 \to \mathbb{R}. \tag{1.4}$$

This nonlinearity is the cause of distortion generation.

Parasitic capacitors in MOS transistors are reported to don't have significant nonlinearity contribution; they reduce the magnitude of the output impedance at high frequencies [27, 28]. This enables the formation of an equivalent model based only on the DC–characteristics of a CMOS stage. Such a model can be obtained by approximating the stage's output current with a power–series expansion around its DC–operating point.

1.2.1 Simple Model

The simplest case results by neglecting the output voltage dependence and modeling the whole stage as a single current source that is governed by power terms of its input voltage

$$i_{itj} = \sum_{k\geq 1} g_{itj,k}\widetilde{u}_{itj}^{k} \tag{1.5}$$

where $g_{itj,k}$ is the corresponding coefficient for each power, k, of $\widetilde{u}_{itj}^{k}$. This approach, however, will result in poor accuracy since it even fails to account for the finite output impedance of the stage. As such, a better approximation has to be made.

[2]Commas between i, t, and j are omitted in coefficients, voltages and currents for simplicity.

1.2.2 More Accurate Model

The most frequently adopted approach [17, 18, 20, 21, 23] is to take into account both the input and output voltages and have a power–series approximation of the form

$$i_{itj} = \sum_{k\geq 1} \left(g_{itj,k} \widetilde{u}^k_{itj} + \overline{g}_{itj,k} u^k_j \right). \tag{1.6}$$

Since HD_2 and HD_3 are the dominant distortion factors, one can restrict $k = 1, 2, 3$ to end up with an easy to manipulate and fairly accurate expression[3]. An additional advantage of this approximation is that the input– and output–related terms are independent of one another; nonetheless, this can lead to significant deviations in the expected behavior of a G_m–stage.

To illustrate such a case, consider the common–source (CS) amplifier of Figure 1.2. Its load, $R_L \parallel C_L$, has a reference voltage of V^{op}_{OUT}, the DC–operating point of the unloaded output.

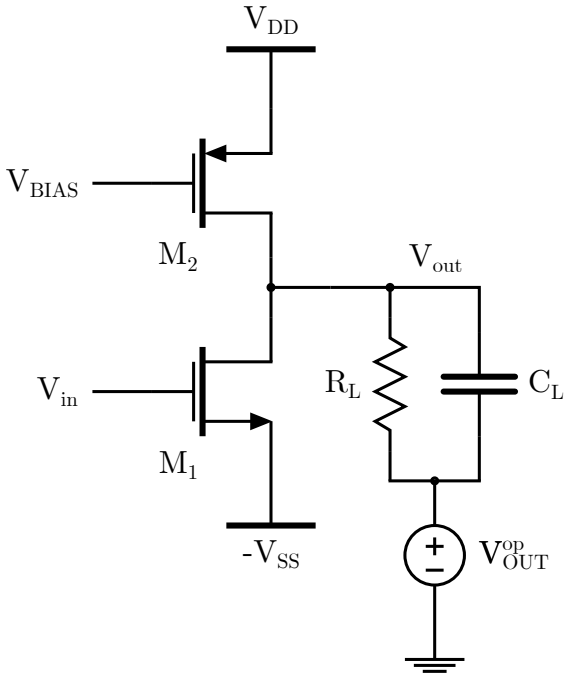

Figure 1.2: CS amplifier.

Should the input and output voltages be independent, the circuit of Figure 1.3 must produce the same distortion. The original CS stage is mirrored, isolating the interference between the input and output voltages; V_{in} acts under a fixed V^{op}_{OUT} and produces a current signal, i_{sig}; this signal is in turn injected into the output node of

[3]Including higher–order terms will account better for distortion expansion and compression at the harmonics of interest; however, since weak nonlinearities are assumed, the error will be negligible.

the mirror–stage (operating under V_{IN}^{op}, the input DC–operating point of Figure 1.2), creating V'_{out}.

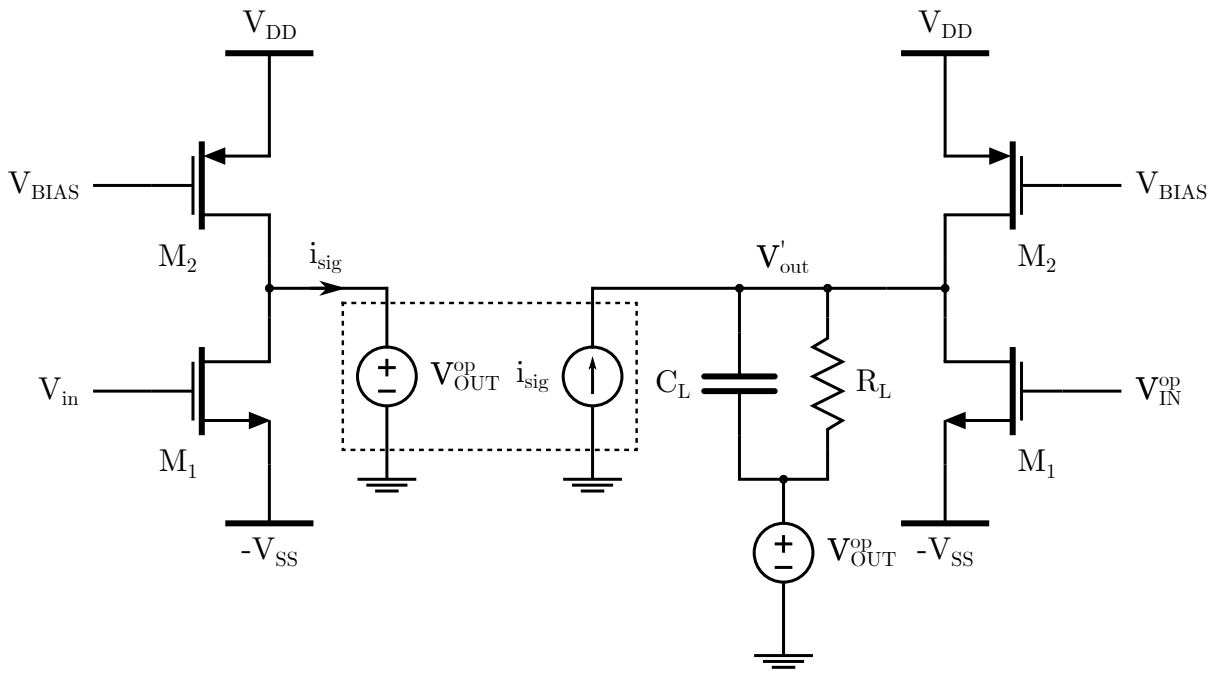

Figure 1.3: CS amplifier – independent input and output voltages.

The two cases were simulated by means of Cadence Spectre in TSMC 0.18 µm technology. The amplifier has a DC–gain of 14.7 dB under a load of 10 kΩ ‖ 10 pF, and a unity–gain frequency of 9.35 MHz. A parametric (with respect to frequency) periodic steady–state (PSS) harmonic balance analysis is performed, with a sinusoidal input signal of 50 mV peak. The resulting HD_2 and HD_3 are presented in Figures 1.4 and 1.5, respectively. It is evident that the two circuits exhibit different distortion mechanisms, even though they have the same fundamental frequency response. Similar findings on the importance of input–output related terms have been recently reported [15].

1.2.3 Proposed Model

Given the drawbacks of the previous approach, it is fair to say that a suitable model should also include cross–products of the input and output voltages. Such approximations have been used at transistor–level [27, 28, 29, 30, 3], where the device acting as amplifier is supposed to admit a two– or three–dimensional Taylor series expansion; the corresponding coefficients of the approximation are then calculated by the partial derivatives of the transistor's current relationship. Equivalent approaches have been adopted at stage–level [31, 32, 33, 3, 14, 15].

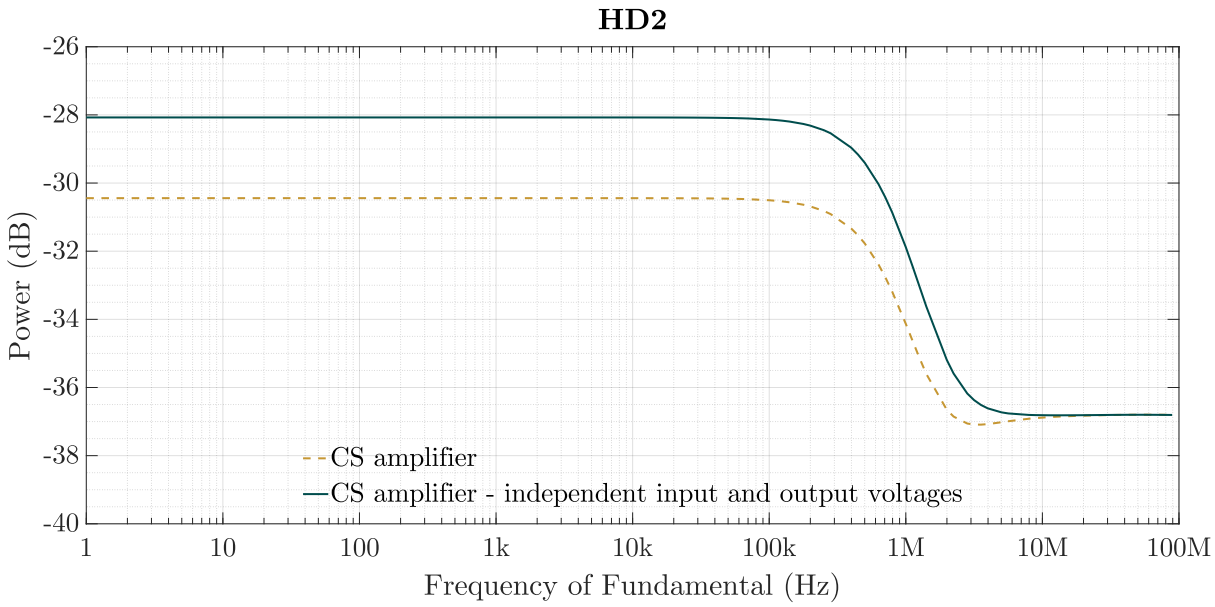

Figure 1.4: HD_2 of the two CS amplifier cases.

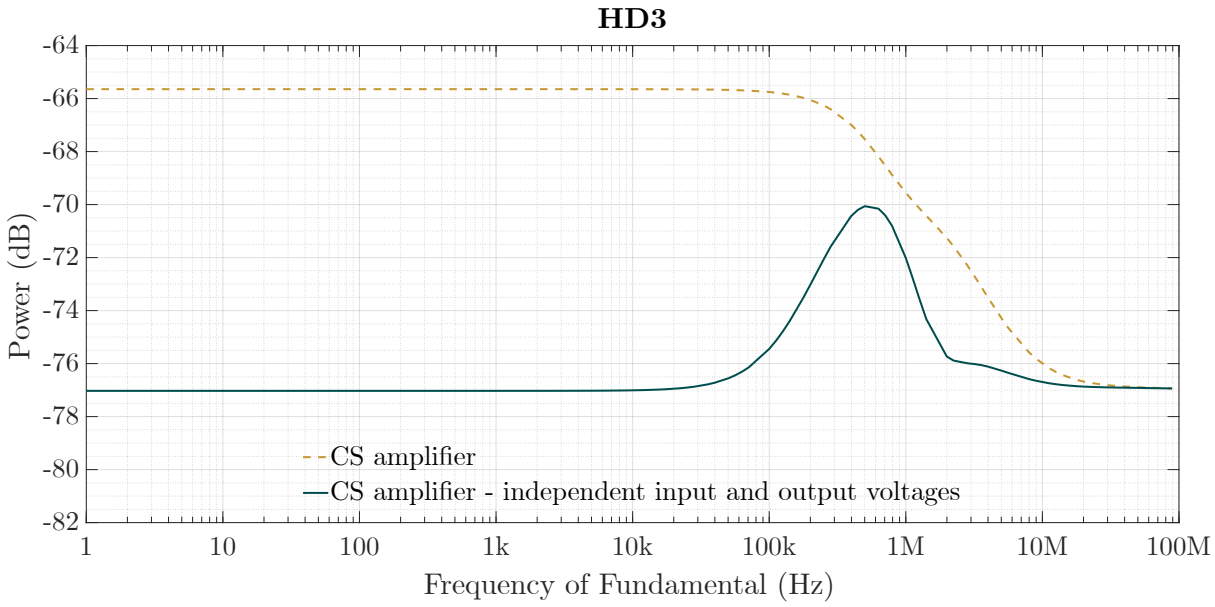

Figure 1.5: HD_3 of the two CS amplifier cases.

In this work, each G_m–stage is considered to have a time–domain [34, 10, 11, 12] power–series current expression

$$i_{itj} = \sum_{\substack{k,\ell \geq 0 \\ k+\ell \geq 1}} g_{itj}^{k\ell} \widetilde{u}_{itj}^{k} u_j^{\ell}. \tag{1.7}$$

Note that for notation simplicity, the $k\ell$–superscript in the $g_{itj}^{k\ell}$–coefficients indicates the

corresponding power of $\widetilde{u}_{itj}^{k}$ and u_j^{ℓ}, and not a power term of the coefficient itself.

It is chosen that $k+\ell = 1,2,3$, to capture the dominant contributing terms to the fundamental, second and third harmonic, and (1.7) reduces to

$$i_{itj} = g_{itj}^{10}\widetilde{u}_{itj} + g_{itj}^{20}\widetilde{u}_{itj}^{2} + g_{itj}^{30}\widetilde{u}_{itj}^{3} + g_{itj}^{01}u_j + g_{itj}^{02}u_j^2 + g_{itj}^{03}u_j^3 + g_{itj}^{11}\widetilde{u}_{itj}u_j + g_{itj}^{21}\widetilde{u}_{itj}^{2}u_j + g_{itj}^{12}\widetilde{u}_{itj}u_j^2. \quad (1.8)$$

The $g_{itj}^{k\ell}$–coefficients of (1.8) of each G_m–stage are derived by curve–fitting to capture in detail its amplitude–adjusted nonlinearities. Taylor series expansion at the DC–operating point (used in most of the aforementioned works and employed in various analyses) is accurate only locally for small signal amplitudes [35]. The derivation procedure of the $g_{itj}^{k\ell}$–coefficients is described analytically in Section 1.3.

Equation (1.8) can establish a circuit equivalent like the one depicted in Figure 1.6. The circuit is comprised of a voltage–controlled current source, $\widetilde{i}_{itj}$, alongside with a voltage–controlled conductance, $\widetilde{G}_{itj}$, set by the differential input voltage, $\widetilde{u}_{itj}$; a nonlinear conductance, $\overline{G}_{itj}$, due to the output voltage, u_j; and a nonlinear, voltage–controlled conductance, G_{itj}, due to the cross–product $\widetilde{u}_{itj}u_j$. Their relationships are given by (1.9)–(1.12).

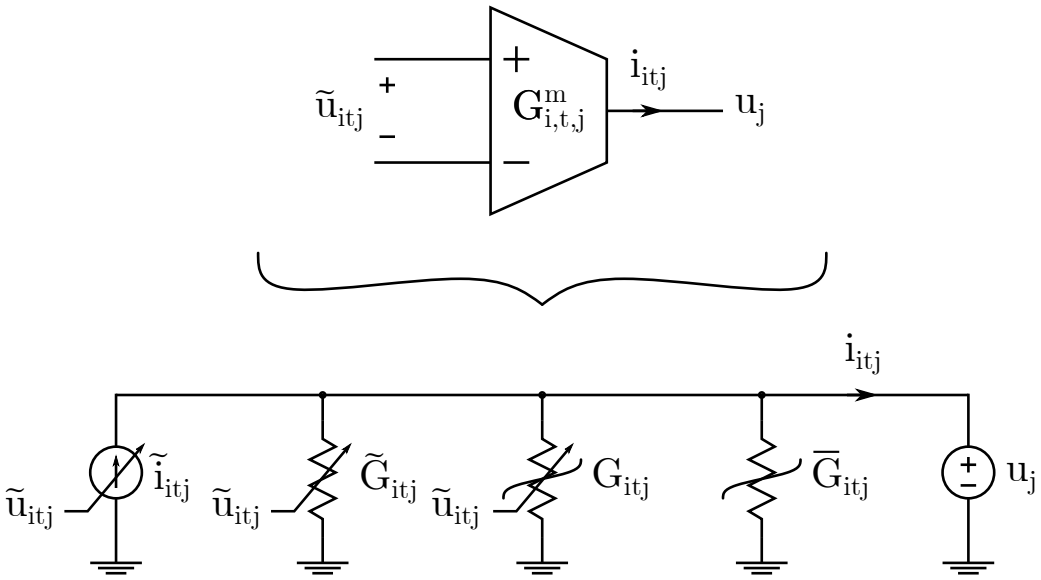

Figure 1.6: G_m–stage circuit equivalent.

$$\widetilde{i}_{itj} = g_{itj}^{10}\widetilde{u}_{itj} + g_{itj}^{20}\widetilde{u}_{itj}^{2} + g_{itj}^{30}\widetilde{u}_{itj}^{3} \quad (1.9)$$

$$\widetilde{G}_{itj} = -g_{itj}^{11}\widetilde{u}_{itj} - g_{itj}^{21}\widetilde{u}_{itj}^{2} \quad (1.10)$$

$$G_{itj} = -g_{itj}^{12}\widetilde{u}_{itj}u_j \quad (1.11)$$

$$\overline{G}_{itj} = -g_{itj}^{01} - g_{itj}^{02}u_j - g_{itj}^{03}u_j^2. \quad (1.12)$$

1.2.4 Formulation of Standard CMOS Gain Stages

The formulation of a CMOS gain stage depends on its topology, and thus, whether it is single–ended or fully–differential.

Single–Ended Structures

The differential–pair can be modeled directly in the form of Figure 1.1. For a CS stage, the negative input should be ac–grounded; a source–follower (SF) stage should be treated as a G_m–stage with 100% negative feedback ($k_{ijj} = 1$), as shown in Figure 1.7.

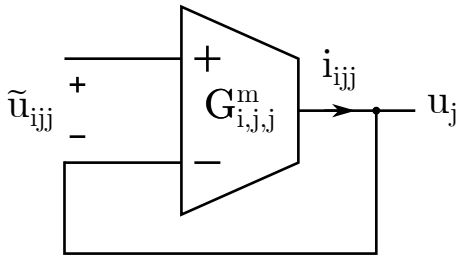

Figure 1.7: SF stage as a G_m–stage.

A common–gate (CG) stage is modeled as depicted in Figure 1.8, where antiparallel stages $G^m_{i,r,j}$ and $G^m_{r,i,i}$ have the same $g^{k\ell}_{itj}$–coefficients. This formulation results from the fact that in a CG stage the output current flows towards its input source, as depicted in Figure 1.9.

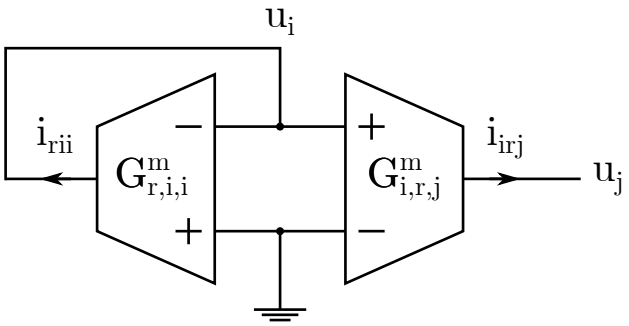

Figure 1.8: CG stage as a G_m–stage.

Stages that result from combinations of the aforementioned standard ones can be represented as connections of their G_m–stage equivalents, or even be treated as a single G_m–stage. An example of the latter case is presented in Section 1.4.5.

Fully–Differential Structures

In the case of a fully–differential stage, an appropriate representation would be that of Figure 1.10. The two G_m–stages are connected with their inputs in parallel, and each

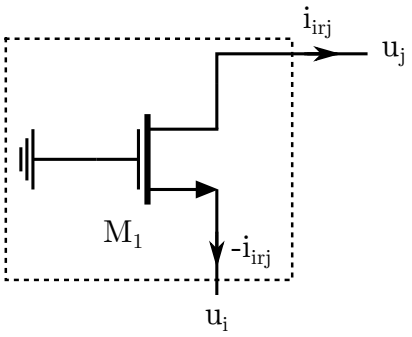

Figure 1.9: Simple CG stage.

set of $g_{itj}^{k\ell}$–coefficients results from the common input and the corresponding output. Ideally, $g_{itm}^{k\ell} = -g_{itj}^{k\ell}$, so as to achieve $i_{itm} = -i_{itj}$.

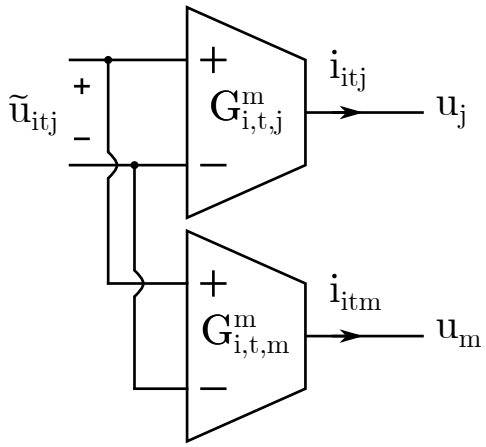

Figure 1.10: Fully–differential structure G_m–stage representation.

1.2.5 Circuit Transformation into a G_m–Stage Equivalent

The transformation of a circuit into an equivalent representation of G_m–stages relies on identifying the standard CMOS gain stages that it is comprised of, and their interconnections.

As an example, consider the three–stage feedback amplifier of Figure 1.11. The amplifier consists of 3 cascaded stages (differential–pair, CS, SF) and a buffer stage (SF) for Miller compensation.

The equivalent representation of the amplifier is that of Figure 1.12. Transistors M_0–M_4 of the differential–pair form the first G_m–stage, $G_{0,3,1}^m$, while the CS stage of M_5–M_6 forms the second stage, $G_{1,r,2}^m$. The SF stage of M_7–M_8 forms $G_{2,3,3}^m$, and the SF stage of M_9–M_{10} forms $G_{2,4,4}^m$. Moreover, it is $k_{233} = k_{244} = 1$, as described in Section 1.2.4.

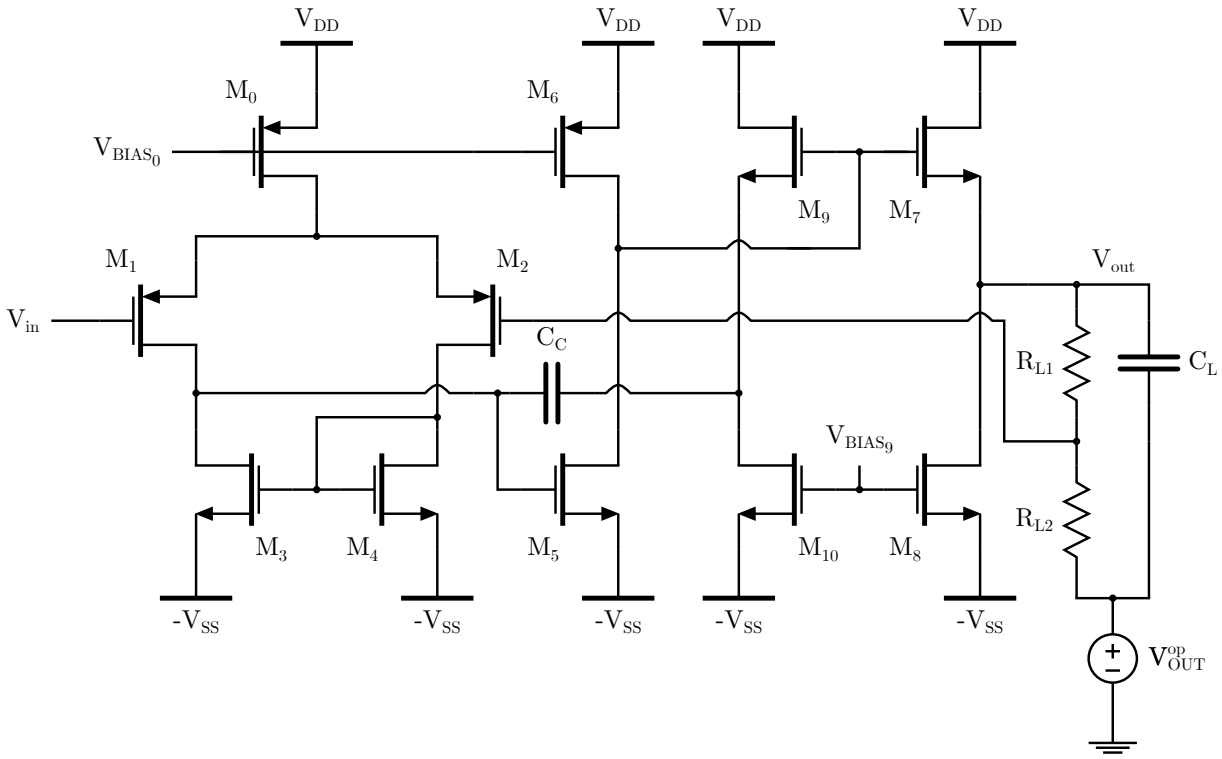

Figure 1.11: Three–stage feedback amplifier.

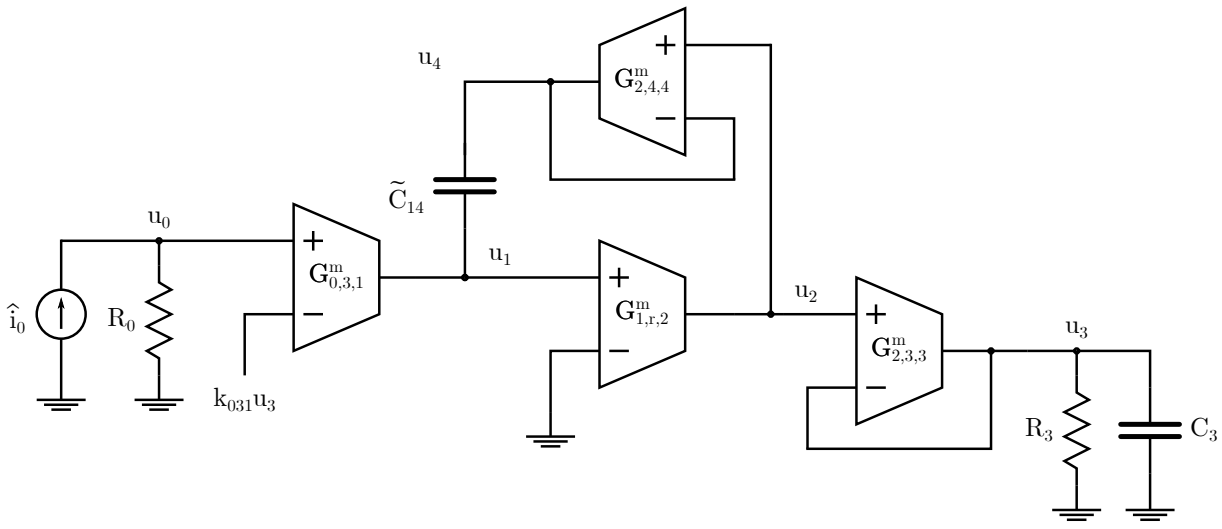

Figure 1.12: G_m–stage equivalent representation of the three–stage feedback amplifier.

The negative input of the differential–pair (and thus, $G^m_{0,3,1}$) is fed with an ac–voltage voltage of

$$\frac{R_{L_2}}{R_{L_1}+R_{L_2}}u_{out} = k_{031}u_{out} = k_{031}u_3$$

where $R_{L_1}+R_{L_2} = R_L = R_3$. Finally, $C_L = C_3$ and $C_C = \widetilde{C}_{14}$. The ac–input signal,

$u_{in} = u_0$, is realized by the current source $\hat{i}_0 = u_0/R_0$ that acts on the normalized[4] $R_0 = 1\,\Omega$; this transformation results from the method's formulation that is presented in Section 1.4.

1.3 Model Coefficients Derivation

The derivation of the $g_{itj}^{k\ell}$–coefficients of each G_m–stage model can be performed by a three–step procedure that involves an ac–analysis performed to the whole circuit structure, 2–dimensional (2D) DC–sweeps around the input and output DC–operating points of each stage, and, finally, linear regression for the estimation of the coefficients. The findings of this procedure should confirm weakly nonlinear behavior for all G_m–stages, otherwise the method's accuracy will be degraded.

The ac–analysis and 2D DC–sweeps can be performed very fast and efficiently in EDA environments like Cadence Spectre. Moreover, they can be set up with very few steps to achieve the desired level of accuracy for the derivation of the $g_{itj}^{k\ell}$–coefficients. Thus, the overall speed of the proposed method is not compromised.

1.3.1 AC–Analysis for Amplitude Levels Estimation

An ac–analysis is initially performed to the complete circuit under consideration, to gain knowledge about the expected signal amplitude at the input and the output of each stage.

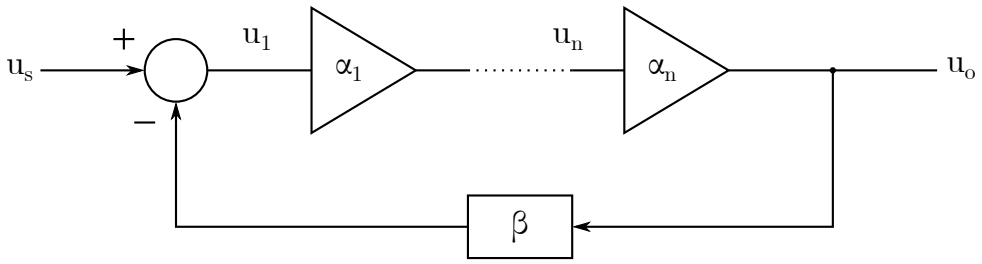

Figure 1.13: Closed–loop system configuration.

The input and output amplitudes of a stage with respect to the circuit's input signal can deviate from an anticipated monotonous drop in open–loop applications as frequency rises. When the circuit is in closed–loop configuration, the maximum value may be achieved at higher frequencies. In the system representation of Figure 1.13, the gain from the input signal, u_s, to the input of the first stage, u_1, is

$$\frac{u_1}{u_s} = \frac{1}{1 + \beta\alpha_1 \cdots \alpha_n}. \tag{1.13}$$

[4]If the input signal source drives a CG stage, R_0 must be significantly smaller in value than the input impedance of the stage.

As the gain of each stage falls with frequency, the gain to the input of the first stage rises, and so does its input amplitude. Depending on the gains $\alpha_1, \ldots, \alpha_n$, and whether additional feedback exists, more stages can exhibit similar behavior.

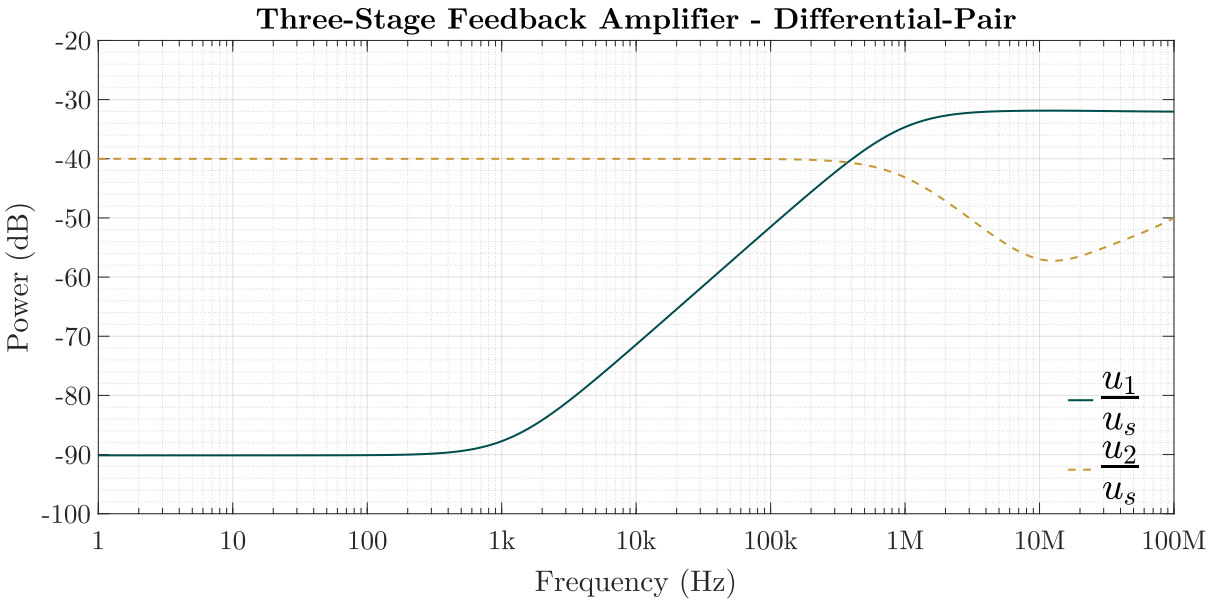

Figure 1.14: Gains u_1/u_s and u_2/u_s for the differential–pair.

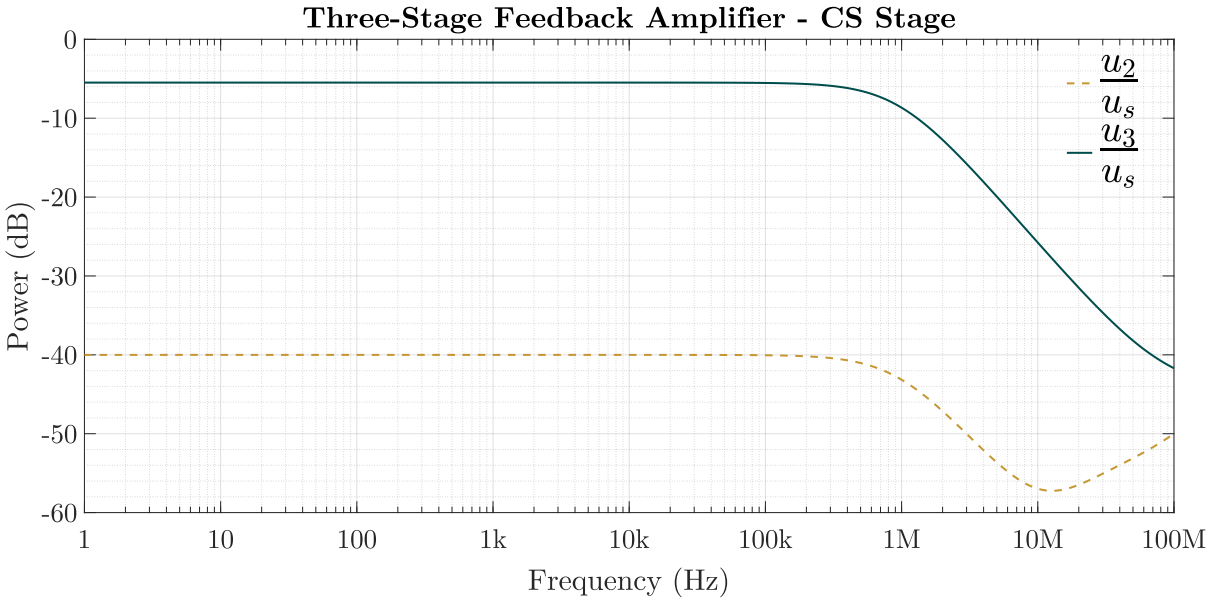

Figure 1.15: Gains u_2/u_s and u_3/u_s for the CS stage.

Figures 1.14 and 1.15 depict the gains u_1/u_s, u_2/u_s and u_3/u_s, for the differential–pair and the CS stage, respectively, of the feedback amplifier of Figure 1.11. Let the differential–pair's differential input voltage be denoted by u_1 and its output voltage

by u_2; accordingly, the CS stage has u_2 as input voltage and u_3 as output voltage. Whereas both gains reach their maximum value at low frequencies in the CS stage, the gain of the input of the differential–pair starts to rise and reaches its peak higher in frequency, but well inside the amplifier's unity–gain bandwidth of 16.80 MHz. Simulations were done again with Cadence Spectre in TSMC 0.18 µm technology.

1.3.2 2D DC–Sweeps for Current–Characteristics

The derived maximum values (within the bandwidth of interest for the distortion estimation), when referred back to the excitation signal, mark the peak amplitudes that the input and the output of a stage will confront. As such, they are the ranges for the 2D DC–sweep required to capture the dependence of the stage's output current on its input and output voltages.

Each stage is set to its input and output DC–operating points, and a 2D DC–sweep of its output current is preformed under no load; the two sweeping parameters are the input and output voltages, with r_1 and r_2 number of steps, respectively.

1.3.3 Model Coefficients Extraction via Linear Regression

After all 2D DC–sweeps are completed, the acquired data have to be processed in an appropriate way to derive each stage's $g_{itj}^{k\ell}$–coefficients. A linear regression approach is used, in the form of a linear least–squares problem [36]

$$I_g = UG + I_\varepsilon. \tag{1.14}$$

The matrices $U \in \mathbb{R}^{(r_1 \cdot r_2)\times 9}$ and $G \in \mathbb{R}^{9\times 1}$ are defined as

$$U = \left[\widetilde{u}_{itj},\ \widetilde{u}_{itj}^2,\ \widetilde{u}_{itj}^3,\ u_j,\ u_j^2,\ u_j^3,\ \widetilde{u}_{itj}u_j,\ \widetilde{u}_{itj}^2u_j,\ \widetilde{u}_{itj}u_j^2\right] \tag{1.15}$$

$$G = \left[g_{itj}^{10},\ g_{itj}^{20},\ g_{itj}^{30},\ g_{itj}^{01},\ g_{itj}^{02},\ g_{itj}^{03},\ g_{itj}^{11},\ g_{itj}^{21},\ g_{itj}^{12}\right]^\top \tag{1.16}$$

forming (1.8) for all the values of the stage's output current, embodied in $I_g \in \mathbb{R}^{(r_1 \cdot r_2)\times 1}$. The column matrix $I_\varepsilon \in \mathbb{R}^{(r_1 \cdot r_2)\times 1}$ accounts for the error between the current values obtained by simulation (I_g) and the ones resulting from UG.

For normalization purposes, and to ensure a robust solution, a scaling is introduced in (1.14) by means of a diagonal matrix, D,

$$I_g = UD^{-1}DG + I_\varepsilon \tag{1.17}$$

$$D = \operatorname{diag}(\delta_1, \ldots, \delta_9) \in \mathbb{R}^{9\times 9} \tag{1.18}$$

where δ_i is the Euclidean norm [37] of the i–th column of U. The solution yielding

the estimation of the $g_{itj}^{k\ell}$–coefficients is

$$G = D^{-1}\left[\left(UD^{-1}\right)^{\top} UD^{-1}\right]^{-1}\left(UD^{-1}\right)^{\top} I_g. \tag{1.19}$$

1.3.4 Weakly Nonlinear G_m–Stage Behavior Criteria

Although it is not always trivial to confirm that a circuit operates under weak nonlinearities *a priori* [8], it is possible to practically confirm such an operation, subjected to certain bounds. Useful insight can be gained by the following two criteria.

Criterion 1

First, the accuracy of the least–squares fit to the simulation current values of a G_m–stage is evaluated by the bounded ratio

$$\frac{\|I_\varepsilon\|_1}{\|I_g\|_1} = \frac{\|I_g - UG\|_1}{\|I_g\|_1} \leq b_I \tag{1.20}$$

where $\|\cdot\|_1$ denotes the 1–norm [37], and $b_I > 0$.

This ratio must be small in order to confirm a good fit. As such, the value of b_I can be adjusted to meet the desired level of accuracy. In the example cases of Section 1.5, a value of b_I in the order of 10^{-4} was found to yield accurate fitting.

Criterion 2

After a fit with good accuracy is confirmed, the normalized magnitudes of the nonlinear terms of (1.8) are considered. Let

$$E(\widetilde{u}_{itj}, u_j) = \begin{bmatrix} \left|g_{itj}^{10}\widetilde{u}_{itj}\right| & \left|g_{itj}^{20}\widetilde{u}_{itj}^2\right| & \left|g_{itj}^{30}\widetilde{u}_{itj}^3\right| \\ \left|g_{itj}^{01}u_j\right| & \left|g_{itj}^{02}u_j^2\right| & \left|g_{itj}^{03}u_j^3\right| \\ \left|g_{itj}^{11}\widetilde{u}_{itj}u_j\right| & \left|g_{itj}^{21}\widetilde{u}_{itj}^2u_j\right| & \left|g_{itj}^{12}\widetilde{u}_{itj}u_j^2\right| \end{bmatrix} \in \mathbb{R}^{3\times 3} \tag{1.21}$$

$$\overline{E} = \frac{1}{\left|g_{itj}^{10}\widetilde{u}_{itj}^{\max}\right|} E(\widetilde{u}_{itj}^{\max}, u_j^{\max}) \in \mathbb{R}^{3\times 3} \tag{1.22}$$

where it is assumed that the dominant linear term of (1.8) is $g_{itj}^{10}\widetilde{u}_{itj}$, and the maximum values $\widetilde{u}_{itj}^{\max}$ and $u_j^{\max}$ are taken from the 2D DC–sweep ranges of the G_m–stage.

The entries of $\overline{E}$ that correspond to the normalized nonlinear terms of (1.8) can be bounded by $b_g^{n\ell} > 0$, to ensure that the dominant linear term, $g_{itj}^{10}\widetilde{u}_{itj}$, is at least $1/b_g^{n\ell}$ times stronger over the entire input and output voltage ranges. A value of $b_g^{n\ell}$ in the order of 10^{-1} was found to be reasonable, especially for a stage where $u_j^{\max} \gg \widetilde{u}_{itj}^{\max}$.

1.3.5 Coefficients Derivation Example

As an example, the coefficients of the CS stage of Figure 1.11 are derived, assuming a sinusoidal signal of 25 mV peak at the input of the amplifier. For such an input, Figure 1.16 presents the 2D DC–sweep's resulting output current as a function of the input and output voltages of the stage. The coefficients are gathered in Table 1.1. In this example, it is $b_I = 5.4701 \cdot 10^{-4}$ and $b_g^{n\ell} = 4.1485 \cdot 10^{-1}$.

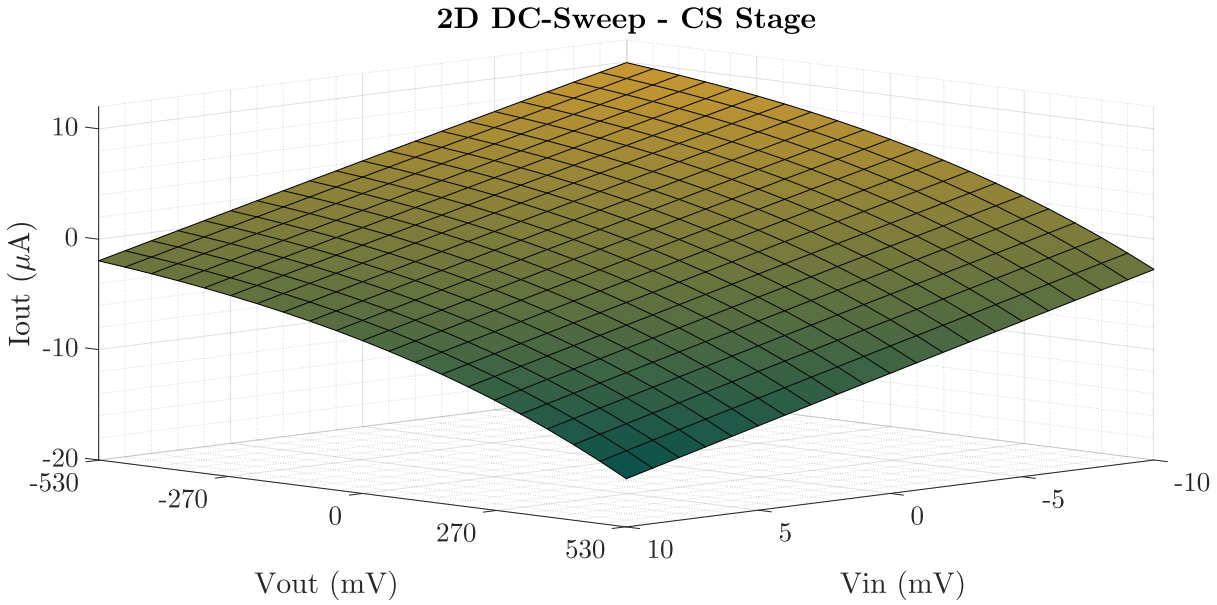

Figure 1.16: 2D DC–sweep of the CS stage's output current.

Table 1.1: CS stage $g_{1r2}^{k\ell}$–coefficients.

Coefficient	Value	Units
g_{1r2}^{10}	$-6.0841 \cdot 10^{-4}$	A/V
g_{1r2}^{20}	$-6.7874 \cdot 10^{-4}$	A/V^2
g_{1r2}^{30}	$+4.1772 \cdot 10^{-4}$	A/V^3
g_{1r2}^{01}	$-1.1433 \cdot 10^{-5}$	A/V
g_{1r2}^{02}	$-8.9247 \cdot 10^{-6}$	A/V^2
g_{1r2}^{03}	$-3.3726 \cdot 10^{-6}$	A/V^3
g_{1r2}^{11}	$-4.5296 \cdot 10^{-5}$	A/V^2
g_{1r2}^{21}	$-6.3003 \cdot 10^{-6}$	A/V^3
g_{1r2}^{12}	$-3.9418 \cdot 10^{-5}$	A/V^3

1.4 Harmonic Distortion Estimation

Consider the general circuit structure of Figure 1.17. The topology is composed of G_m–stages, resistors and capacitors. Each node j, $j = 0, 1, \ldots, n$, may feature a resistor, R_j, and a capacitor, C_j, connected to ground. It can also have an excitation signal, as an independent current source, $\hat{i}_j$. The G_m–stages behave as described in Section 1.2, while capacitor $\widetilde{C}_{\ell j}$ provides coupling between nodes ℓ and j, with

$$i_{\widetilde{C}_{\ell j}} = \widetilde{C}_{\ell j}\left(\dot{u}_\ell - \dot{u}_j\right) = -i_{\widetilde{C}_{j\ell}}. \tag{1.23}$$

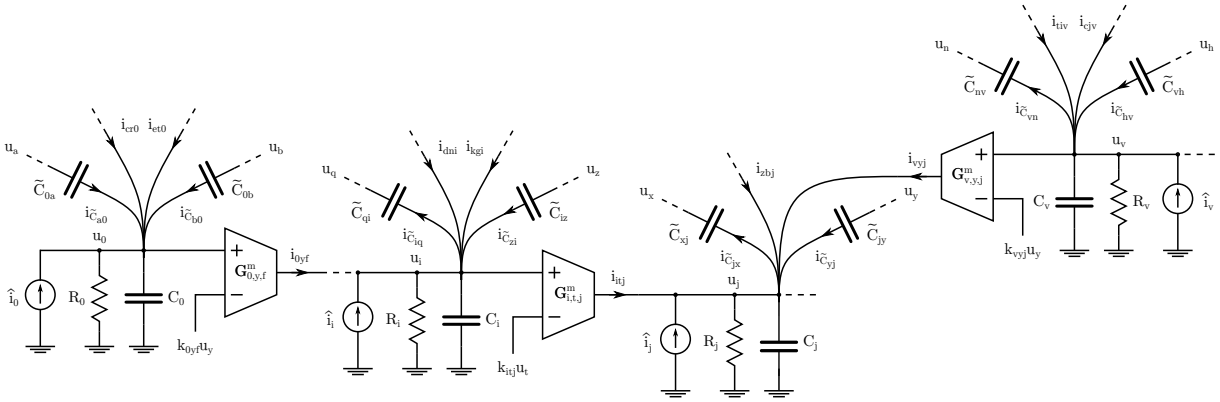

Figure 1.17: General circuit structure, composed of G_m–stages.

For each node j, it holds

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} i_{\widetilde{C}_{\ell j}} = \frac{u_j}{R_j} + C_j \dot{u}_j \tag{1.24}$$

and by using (1.23)

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} \widetilde{C}_{\ell j}\dot{u}_\ell = \frac{u_j}{R_j} + \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j}\right)\dot{u}_j. \tag{1.25}$$

Equation (1.25) constitutes a manipulated form of the state–space equation of the general form $C^c \dot{u} = G^c u + \hat{I}$, where C^c and G^c are the corresponding capacitance and conductance matrices of the whole circuit.

Assuming that the circuit operates in steady–state, let the voltage of node j be of the form (recall that only harmonics up to the third are considered)

$$u_j = u_j^f + u_j^h \tag{1.26}$$

$$u_j^f = \theta^f S_j^f \tag{1.27}$$

$$u_j^h = \theta^h S_j^h \tag{1.28}$$

where[5]

$$S_j^f = \left[a_{j,1},\ b_{j,1}\right]^\top \in \mathbb{R}^{2\times 1} \tag{1.29}$$
$$S_j^h = \left[a_{j,2},\ b_{j,2},\ a_{j,3},\ b_{j,3}\right]^\top \in \mathbb{R}^{4\times 1} \tag{1.30}$$
$$\theta^f = \left[\sin\omega t,\ \cos\omega t\right] \in \mathbb{R}^{1\times 2} \tag{1.31}$$
$$\theta^h = \left[\sin 2\omega t,\ \cos 2\omega t,\ \sin 3\omega t,\ \cos 3\omega t\right] \in \mathbb{R}^{1\times 4}. \tag{1.32}$$

Terms u_j^f and u_j^h represent the voltage components of the fundamental and the harmonic tones, respectively, while vectors S_j^f and S_j^h feature the corresponding sin and cos coefficients.

In the same vein, for the excitation current source of node j it is

$$\hat{i}_j = \hat{i}_j^f + \hat{i}_j^h \tag{1.33}$$
$$\hat{i}_j^f = \theta^f P_j^f \tag{1.34}$$
$$\hat{i}_j^h = \theta^h P_j^h \tag{1.35}$$

where

$$P_j^f = \left[\hat{a}_{j,1},\ \hat{b}_{j,1}\right]^\top \in \mathbb{R}^{2\times 1} \tag{1.36}$$
$$P_j^h = \left[\hat{a}_{j,2},\ \hat{b}_{j,2},\ \hat{a}_{j,3},\ \hat{b}_{j,3}\right]^\top \in \mathbb{R}^{4\times 1}. \tag{1.37}$$

In the following analysis it has been assumed that the circuit features only one excitation source, that of node 0.

The proposed harmonic distortion estimation method is performed in two steps. First, the fundamental tone of ω is estimated, followed by the estimation of the harmonic tones of 2ω and 3ω, to finally derive HD_2 and HD_3.

1.4.1 Fundamental Tone Estimation

Since weak nonlinearities are assumed, their contribution to the fundamental tone can be considered negligible. Thus, the fundamental tone voltage component of node j, (1.27), should satisfy the linear part of (1.25). As such, for the fundamental tone estimation, the output current, i_{itj}^f, of stage $G_{i,t,j}^m$, is expressed using (1.3) and (1.27) as

[5] Vectors θ^f and θ^h are functions of time, so a more appropriate notation would be that of $\theta^f(t)$ and $\theta^h(t)$; time is omitted for simplicity.

only the linear part of (1.8)

$$i^f_{itj} = \theta^f \left(g^{10}_{itj} S^f_i - g^{10}_{itj} k_{itj} S^f_t + g^{01}_{itj} S^f_j \right). \tag{1.38}$$

That is, a G_m–stage's output current is the sum of three independent ones, each one linearly dependent on the fundamental tone voltage component of its corresponding node.

The expression of i^f_{itj} can be used to form a system of equations for the fundamental tone coefficients of the complete circuit under consideration, relying on (1.25). Let

$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \in \mathbb{R}^{2\times 2}. \tag{1.39}$$

Then, it is

$$i u^f_j = \dot{\theta}^f S^f_j = \omega \theta^f J S^f_j. \tag{1.40}$$

Combining (1.38) and (1.40) with (1.25) results in

$$\theta^f \left[P^f_j + \sum_{i,t} \left(g^{10}_{itj} S^f_i - g^{10}_{itj} k_{itj} S^f_t + g^{01}_{itj} S^f_j \right) + \sum_{\ell} \widetilde{C}_{\ell j} \omega J S^f_\ell \right] = \theta^f \left[\frac{1}{R_j} S^f_j + \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) \omega J S^f_j \right]. \tag{1.41}$$

The vector function θ^f consists of two linearly independent functions of time, and embodies two independent equations with respect to the coefficients of $\sin \omega t$ and $\cos \omega t$. So, θ^f can be eliminated for (1.41) to hold for any $t \in \mathbb{R}$. Reordering terms yields

$$P^f_j + \sum_{i,t} g^{10}_{itj} S^f_i - \sum_{i,t} g^{10}_{itj} k_{itj} S^f_t + \omega \sum_{\ell} \widetilde{C}_{\ell j} J S^f_\ell = \left(\frac{1}{R_j} - \sum_{i,t} g^{01}_{itj} \right) S^f_j + \omega \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) J S^f_j. \tag{1.42}$$

Consider the vector of the fundamental tone coefficients of all voltages

$$S^f = \left[\left(S^f_0 \right)^\top, \left(S^f_1 \right)^\top, \ldots, \left(S^f_n \right)^\top \right]^\top \in \mathbb{R}^{2(n+1)\times 1} \tag{1.43}$$

and that of the excitation current source[6]

$$P^f = \left[\left(P^f_0 \right)^\top, \left(0,\ 0 \right), \ldots, \left(0,\ 0 \right) \right]^\top \in \mathbb{R}^{2(n+1)\times 1}. \tag{1.44}$$

Then, the equivalent of (1.42) for the whole circuit structure is constructed in a

[6] If more than one excitation signals are present, they should be included in the corresponding entries of the vector.

block–matrix form

$$P^f + \left(G^f + K^f + \omega F^f\right) S^f = \left(T^f + \omega W^f\right) S^f \tag{1.45}$$

where

$$G^f = \left[\sum_t g^{10}_{itj}\right]^n_{j,i=0} \otimes I_2 \in \mathbb{R}^{2(n+1)\times 2(n+1)} \tag{1.46}$$

$$K^f = \left[-\sum_i g^{10}_{itj} k_{itj}\right]^n_{j,t=0} \otimes I_2 \in \mathbb{R}^{2(n+1)\times 2(n+1)} \tag{1.47}$$

$$F^f = \left[\widetilde{C}_{\ell j}\right]^n_{j,\ell=0} \otimes J \in \mathbb{R}^{2(n+1)\times 2(n+1)} \tag{1.48}$$

$$T^f = \operatorname{diag}\left(\left[\tfrac{1}{R_j} - \sum_{i,t} g^{01}_{itj}\right]^n_{j=0}\right) \otimes I_2 \in \mathbb{R}^{2(n+1)\times 2(n+1)} \tag{1.49}$$

$$W^f = \operatorname{diag}\left(\left[C_j + \sum_\ell \widetilde{C}_{\ell j}\right]^n_{j=0}\right) \otimes J \in \mathbb{R}^{2(n+1)\times 2(n+1)}. \tag{1.50}$$

In (1.46)–(1.50), $\otimes$ denotes the Kronecker's product [37], and I_n is the $n \times n$ identity matrix. The vector of the fundamental tone coefficients is the solution of (1.45)

$$S^f = \left[T^f - G^f - K^f + \omega\left(W^f - F^f\right)\right]^{-1} P^f. \tag{1.51}$$

1.4.2 Harmonic Tones Estimation

The harmonic tones voltage components of node j, (1.28), are generated by the nonlinear terms of (1.8). Including all voltage terms in the form of (1.26) and computing all produced terms would result in cumbersome expressions that constitute a nonlinear equality problem. Even though this approach yields the exact algebraic solution, it is neither easy to implement nor computationally efficient.

A close inspection of (1.8), in association with (1.26), reveals that the generated coefficients of the second and third harmonic tones due to the nonlinear terms of (1.8) will eventually be a sum of products of

(a) only fundamental tone coefficients,

(b) a single harmonic tone coefficient to the power of one and one or more fundamental tone coefficients,

(c) higher orders or products of harmonic tones coefficients.

Since the amplitudes of the harmonic tones are expected to be much smaller than that of the fundamental tone, products involving two or more harmonic tones coefficients or powers of them are negligible and can be safely ignored. This approximation can be validated after the estimation of the harmonic tones, as demonstrated in Section 1.4.3.

Based on the above and including the linear part of (1.8), the output current, i^h_{itj}, of stage $G^m_{i,t,j}$, can be approximated, using (1.3) and (1.28), by

$$i^h_{itj} = \theta^h \left[g^{10}_{itj} S^h_i - g^{10}_{itj} k_{itj} S^h_t + g^{01}_{itj} S^h_j + Z_{itj} + X^\alpha_{itj} S^h_i + X^\beta_{itj} S^h_t + X^\gamma_{itj} S^h_j \right] \tag{1.52}$$

where the term $\theta^h Z_{itj}$ is the sum of the products (a), and the term $\theta^h \left(X^\alpha_{itj} S^h_i + X^\beta_{itj} S^h_t + X^\gamma_{itj} S^h_j \right)$ is the sum of the products (b). Note that the approximate expression of i^h_{itj} is linear to the corresponding harmonic tones coefficients.

The term Z_{itj} is expressed as

$$Z_{itj} = \left[p^{s2}_{itj},\ p^{c2}_{itj},\ p^{s3}_{itj},\ p^{c3}_{itj} \right]^\top \in \mathbb{R}^{4\times 1} \tag{1.53}$$

where

$$p^{s2}_{itj} = g^{20}_{itj} \widetilde{f}^{s2}_{itj} + g^{02}_{itj} f^{s2}_j + g^{11}_{itj} h^{s2}_{itj} \tag{1.54}$$
$$p^{c2}_{itj} = g^{20}_{itj} \widetilde{f}^{c2}_{itj} + g^{02}_{itj} f^{c2}_j + g^{11}_{itj} h^{c2}_{itj} \tag{1.55}$$
$$p^{s3}_{itj} = g^{30}_{itj} \widetilde{f}^{s3}_{itj} + g^{03}_{itj} f^{s3}_j + g^{21}_{itj} r^{s3}_{iij} + g^{12}_{itj} o^{s3}_{itj} \tag{1.56}$$
$$p^{c3}_{itj} = g^{30}_{itj} \widetilde{f}^{c3}_{itj} + g^{03}_{itj} f^{c3}_j + g^{21}_{itj} r^{c3}_{itj} + g^{12}_{itj} o^{c3}_{itj}. \tag{1.57}$$

Furthermore, matrices $X^\alpha_{itj} \in \mathbb{R}^{4\times 4}$, $X^\beta_{itj} \in \mathbb{R}^{4\times 4}$ and $X^\gamma_{itj} \in \mathbb{R}^{4\times 4}$ are defined as

$$X^\alpha_{itj} = g^{20}_{itj} \widetilde{N}_{itj} + g^{30}_{itj} \frac{3}{2} \widetilde{M}_{itj} + g^{11}_{itj} \frac{1}{2} N_j + g^{21}_{itj} Q_{itj} + g^{12}_{itj} \frac{1}{2} M_j \tag{1.58}$$
$$X^\beta_{itj} = -k_{itj} X^\alpha_{itj} \tag{1.59}$$
$$X^\gamma_{itj} = g^{02}_{itj} N_j + g^{03}_{itj} \frac{3}{2} M_j + g^{11}_{itj} \frac{1}{2} \widetilde{N}_{itj} + g^{21}_{itj} \frac{1}{2} \widetilde{M}_{itj} + g^{12}_{itj} Q_{itj}. \tag{1.60}$$

The quantities forming (1.54)–(1.60) can be found in the Appendix and are omitted from this part of the text for better comprehension of the method's steps.

Expression (1.52) is now used to form a system of equations for the harmonic tones coefficients, based again on (1.25). To this end, let

$$L = \begin{bmatrix} 2 & 0 \\ 0 & 3 \end{bmatrix} \in \mathbb{R}^{2\times 2} \tag{1.61}$$

and express

$$\dot{u}^h_j = \dot{\theta}^h S^h_j = \omega \theta^h \left(L \otimes J \right) S^h_j. \tag{1.62}$$

The combination of (1.52) and (1.62) with (1.25) yields

$$\theta^h \left[P_j^h + \sum_{i,t} \left(g_{itj}^{10} S_i^h - g_{itj}^{10} k_{itj} S_t^h + g_{itj}^{01} S_j^h + Z_{itj} + X_{itj}^{\alpha} S_i^h + X_{itj}^{\beta} S_t^h + X_{itj}^{\gamma} S_j^h \right) + \sum_{\ell} \widetilde{C}_{\ell j} \omega \left(L \otimes J \right) S_{\ell}^h \right] = \theta^h \left[\frac{1}{R_j} S_j^h + \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) \omega \left(L \otimes J \right) S_j^h \right]. \tag{1.63}$$

The vector function θ^h consists of four linearly independent functions of time, implying four equations of the coefficients of $\sin 2\omega t$, $\cos 2\omega t$, $\sin 3\omega t$ and $\cos 3\omega t$. Eliminating θ^h and reordering terms results in

$$\left(P_j^h + \sum_{i,t} Z_{itj} \right) + \sum_{i,t} g_{itj}^{10} S_i^h - \sum_{i,t} g_{itj}^{10} k_{itj} S_t^h + \sum_{i,t} \left(X_{itj}^{\alpha} S_i^h + X_{itj}^{\beta} S_t^h + X_{itj}^{\gamma} S_j^h \right) + \omega \sum_{\ell} \widetilde{C}_{\ell j} \left(L \otimes J \right) S_{\ell}^h = \left(\frac{1}{R_j} - \sum_{i,t} g_{itj}^{01} \right) S_j^h + \omega \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) \left(L \otimes J \right) S_j^h. \tag{1.64}$$

Let the vector of the harmonic tones coefficients of all voltages of the circuit be

$$S^h = \left[\left(S_0^h \right)^{\top}, \left(S_1^h \right)^{\top}, \ldots, \left(S_n^h \right)^{\top} \right]^{\top} \in \mathbb{R}^{2(n+1)\times 1} \tag{1.65}$$

and consider the vector $P^h \in \mathbb{R}^{4(n+1)\times 1}$ of the excitation current source[7]

$$P^h = \left[\left(P_0^h \right)^{\top}, \left(0,\ 0,\ 0,\ 0 \right), \ldots, \left(0,\ 0,\ 0,\ 0 \right) \right]^{\top}. \tag{1.66}$$

Moreover, let the vector

$$B^h = P^h + Z^h \in \mathbb{R}^{4(n+1)\times 1} \tag{1.67}$$

where

$$Z^h = \left[\sum_{i,t} Z_{itj} \right]_{j=0}^{n} \in \mathbb{R}^{4(n+1)\times 1}. \tag{1.68}$$

Then, equation (1.64) is written in block–matrix form

$$B^h + \left(G^h + K^h + X^h + \omega F^h \right) S^h = \left(T^h + \omega W^h \right) S^h \tag{1.69}$$

where

$$G^h = G^f \otimes I_2 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.70}$$

$$K^h = K^f \otimes I_2 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.71}$$

[7] In the case of more than one excitation signals being present, they should be added at the corresponding entries of the vector.

$$F^h = \left[\widetilde{C}_{\ell j}\right]_{j,\ell=0}^{n} \otimes (L \otimes J) \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.72}$$

$$T^h = T^f \otimes I_2 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.73}$$

$$W^h = \operatorname{diag}\left(\left[C_j + \textstyle\sum_\ell \widetilde{C}_{\ell j}\right]_{j=0}^{n}\right) \otimes (L \otimes J) \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.74}$$

$$X^h = \left[\textstyle\sum_t X_{itj}^{\alpha}\right]_{j,i=0}^{n} + \left[\textstyle\sum_i X_{itj}^{\beta}\right]_{j,t=0}^{n} + \bigoplus_{j=0}^{n}\left[\textstyle\sum_{i,t} X_{itj}^{\gamma}\right] \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{1.75}$$

and $\bigoplus$ denotes the direct sum of matrices [38].

The solution of (1.69) gives the vector of the harmonic tones coefficients

$$S^h = \left[T^h - G^h - K^h - X^h + \omega\left(W^h - F^h\right)\right]^{-1} B^h. \tag{1.76}$$

The solution of (1.51) and (1.76) can be easily calculated, making the speed and computational efficiency of the proposed method superior to that of traditional distortion estimation via simulation.

Since all coefficients are known, the desired HD_2 and HD_3 factors can be immediately obtained for any node j of the circuit

$$HD_2^j = 10\log_{10}\left(\frac{a_{j,2}^2 + b_{j,2}^2}{a_{j,1}^2 + b_{j,1}^2}\right) \tag{1.77}$$

$$HD_3^j = 10\log_{10}\left(\frac{a_{j,3}^2 + b_{j,3}^2}{a_{j,1}^2 + b_{j,1}^2}\right). \tag{1.78}$$

For a differential output, between nodes j and m, the distortion factors are given by

$$HD_2^{jm} = 10\log_{10}\left[\frac{\left(a_{j,2} - a_{m,2}\right)^2 + \left(b_{j,2} - b_{m,2}\right)^2}{\left(a_{j,1} - a_{m,1}\right)^2 + \left(b_{j,1} - b_{m,1}\right)^2}\right] \tag{1.79}$$

$$HD_3^{jm} = 10\log_{10}\left[\frac{\left(a_{j,3} - a_{m,3}\right)^2 + \left(b_{j,3} - b_{m,3}\right)^2}{\left(a_{j,1} - a_{m,1}\right)^2 + \left(b_{j,1} - b_{m,1}\right)^2}\right]. \tag{1.80}$$

1.4.3 Harmonic Tones Approximation Error Evaluation

The assumption regarding the amplitudes of the harmonic tones that led to the elimination of the products (c) in Section 1.4.2 can be validated retrospectively after the solution of (1.51) and (1.76). To this end, consider the error excitation current source of stage $G_{i,t,j}^m$

$$\hat{i}_{itj}^{\varepsilon} = \theta^h \hat{P}_{itj}^{\varepsilon} = \theta^h \left[\hat{a}_{itj,2}^{\varepsilon},\ 0,\ \hat{a}_{itj,3}^{\varepsilon},\ 0\right]^{\top} \tag{1.81}$$

where $\hat{P}^{\varepsilon}_{itj} \in \mathbb{R}^{4\times 1}$ has the same form as (1.37) and

$$\begin{aligned}\hat{a}^{\varepsilon}_{itj,2} &= \left|g^{30}_{itj}\right|\left(\frac{3}{2}\widetilde{c}_{itj}\widetilde{d}^{2}_{itj}+\frac{9}{4}\widetilde{d}^{3}_{itj}\right)+\left|g^{03}_{itj}\right|\left(\frac{3}{2}c_j d_j^2+\frac{9}{4}d_j^3\right)\\ &+\left|g^{21}_{itj}\right|\left(\frac{1}{2}c_j\widetilde{d}^{2}_{itj}+\widetilde{c}_{itj}\widetilde{d}_{itj}d_j+\frac{9}{4}\widetilde{d}^{2}_{itj}d_j\right)+\left|g^{12}_{itj}\right|\left(\frac{1}{2}\widetilde{c}_{itj}d_j^2+c_j\widetilde{d}_{itj}d_j+\frac{9}{4}\widetilde{d}_{itj}d_j^2\right) \qquad (1.82)\\ \hat{a}^{\varepsilon}_{itj,3} &= \left|g^{30}_{itj}\right|\left(\frac{3}{4}\widetilde{c}_{itj}\widetilde{d}^{2}_{itj}+\frac{9}{4}\widetilde{d}^{3}_{itj}\right)+\left|g^{03}_{itj}\right|\left(\frac{3}{4}c_j d_j^2+\frac{9}{4}d_j^3\right)\\ &+\left|g^{21}_{itj}\right|\left(\frac{1}{4}c_j\widetilde{d}^{2}_{itj}+\frac{1}{2}\widetilde{c}_{itj}\widetilde{d}_{itj}d_j+\frac{9}{4}\widetilde{d}^{2}_{itj}d_j\right)+\left|g^{12}_{itj}\right|\left(\frac{1}{4}\widetilde{c}_{itj}d_j^2+\frac{1}{2}c_j\widetilde{d}_{itj}d_j+\frac{9}{4}\widetilde{d}_{itj}d_j^2\right). \qquad (1.83)\end{aligned}$$

The coefficients involved in (1.82) and (1.83) are the maximum amplitude values of the fundamental and any harmonic tone at the input and the output of stage $G^{m}_{i,t,j}$, over the entire frequency range of interest, evaluated as

$$\widetilde{c}_{itj} = \max\left\{\sqrt{\widetilde{a}^{2}_{itj,1}+\widetilde{b}^{2}_{itj,1}}\right\} \qquad (1.84)$$

$$c_j = \max\left\{\sqrt{a^{2}_{j,1}+b^{2}_{j,1}}\right\} \qquad (1.85)$$

$$\widetilde{d}_{itj} = \max\left\{\sqrt{\widetilde{a}^{2}_{itj,2}+\widetilde{b}^{2}_{itj,2}}, \sqrt{\widetilde{a}^{2}_{itj,3}+\widetilde{b}^{2}_{itj,3}}\right\} \qquad (1.86)$$

$$d_j = \max\left\{\sqrt{a^{2}_{j,2}+b^{2}_{j,2}}, \sqrt{a^{2}_{j,3}+b^{2}_{j,3}}\right\} \qquad (1.87)$$

where

$$\widetilde{a}_{itj,1} = a_{i,1} - k_{itj}a_{t,1} \qquad (1.88)$$

$$\widetilde{b}_{itj,1} = b_{i,1} - k_{itj}b_{t,1} \qquad (1.89)$$

$$\widetilde{a}_{itj,2} = a_{i,2} - k_{itj}a_{t,2} \qquad (1.90)$$

$$\widetilde{b}_{itj,2} = b_{i,2} - k_{itj}b_{t,2} \qquad (1.91)$$

$$\widetilde{a}_{itj,3} = a_{i,3} - k_{itj}a_{t,3} \qquad (1.92)$$

$$\widetilde{b}_{itj,3} = b_{i,3} - k_{itj}b_{t,3}. \qquad (1.93)$$

The current of (1.81) is injected into the output node, j, of stage $G^{m}_{i,t,j}$, while no other input is present in the circuit under consideration. The expression of $\hat{i}^{\varepsilon}_{itj}$ accounts for the products (c) that would have been generated by the nonlinear terms of (1.8). Its magnitude is an overestimation of the induced error in the estimation of the harmonic tones by (1.76); the maximum values of (1.84)–(1.87) may not be an input–output corresponding pair in frequency, and may also result from a combination of both harmonic tones. Furthermore, the involved $g^{k\ell}_{itj}$–coefficients are summed in absolute–value fashion, while they may feature opposite signs.

The harmonic tones coefficients due to the error current source of stage $G^m_{i,t,j}$ are given by the solution of

$$S^{h,\varepsilon}_{itj} = \left[T^h - G^h - K^h + \omega\left(W^h - F^h\right)\right]^{-1} P^{h,\varepsilon}_{itj} \tag{1.94}$$

where

$$P^{h,\varepsilon}_{itj} = \Big[\Big(0,\ 0,\ 0,\ 0\Big),\ \ldots,\ \overbrace{\Big(\hat{a}^{\varepsilon}_{itj,2},\ 0,\ \hat{a}^{\varepsilon}_{itj,3},\ 0\Big)}^{\text{node } j},\ \ldots,\ \Big(0,\ 0,\ 0,\ 0\Big)\Big]^{\top} \in \mathbb{R}^{4(n+1)\times 1}. \tag{1.95}$$

This procedure is repeated for all G_m–stages of the circuit, and a total error estimation is obtained by summing the absolute coefficient values of all $S^{h,\varepsilon}_{itj} \in \mathbb{R}^{4(n+1)\times 1}$ vectors

$$S^{h,\varepsilon} = \sum_{itj} \Big[\left|a^{\varepsilon}_{0,2}\right|,\ \left|b^{\varepsilon}_{0,2}\right|,\ \left|a^{\varepsilon}_{0,3}\right|,\ \left|b^{\varepsilon}_{0,3}\right|,\ \left|a^{\varepsilon}_{1,2}\right|,\ \left|b^{\varepsilon}_{1,2}\right|,\ \left|a^{\varepsilon}_{1,3}\right|,\ \left|b^{\varepsilon}_{1,3}\right|,\ \ldots,$$
$$\ldots,\ \left|a^{\varepsilon}_{n,2}\right|,\ \left|b^{\varepsilon}_{n,2}\right|,\ \left|a^{\varepsilon}_{n,3}\right|,\ \left|b^{\varepsilon}_{n,3}\right|\Big]^{\top} \in \mathbb{R}^{4(n+1)\times 1}. \tag{1.96}$$

Again, this constitutes an overestimation of the total propagated error, since (1.96) supposes all calculated coefficients to be in phase at every node of the circuit.

The final step to validate the harmonic tones approximation is to compare the power of the second and the third harmonic estimated by (1.76) to the power of the ones resulting from (1.96), in the frequency range of interest. The power difference would indicate a pessimistic error estimation in the second and the third harmonic, and thus in HD_2 and HD_3 factors.

1.4.4 Proposed Method Application Procedure

Concluding the theoretical analysis of the harmonic distortion estimation, the application of the proposed method is summarized as Procedure 1.

Procedure 1: Proposed Harmonic Distortion Estimation Method

1: Decompose the circuit as an interconnection of CMOS stages.
2: Derive each stage's $g^{k\ell}_{itj}$–coefficients by curve–fitting, confirming the criteria of Section 1.3.4 and Section 1.3.4.
3: Replace each CMOS stage with its G_m–stage model equivalent.
4: Add all resistors and capacitors, including parasitic ones if of interest.
5: Add the circuit's excitation current source(s).
6: Form matrices (1.44)–(1.50) and solve (1.51) for the fundamental tone estimation.
7: Form matrices (1.66)–(1.75) and solve (1.76) for the harmonic tones estimation, evaluating the harmonic tones approximation of Section 1.4.2 with the procedure of Section 1.4.3.
8: Use (1.77)–(1.78) or (1.79)–(1.80) to estimate the desired HD_2 and HD_3 factors.

1.4.5 Application Examples

The application of the proposed method is illustrated via two example cases, where the necessary parameters are derived and all calculation steps are followed. The examples are continued in Section 1.5, where the estimated distortion factors are compared to that resulting by simulation, for a range of frequencies.

One–Stage Cascode Amplifier

Consider the one–stage cascode amplifier of Figure 1.18. The load, $R_L \parallel C_L$, is connected to ground via a DC–voltage of V_{OUT}^{op}, equal to the DC–voltage of the unloaded output of the amplifier.

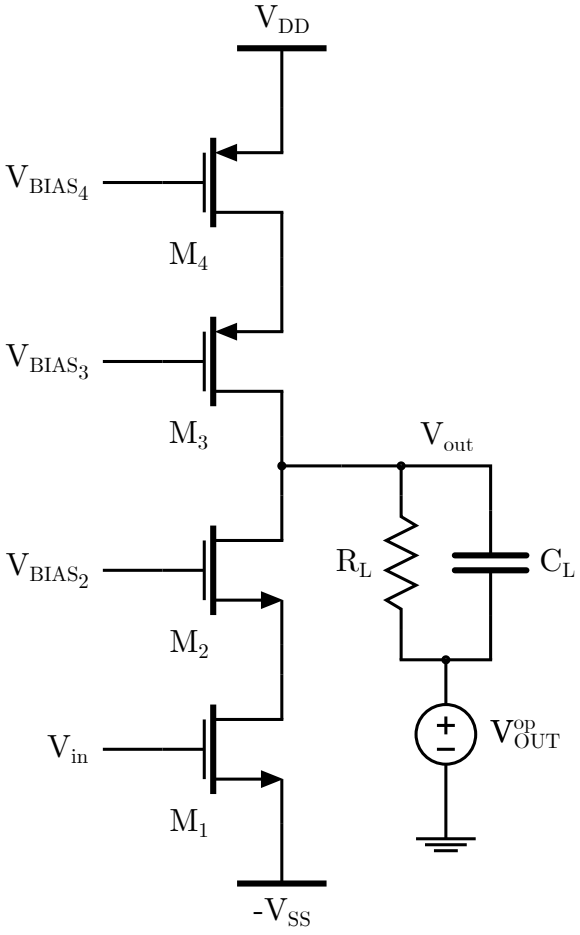

Figure 1.18: One–stage cascode amplifier.

The equivalent G_m–stage representation is shown in Figure 1.19, where the whole stage is treated as a single G_m–stage, $G_{0,r,1}^m$. The ac–input signal, $u_{in} = u_0$, is realized by $\hat{i}_0 = u_0/R_0$ acting on $R_0 = 1\,\Omega$, and $R_L = R_1$, $C_L = C_1$.

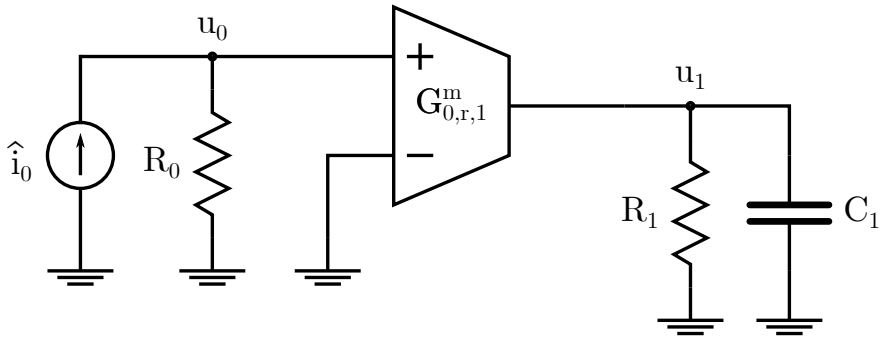

Figure 1.19: G_m–stage equivalent representation of the one–stage cascode amplifier.

Given the stage's derived $g_{0r1}^{k\ell}$–coefficients, the necessary matrices are defined according to (1.43)–(1.44) and (1.46)–(1.50)

$$S^f = \left[a_{0,1},\ b_{0,1},\ a_{1,1},\ b_{1,1}\right]^\top$$
$$P^f = \left[\hat{a}_{0,1},\ \hat{b}_{0,1},\ 0,\ 0\right]^\top$$

and

$$G^f = \begin{bmatrix} 0 & 0 \\ g_{0r1}^{10} & 0 \end{bmatrix} \otimes I_2$$
$$K^f = 0_4$$
$$F^f = 0_4$$
$$T^f = \begin{bmatrix} \frac{1}{R_0} & 0 \\ 0 & \frac{1}{R_1} - g_{0r1}^{01} \end{bmatrix} \otimes I_2$$
$$W^f = \begin{bmatrix} 0 & 0 \\ 0 & C_1 \end{bmatrix} \otimes J$$

where 0_n denotes the $n \times n$ zero matrix. Then, the solution for the fundamental tone coefficients comes directly from (1.51).

The harmonic tones coefficients vector, S^h, and the vector B^h are defined according to (1.65)–(1.68)

$$S^h = \left[a_{0,2},\ b_{0,2},\ a_{0,3},\ b_{0,3},\ a_{1,2},\ b_{1,2},\ a_{1,3},\ b_{1,3}\right]^\top$$
$$B^h = \left[\hat{a}_{0,2},\ \hat{b}_{0,2},\ \hat{a}_{0,3},\ \hat{b}_{0,3},\ p_{0r1}^{s2},\ p_{0r1}^{c2},\ p_{0r1}^{s3},\ p_{0r1}^{c3}\right]^\top$$

where the following are calculated using (1.54)–(1.57)

$$p_{0r1}^{s2} = g_{0r1}^{20}\widetilde{f}_{0r1}^{s2} + g_{0r1}^{02} f_1^{s2} + g_{0r1}^{11} h_{0r1}^{s2}$$

$$
\begin{aligned}
p_{0r1}^{c2} &= g_{0r1}^{20}\widetilde{f}_{0r1}^{c2} + g_{0r1}^{02}f_1^{c2} + g_{0r1}^{11}h_{0r1}^{c2} \\
p_{0r1}^{s3} &= g_{0r1}^{30}\widetilde{f}_{0r1}^{s3} + g_{0r1}^{03}f_1^{s3} + g_{0r1}^{21}r_{0r1}^{s3} + g_{0r1}^{12}o_{0r1}^{s3} \\
p_{0r1}^{c3} &= g_{0r1}^{30}\widetilde{f}_{0r1}^{c3} + g_{0r1}^{03}f_1^{c3} + g_{0r1}^{21}r_{0r1}^{c3} + g_{0r1}^{12}o_{0r1}^{c3}
\end{aligned}
$$

and (1.97)–(1.110) are calculated for $\widetilde{a}_{0r1,1} = a_{0,1}$, $\widetilde{b}_{0r1,1} = b_{0,1}$, $a_{1,1}$ and $b_{1,1}$. Finally, following (1.58)–(1.60) and (1.70)–(1.75), it is

$$
\begin{aligned}
G^h &= G^f \otimes I_2 \\
K^h &= 0_8 \\
F^h &= 0_8 \\
T^h &= T^f \otimes I_2 \\
W^h &= \begin{bmatrix} 0 & 0 \\ 0 & C_1 \end{bmatrix} \otimes (L \otimes J) \\
X^h &= \begin{bmatrix} 0_4 & 0_4 \\ X_{0r1}^{\alpha} & X_{0r1}^{\gamma} \end{bmatrix}
\end{aligned}
$$

where

$$
\begin{aligned}
X_{0r1}^{\alpha} &= g_{0r1}^{20}\widetilde{N}_{0r1} + g_{0r1}^{30}\frac{3}{2}\widetilde{M}_{0r1} + g_{0r1}^{11}\frac{1}{2}N_1 + g_{0r1}^{21}Q_{0r1} + g_{0r1}^{12}\frac{1}{2}M_1 \\
X_{0r1}^{\gamma} &= g_{0r1}^{02}N_1 + g_{0r1}^{03}\frac{3}{2}M_1 + g_{0r1}^{11}\frac{1}{2}\widetilde{N}_{0r1} + g_{0r1}^{21}\frac{1}{2}\widetilde{M}_{0r1} + g_{0r1}^{12}Q_{0r1}
\end{aligned}
$$

and the matrices of (1.111)–(1.115) are similarly calculated for $\widetilde{a}_{0r1,1} = a_{0,1}$, $\widetilde{b}_{0r1,1} = b_{0,1}$, $a_{1,1}$ and $b_{1,1}$. The harmonic tones solution is given by (1.76), enabling the estimation of HD_2 and HD_3 at the amplifier's output.

Three–Stage Feedback Amplifier

A more general example is given for the three–stage feedback amplifier of Figure 1.11. The application of the method on the equivalent network of Figure 1.12 yields the following matrices according to the definitions of (1.46)–(1.50)

$$
G^f = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
g_{031}^{10} & 0 & 0 & 0 & 0 \\
0 & g_{2r1}^{10} & 0 & 0 & 0 \\
0 & 0 & g_{233}^{10} & 0 & 0 \\
0 & 0 & g_{244}^{10} & 0 & 0
\end{bmatrix} \otimes I_2
$$

$$K^f = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_{031}^{10} k_{031} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_{233}^{10} & 0 \\ 0 & 0 & 0 & 0 & -g_{244}^{10} \end{bmatrix} \otimes I_2$$

$$F^f = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \widetilde{C}_{14} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \widetilde{C}_{14} & 0 & 0 & 0 \end{bmatrix} \otimes J$$

$$T^f = \begin{bmatrix} \frac{1}{R_0} & 0 & 0 & 0 & 0 \\ 0 & -g_{031}^{01} & 0 & 0 & 0 \\ 0 & 0 & -g_{1r2}^{01} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_3} - g_{233}^{01} & 0 \\ 0 & 0 & 0 & 0 & -g_{244}^{01} \end{bmatrix} \otimes I_2$$

$$W^f = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & \widetilde{C}_{14} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & \widetilde{C}_{14} \end{bmatrix} \otimes J.$$

The vectors S^f and P^f of (1.43)–(1.44) are omitted for simplicity. Then, (1.51) gives the fundamental tone coefficients for all nodes of the circuit.

For the harmonic tones estimation, the matrices of (1.70)–(1.75) are

$$G^h = G^f \otimes I_2$$

$$K^h = K^f \otimes I_2$$

$$F^h = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \widetilde{C}_{14} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \widetilde{C}_{14} & 0 & 0 & 0 \end{bmatrix} \otimes (L \otimes J)$$

$$T^h = T^f \otimes I_2$$

$$W^h = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & \widetilde{C}_{14} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & \widetilde{C}_{14} \end{bmatrix} \otimes (L \otimes J)$$

$$X^h = \begin{bmatrix} 0_4 & 0_4 & 0_4 & 0_4 & 0_4 \\ X^{\alpha}_{031} & X^{\gamma}_{031} & 0_4 & X^{\beta}_{031} & 0_4 \\ 0_4 & X^{\alpha}_{1r2} & X^{\gamma}_{1r2} & 0_4 & 0_4 \\ 0_4 & 0_4 & X^{\alpha}_{233} & X^{\beta}_{233} + X^{\gamma}_{233} & 0_4 \\ 0_4 & 0_4 & X^{\alpha}_{244} & 0_4 & X^{\beta}_{244} + X^{\gamma}_{244} \end{bmatrix}$$

where the following are calculated using (1.58)–(1.60), the corresponding (1.88)–(1.89) and (1.111)–(1.115)

$$\begin{aligned}
X^{\alpha}_{031} &= g^{20}_{031}\widetilde{N}_{031} + g^{30}_{031}\frac{3}{2}\widetilde{M}_{031} + g^{11}_{031}\frac{1}{2}N_1 + g^{21}_{031}Q_{031} + g^{12}_{031}\frac{1}{2}M_1 \\
X^{\beta}_{031} &= -k_{031}X^{\alpha}_{031} \\
X^{\gamma}_{031} &= g^{02}_{031}N_1 + g^{03}_{031}\frac{3}{2}M_1 + g^{11}_{031}\frac{1}{2}\widetilde{N}_{031} + g^{21}_{031}\frac{1}{2}\widetilde{M}_{031} + g^{12}_{031}Q_{031} \\
X^{\alpha}_{1r2} &= g^{20}_{1r2}\widetilde{N}_{1r2} + g^{30}_{1r2}\frac{3}{2}\widetilde{M}_{1r2} + g^{11}_{1r2}\frac{1}{2}N_2 + g^{21}_{1r2}Q_{1r2} + g^{12}_{1r2}\frac{1}{2}M_2 \\
X^{\gamma}_{1r2} &= g^{02}_{1r2}N_2 + g^{03}_{1r2}\frac{3}{2}M_2 + g^{11}_{1r2}\frac{1}{2}\widetilde{N}_{1r2} + g^{21}_{1r2}\frac{1}{2}\widetilde{M}_{1r2} + g^{12}_{1r2}Q_{1r2} \\
X^{\alpha}_{233} &= g^{20}_{233}\widetilde{N}_{233} + g^{30}_{233}\frac{3}{2}\widetilde{M}_{233} + g^{11}_{233}\frac{1}{2}N_3 + g^{21}_{233}Q_{233} + g^{12}_{233}\frac{1}{2}M_3 \\
X^{\beta}_{233} &= -X^{\alpha}_{233} \\
X^{\gamma}_{233} &= g^{02}_{233}N_3 + g^{03}_{233}\frac{3}{2}M_3 + g^{11}_{233}\frac{1}{2}\widetilde{N}_{233} + g^{21}_{233}\frac{1}{2}\widetilde{M}_{233} + g^{12}_{233}Q_{233} \\
X^{\alpha}_{244} &= g^{20}_{244}\widetilde{N}_{244} + g^{30}_{244}\frac{3}{2}\widetilde{M}_{244} + g^{11}_{244}\frac{1}{2}N_4 + g^{21}_{244}Q_{244} + g^{12}_{244}\frac{1}{2}M_4 \\
X^{\beta}_{244} &= -X^{\alpha}_{244} \\
X^{\gamma}_{244} &= g^{02}_{244}N_4 + g^{03}_{244}\frac{3}{2}M_4 + g^{11}_{244}\frac{1}{2}\widetilde{N}_{244} + g^{21}_{244}\frac{1}{2}\widetilde{M}_{244} + g^{12}_{244}Q_{244}.
\end{aligned}$$

The vectors S^h and B^h of (1.65), (1.67) (omitted for simplicity) are formed according to the definitions of (1.54)–(1.57), (1.66), (1.68), the corresponding (1.88)–(1.89) and (1.97)–(1.110). The harmonic tones coefficients are finally computed by (1.76), and thus HD_2 and HD_3.

1.4.6 Additional Remarks

To conclude the proposed method's core section, some remarks regarding less typical circuit cases are in order.

Series Resistor

In a case where a resistor is in series with a capacitor (like in a Miller compensation scheme where a series resistor is included for the elimination of a possible right half–

plane zero), the method's form does not feature an explicit way to account for it. However, the resistor can be replaced by the equivalent block of Figure 1.20, as a G_m–stage model. If the resistor, R, placed between nodes a and b, is linear, the only non–zero coefficients of the two stages modeled by (1.8) are $g^{10}_{baa} = g^{10}_{abb} = 1/R$. Weak nonlinear behavior of a resistor can also be captured by including more terms of (1.8).

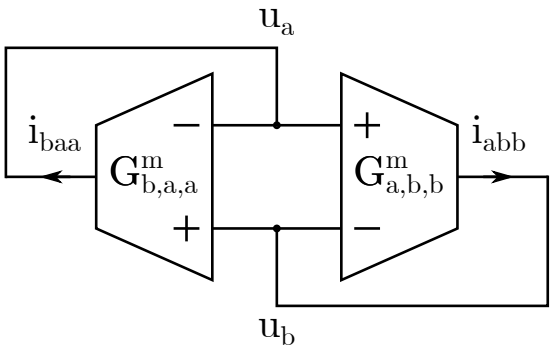

Figure 1.20: Resistor as two antiparallel G_m–stages.

Another possible use of such a resistor formulation is to model a capacitance, C_t, at the negative input of the stage $G^m_{i,t,j}$, in the case where $k_{itj} \neq 1$. For example, if a capacitor is added at the gate of M_2 in Figure 1.11, R_{L_1} can be replaced by the equivalent block of Figure 1.20; then, the voltage at the gate of M_2 becomes a new variable, u_5, and stage $G^m_{0,3,1}$ changes to $G^m_{0,5,1}$, with $k_{051} = 1$.

Parasitic Capacitors

Parasitic capacitors can be added at any node of the G_m–stage circuit representation. Their inclusion benefits nodes where no other capacitance is present, or nodes with a very small capacitance value.

Process, Supply Voltage and Temperature Variations

The method can be performed for process, supply voltage and temperature variations (PVT), by simply repeating the derivation of the $g^{k\ell}_{itj}$–coefficients of all G_m–stages and then solving (1.51) and (1.76). The variations will have an impact on the resulting output currents of the stages, that will be captured by the newly derived $g^{k\ell}_{itj}$–coefficients. The repetition of the method is much faster than the required repetition of simulation, boosting even further the speed–up gain of the distortion estimation.

1.5 Simulation Results

The proposed harmonic distortion estimation method is verified by Cadence Spectre simulation in TSMC 0.18 μm technology. Supply rails are set to ±2.5 V for all cases presented, while distortion results are obtained from parametric PSS–analysis. Each amplifier load has a reference voltage equal to the DC–operating point of its output node.

The method is implemented in MATLAB, and no parasitic capacitors are taken into account; their inclusion would result in better accuracy at high frequencies. As a rough estimate, the time of distortion estimation drops from minutes (parametric PSS–analysis) to seconds (proposed method).

1.5.1 One–Stage Cascode Amplifier

The first simulation case is that of the one–stage cascode amplifier of Figure 1.18. The implemented stage has 21.56 dB DC–gain and a unity–gain frequency of 17.86 MHz, while driving a load of 10 kΩ ‖ 10 pF. Under an input signal of 12.5 mV peak, the method's resulting HD_2 and HD_3 factors are presented in Figures 1.21 and 1.22, respectively, against the results obtained by Cadence Spectre.

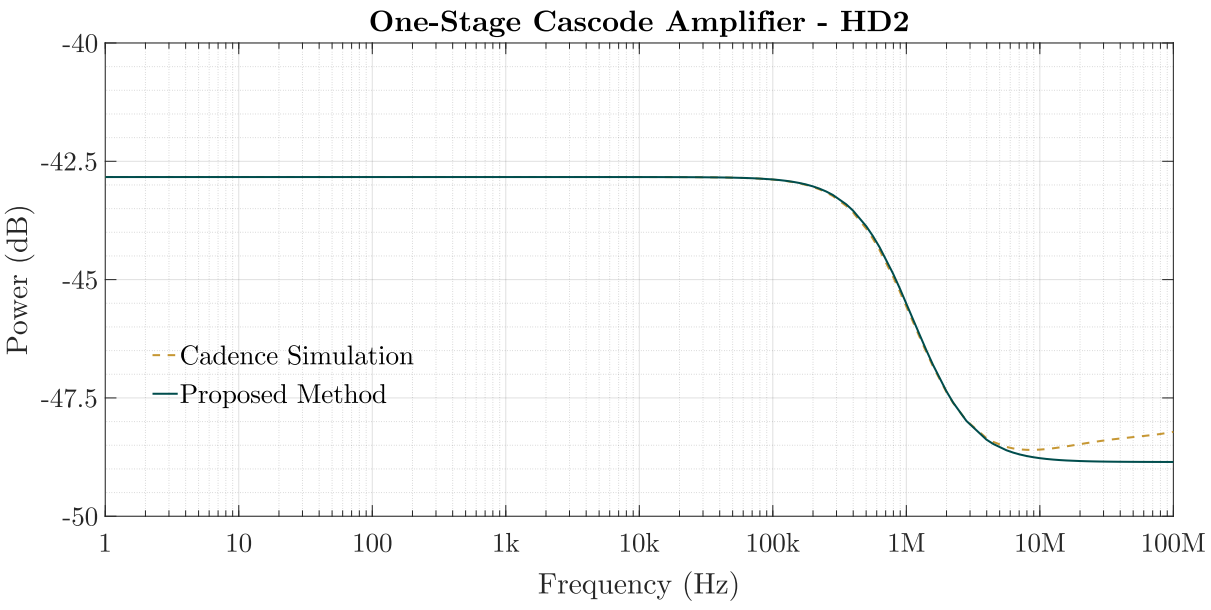

Figure 1.21: HD_2 of the one–stage cascode amplifier.

The results of the proposed method are in fine agreement with the simulation ones; the error between the simulation and the method is less than 0.64 dB for HD_2, and 1.75 dB for HD_3, for up to 100 MHz. For frequencies up to the unity–gain frequency of the amplifier, the HD_2 error is found to be less than 0.33 dB. Figure

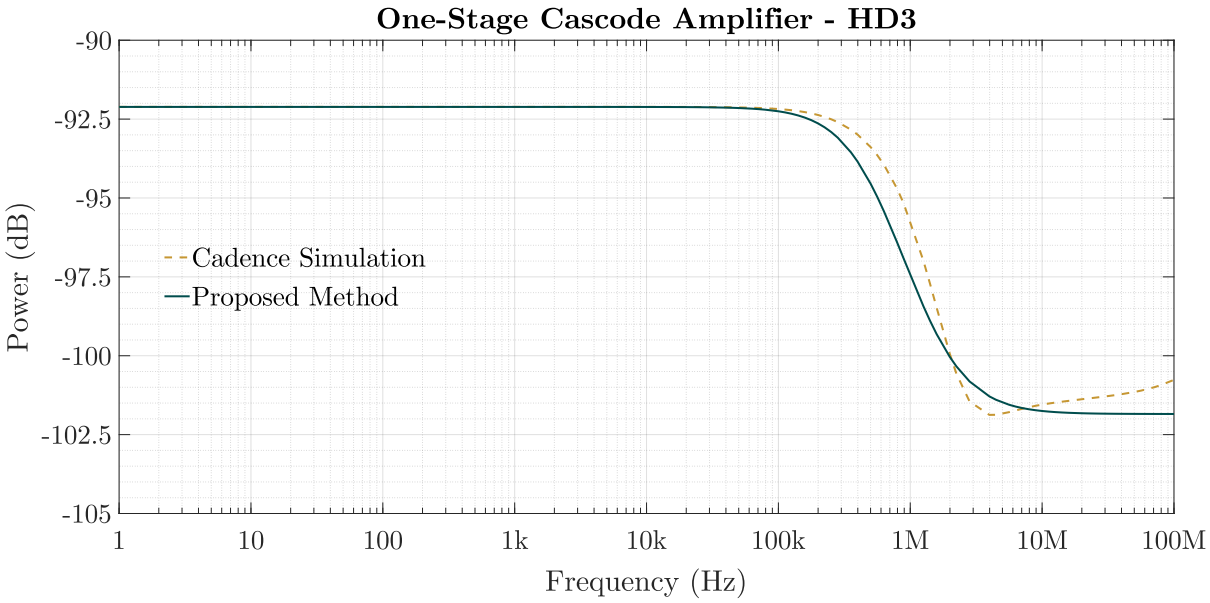

Figure 1.22: HD_3 of the one–stage cascode amplifier.

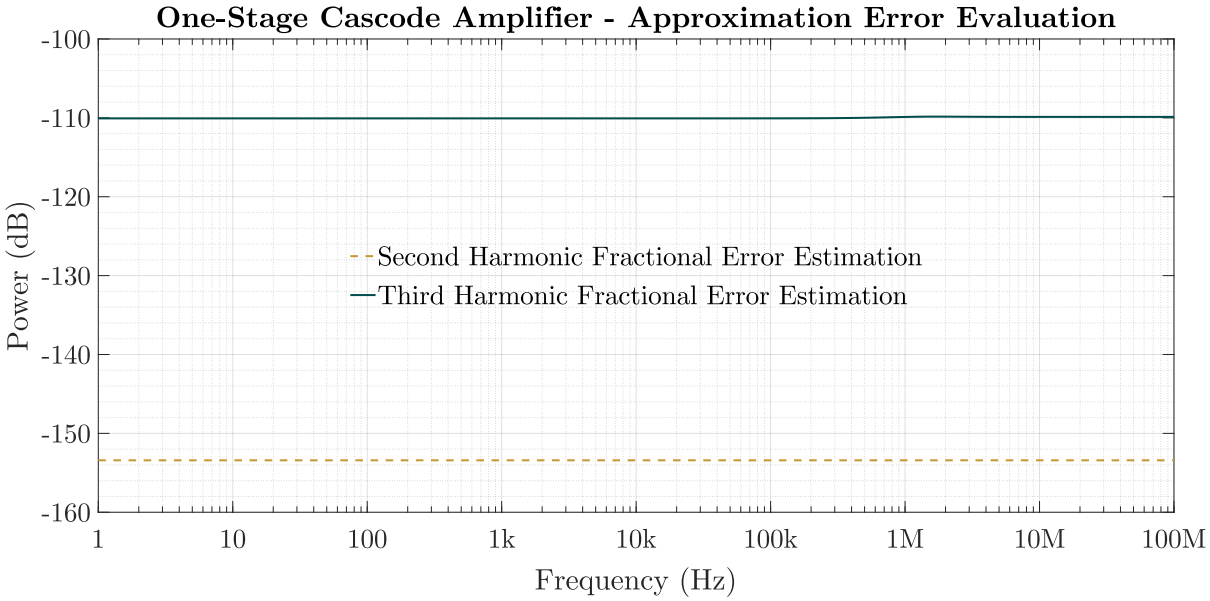

Figure 1.23: Approximation error evaluation in the second and the third harmonic for the one–stage cascode amplifier.

1.23 shows the approximation error in the second and the third harmonic, that is seen to be practically non-existed.

1.5.2 Three–Stage Feedback Amplifier

Next, the method is applied to the three–stage feedback amplifier of Figure 1.11, that has a feedback factor of $\beta = 0.05$. The amplifier drives a load of $10\,\text{k}\Omega \parallel 10\,\text{pF}$, has a DC–gain of 26.01 dB and a unity–gain frequency of 16.80 MHz. Figure 1.24 shows HD_2, with HD_3 being depicted in Figure 1.25, for an input signal of 25 mV peak.

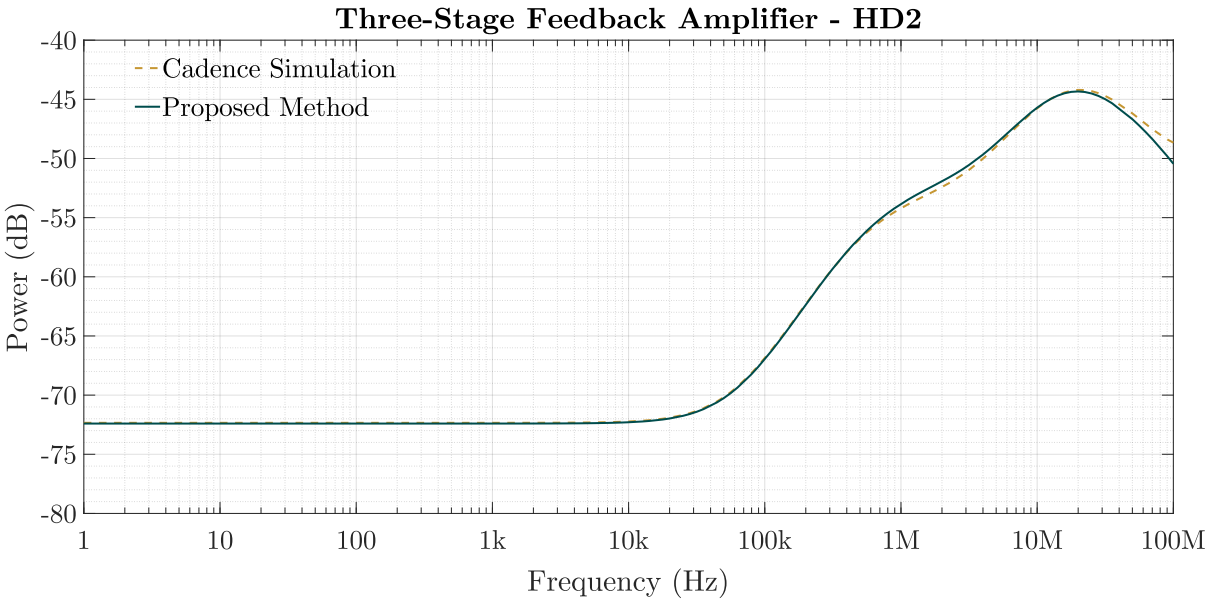

Figure 1.24: HD_2 of the three–stage feedback amplifier.

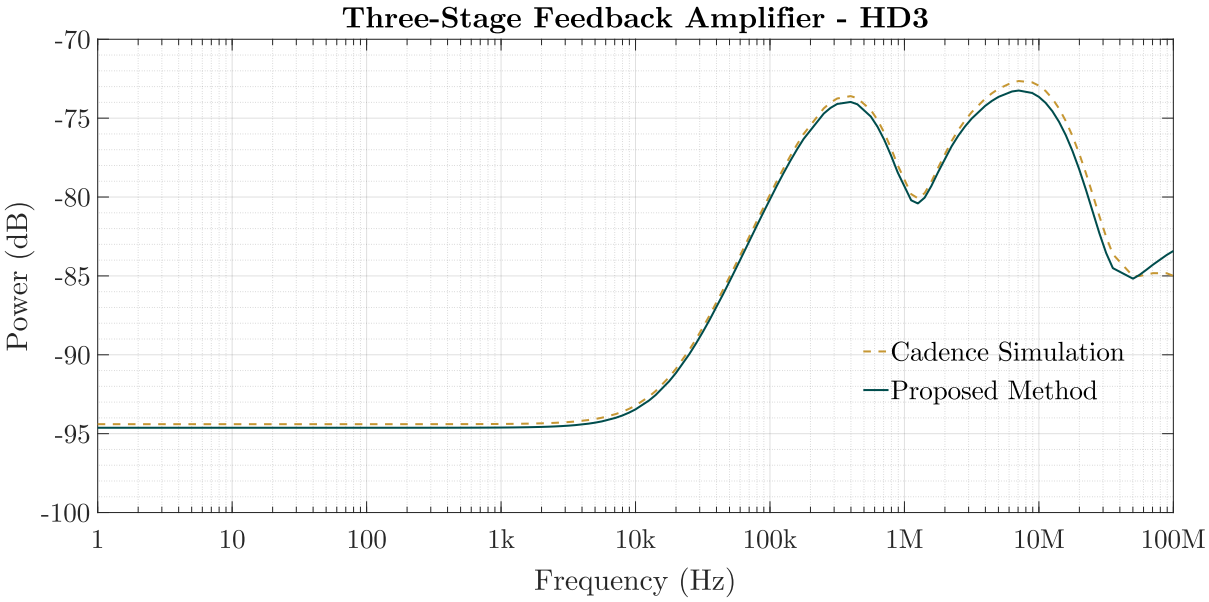

Figure 1.25: HD_3 of the three–stage feedback amplifier.

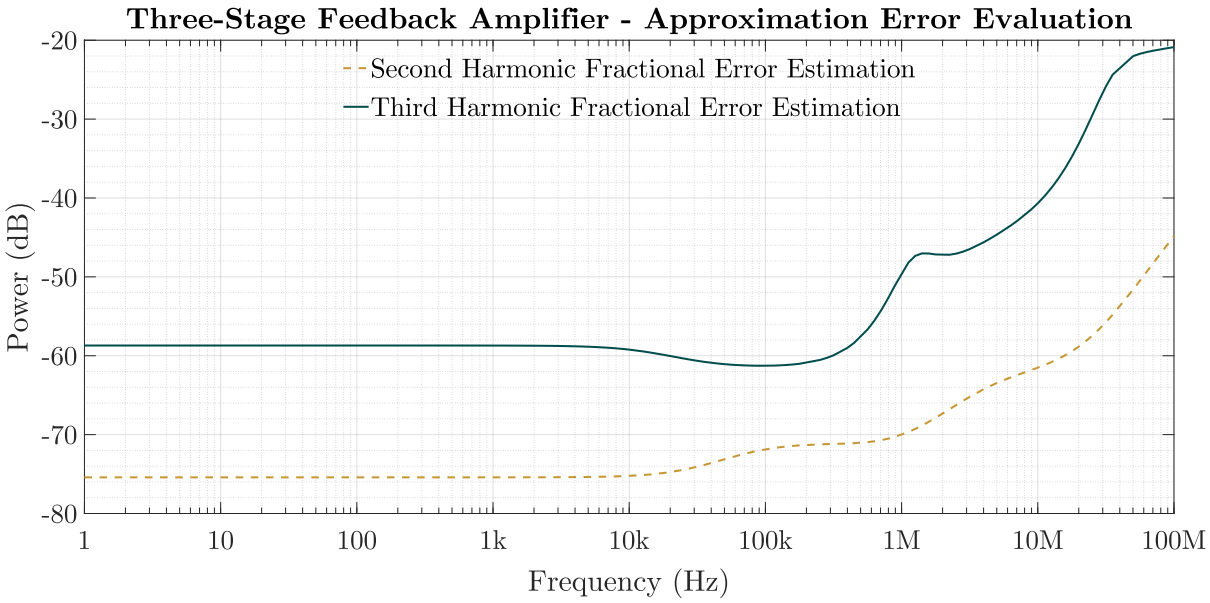

Figure 1.26: Approximation error evaluation in the second and the third harmonic for the three–stage feedback amplifier.

Both distortion factors predicted by the method are in excellent agreement with the ones from the simulation. Up to 100 MHz, the error is less than 1.79 dB for HD_2, and less than 1.58 dB for HD_3. Within the amplifier's unity–gain bandwidth, the maximum errors fall to 0.49 dB and 0.93 dB, respectively. The approximation error in the harmonic tones is illustrated in Figure 1.26, proving the validity of the method's estimation results.

1.5.3 One–Stage Fully–Differential Amplifier

Finally, the one–stage fully–differential amplifier of Figure 1.30 is simulated. The structure has 25.52 dB DC–gain and 23.79 MHz unity–gain frequency, under a load of 25 kΩ || 5 pF per output. With a 25 mV peak input signal, Figures 1.27 and 1.28 present HD_2 and HD_3, respectively.

The HD_3 factor is again in fine agreement with the corresponding simulation result; the error is found to be less than 2.36 dB for the bandwidth of 100 MHz, while within the amplifier's unity–gain frequency is less than 0.41 dB. Both HD_2 estimation results indicate practically a negligible second harmonic, as is expected by the fully–differential nature of the structure. The approximation error in the harmonics is depicted in Figure 1.29, being essentially zero.

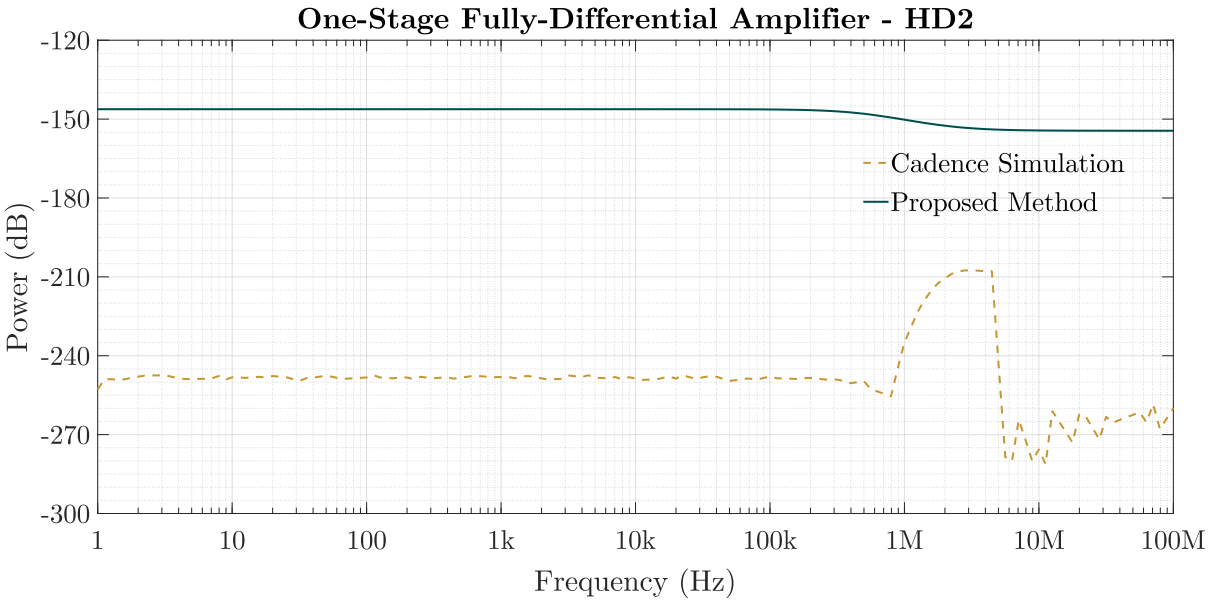

Figure 1.27: HD_2 of the one–stage fully–differential amplifier.

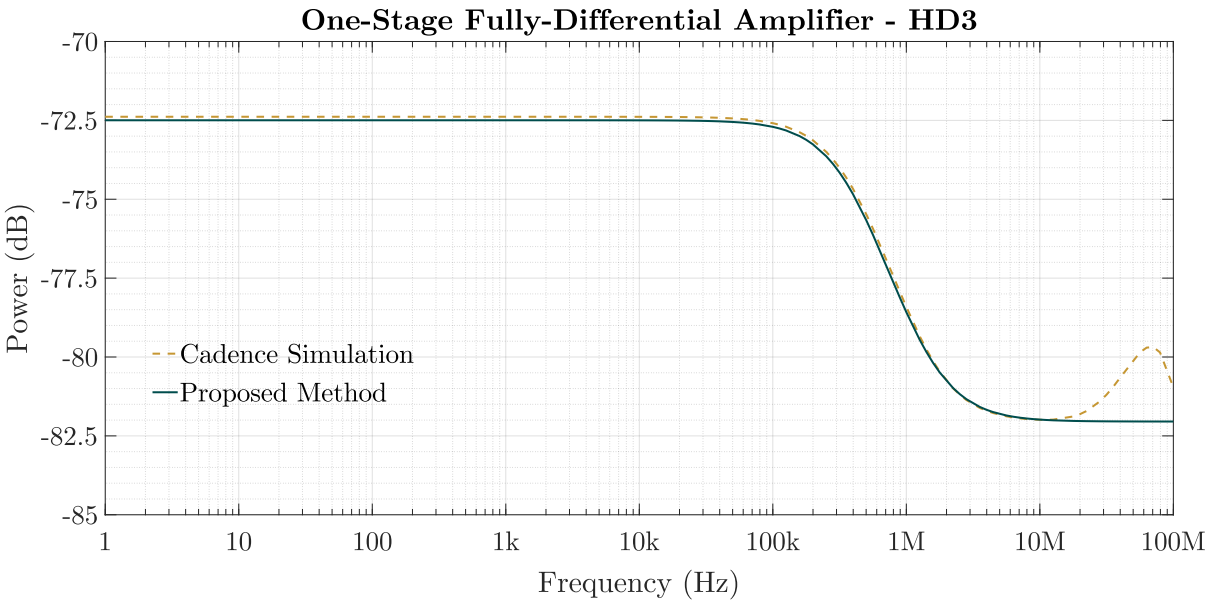

Figure 1.28: HD_3 of the one–stage fully–differential amplifier.

1.6 Summary

In this chapter, a time–domain harmonic distortion estimation method is presented, that can be applied systematically to CMOS circuits with any number of stages. It can be implemented in MATLAB and yields accurate distortion estimation results, verified by comparison with Cadence Spectre simulation. The method holds a fast computational profile that intends to be exploited by integration in EDA suites.

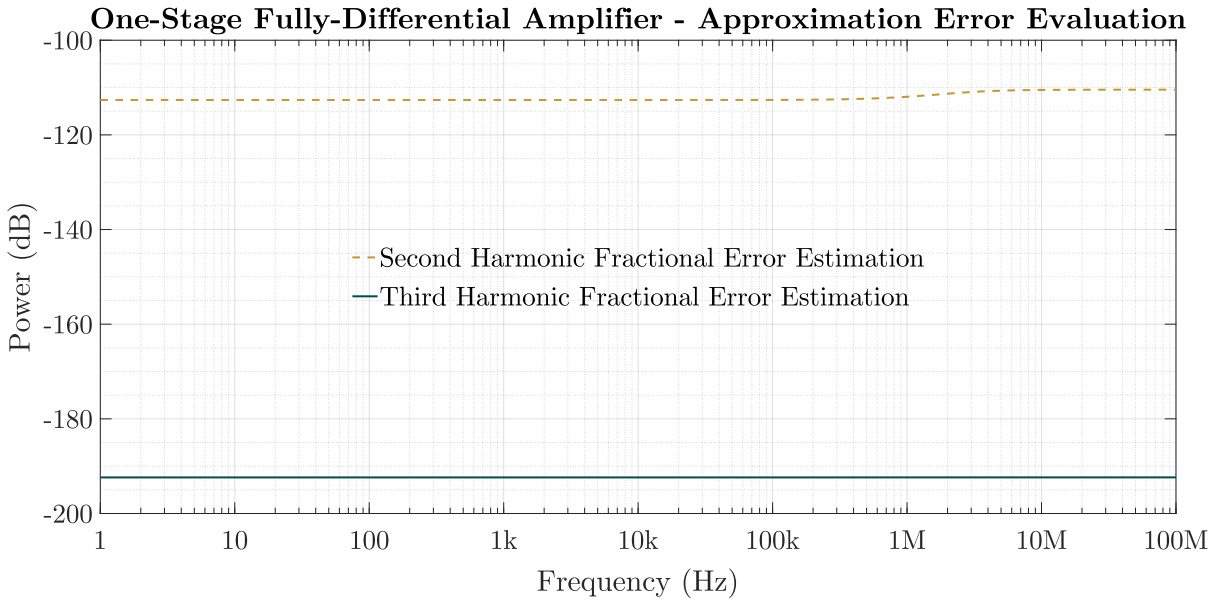

Figure 1.29: Approximation error evaluation in the second and the third harmonic for the one–stage fully–differential amplifier.

Appendix: Quantities Forming (1.54)–(1.60)

With coefficients $\widetilde{a}_{itj,1}$, $\widetilde{b}_{itj,1}$, $a_{j,1}$ and $b_{j,1}$ known from the solution of S^f by (1.51), the coefficients of (1.54)–(1.57) and the matrices (1.111)–(1.115) of (1.58)–(1.60) are given by

$$\widetilde{f}^{s2}_{itj} = \widetilde{a}_{itj,1}\widetilde{b}_{itj,1} \tag{1.97}$$

$$\widetilde{f}^{x2}_{itj} = \frac{-\widetilde{a}^2_{itj,1} + \widetilde{b}^2_{itj,1}}{2} \tag{1.98}$$

$$\widetilde{f}^{s3}_{itj} = \frac{\widetilde{a}_{itj,1}}{4}\left(-\widetilde{a}^2_{itj,1} + 3\widetilde{b}^2_{itj,1}\right) \tag{1.99}$$

$$\widetilde{f}^{x3}_{itj} = \frac{\widetilde{b}_{itj,1}}{4}\left(-3\widetilde{a}^2_{itj,1} + \widetilde{b}^2_{itj,1}\right) \tag{1.100}$$

$$f^{s2}_{j} = a_{j,1}b_{j,1} \tag{1.101}$$

$$f^{x2}_{j} = \frac{-a^2_{j,1} + b^2_{j,1}}{2} \tag{1.102}$$

$$f^{s3}_{j} = \frac{a_{j,1}}{4}\left(-a^2_{j,1} + 3b^2_{j,1}\right) \tag{1.103}$$

$$f^{x3}_{j} = \frac{b_{j,1}}{4}\left(-3a^2_{j,1} + b^2_{j,1}\right) \tag{1.104}$$

$$h^{s2}_{itj} = \frac{\widetilde{a}_{itj,1}b_{j,1} + \widetilde{b}_{itj,1}a_{j,1}}{2} \tag{1.105}$$

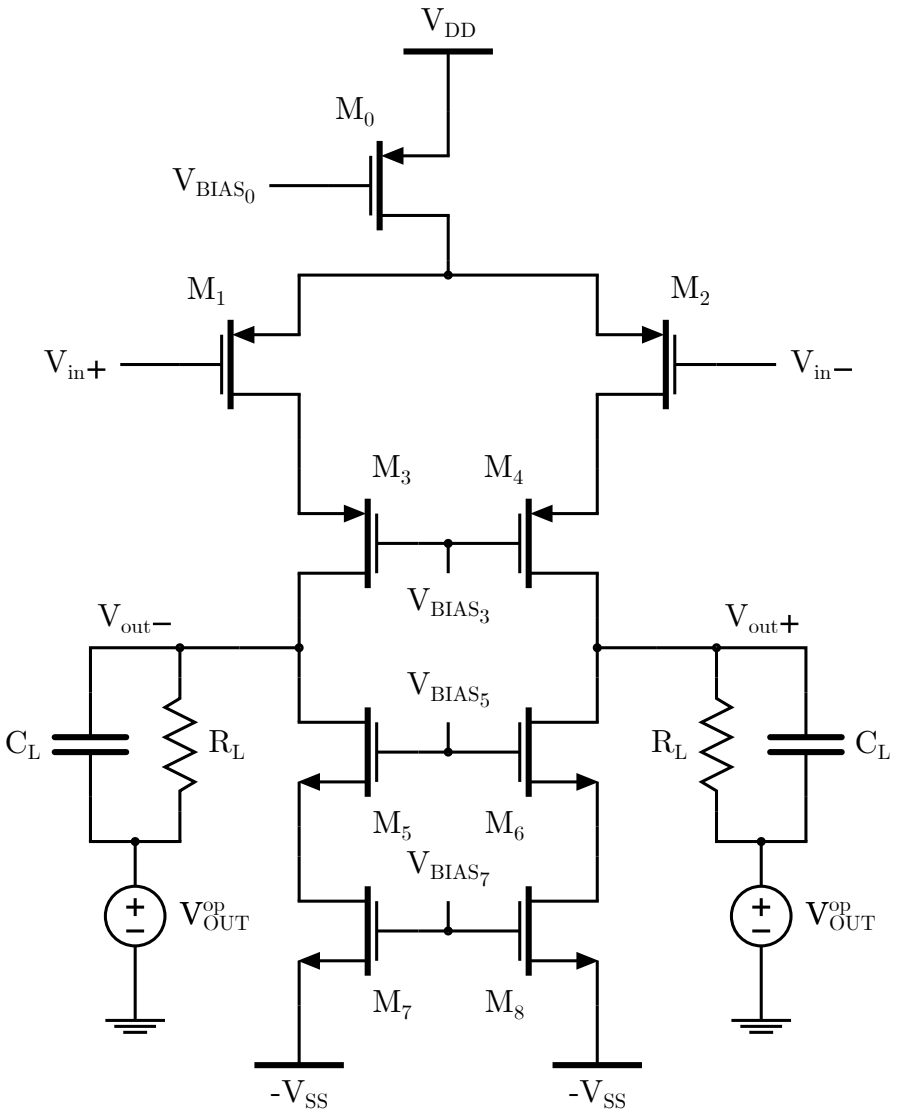

Figure 1.30: One–stage fully–differential amplifier.

$$h^{c2}_{itj} = \frac{-\widetilde{a}_{itj,1}a_{j,1} + \widetilde{b}_{itj,1}b_{j,1}}{2} \tag{1.106}$$

$$r^{s3}_{itj} = \left(-\widetilde{a}^2_{itj,1} + \widetilde{b}^2_{itj,1}\right)\frac{a_{j,1}}{4} + \left(\widetilde{a}_{itj,1}\widetilde{b}_{itj,1}\right)\frac{b_{j,1}}{2} \tag{1.107}$$

$$r^{c3}_{itj} = \left(-\widetilde{a}^2_{itj,1} + \widetilde{b}^2_{ijt,1}\right)\frac{b_{j,1}}{4} - \left(\widetilde{a}_{itj,1}\widetilde{b}_{itj,1}\right)\frac{a_{j,1}}{2} \tag{1.108}$$

$$o^{s3}_{itj} = \left(-a^2_{j,1} + b^2_{j,1}\right)\frac{\widetilde{a}_{itj,1}}{4} + \left(a_{j,1}b_{j,1}\right)\frac{\widetilde{b}_{itj,1}}{2} \tag{1.109}$$

$$o^{c3}_{itj} = \left(-a^2_{j,1} + b^2_{j,1}\right)\frac{\widetilde{b}_{itj,1}}{4} - \left(a_{j,1}b_{j,1}\right)\frac{\widetilde{a}_{itj,1}}{2} \tag{1.110}$$

$$\widetilde{N}_{itj} = \begin{bmatrix} 0 & 0 & \widetilde{b}_{itj,1} & -\widetilde{a}_{itj,1} \\ 0 & 0 & \widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} \\ \widetilde{b}_{itj,1} & \widetilde{a}_{itj,1} & 0 & 0 \\ -\widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{4\times 4} \tag{1.111}$$

$$N_j = \begin{bmatrix} 0 & 0 & b_{j,1} & -a_{j,1} \\ 0 & 0 & a_{j,1} & b_{j,1} \\ b_{j,1} & a_{j,1} & 0 & 0 \\ -a_{j,1} & b_{j,1} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{4\times 4} \tag{1.112}$$

$$\widetilde{M}_{itj} = \left(\widetilde{a}^2_{itj,1} + \widetilde{b}^2_{itj,1}\right) I_4 \in \mathbb{R}^{4\times 4} \tag{1.113}$$

$$M_j = \left(a^2_{j,1} + b^2_{j,1}\right) I_4 \in \mathbb{R}^{4\times 4} \tag{1.114}$$

$$Q_{itj} = \left(\widetilde{a}_{itj,1} a_{j,1} + \widetilde{b}_{itj,1} b_{j,1}\right) I_4 \in \mathbb{R}^{4\times 4}. \tag{1.115}$$

References

[1] Tony Chan Carusone, David Johns, and Kenneth Martin. *Analog Integrated Circuit Design*. 2nd ed. John Wiley & Sons, Inc., 2011.

[2] Douglas Self. *Audio Power Amplifier Design*. 6th ed. Focal Press, 2013.

[3] P. Dobrovolny et al. "Analysis and compact behavioral modeling of nonlinear distortion in analog communication circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 22.9 (Sept. 2003), pp. 1215–1227.

[4] Rowan J. Gilmore and Michael B. Steer. "Nonlinear circuit analysis using the method of harmonic balance—A review of the art. Part I. Introductory concepts". In: *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering* 1.1 (1991), pp. 22–37.

[5] Stephen A. Maas. *Nonlinear Microwave and RF Circuits*. 2nd ed. Artech House, 2003.

[6] D. Tannir and R. Khazaka. "Adjoint Sensitivity Analysis of Nonlinear Distortion in Radio Frequency Circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 30.6 (June 2011), pp. 934–939.

[7] D. Tannir. "Direct Sensitivity Analysis of Nonlinear Distortion in RF Circuits Using Multidimensional Moments". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 34.3 (Mar. 2015), pp. 321–331.

[8] Piet Wambacq and Willy Sansen. *Distortion Analysis of Analog Integrated Circuits*. 1st ed. Vol. 451. The Springer International Series in Engineering and Computer Science. Springer US, 1998.

[9] Peng Li and L. T. Pileggi. "Efficient per-nonlinearity distortion analysis for analog and RF circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 22.10 (Oct. 2003), pp. 1297–1309.

[10] Z. Zhang, A. Celik, and P. Sotiriadis. "A fast state-space algorithm to estimate harmonic distortion in fully differential weakly nonlinear G_m-C filters". In: *2006 IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2006, 4 pp.–2956. DOI: 10.1109/ISCAS.2006.1693244.

[11] Zhaonian Zhang, A. Celik, and P. P. Sotiriadis. "State-space harmonic distortion modeling in weakly nonlinear, fully balanced G_m-C filters-a modular approach resulting in closed-form solutions". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 53.1 (Jan. 2006), pp. 48–59. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.854296.

[12] P. P. Sotiriadis et al. "Fast State-Space Harmonic-Distortion Estimation in Weakly Nonlinear G_m-C Filters". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 54.1 (Jan. 2007), pp. 218–228. ISSN: 1549-8328. DOI: 10.1109/TCSI.2006.887458.

[13] A. Cooman et al. "Distortion Contribution Analysis With the Best Linear Approximation". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.12 (Dec. 2018), pp. 4133–4146. ISSN: 1549-8328. DOI: 10.1109/TCSI.2018.2834139.

[14] Y. Miao and Y. Zhang. "Distortion Modeling of Feedback Two-Stage Amplifier Compensated With Miller Capacitor and Nulling Resistor". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 59.1 (Jan. 2012), pp. 93–105.

[15] G. Shi. "Symbolic Distortion Analysis of Multistage Amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.1 (Jan. 2019), pp. 369–382.

[16] G. Palumbo and S. Pennisi. "Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain". In: *ICECS 2001. 8th IEEE International Conference on Electronics, Circuits and Systems (Cat. No.01EX483)*. Vol. 1. Sept. 2001, 209–212 vol.1. DOI: 10.1109/ICECS.2001.957717.

[17] G. Giustolisi, G. Palumbo, and S. Pennisi. "Harmonic distortion in single-stage amplifiers". In: *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*. Vol. 2. May 2002, pp. II–II. DOI: 10.1109/ISCAS.2002.1010916.

[18] G. Palumbo and S. Pennisi. "High-frequency harmonic distortion in feedback amplifiers: analysis and applications". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 50.3 (Mar. 2003), pp. 328–340. ISSN: 1057-7122. DOI: 10.1109/TCSI.2003.808835.

[19] G. Palumbo and S. Pennisi. "Harmonic distortion in three-stage nested-Miller-compensated amplifiers". In: *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*. Vol. 1. May 2004, pp. I–485. DOI: 10.1109/ISCAS.2004.1328237.

[20] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Accurate estimation of high-frequency harmonic distortion in two-stage Miller OTAs". In: *IEE Proceedings - Circuits, Devices and Systems* 152.5 (Oct. 2005), pp. 417–424. ISSN: 1350-2409. DOI: 10.1049/ip-cds:20045057.

[21] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Distortion analysis of three-stage amplifiers with reversed nested-Miller compensation". In: *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.* Vol. 3. Sept. 2005, III/93–III/96 vol. 3. DOI: 10.1109/ECCTD.2005.1523068.

[22] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "New analytical approach to evaluate harmonic distortion in nonlinear feedback amplifiers". In: *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.* Vol. 3. Sept. 2005, III/97–III100 vol. 3. DOI: 10.1109/ECCTD.2005.1523069.

[23] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Distortion analysis of Miller-compensated three-stage amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 53.5 (May 2006), pp. 961–976. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.862287.

[24] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "An approach to model high-frequency distortion in negative-feedback amplifiers". In: *International Journal of Circuit Theory and Applications* 36.1 (2008), pp. 3–18.

[25] A. Borys. "On analysis of harmonic distortion in op amps based circuits via Volterra series". In: *2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems*. June 2016, pp. 330–335. DOI: 10.1109/MIXDES.2016.7529758.

[26] Dimitrios Baxevanakis and Paul P. Sotiriadis. "Accurate Harmonic Distortion Estimation in CMOS Circuits using a Cross-Product Gm-Stage Modeling". In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, Oct. 2020. DOI: 10.1109/iscas45731.2020.9181113.

[27] Sanghoon Kang, Byounggi Choi, and Bumman Kim. "Linearity analysis of CMOS for RF application". In: *IEEE Transactions on Microwave Theory and Techniques* 51.3 (Mar. 2003), pp. 972–977. ISSN: 0018-9480. DOI: 10.1109/TMTT.2003.808709.

[28] B. Toole, C. Plett, and M. Cloutier. "RF circuit implications of moderate inversion enhanced linear region in MOSFETs". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 51.2 (Feb. 2004), pp. 319–328. ISSN: 1549-8328. DOI: 10.1109/TCSI.2003.822400.

[29] B. Hernes and W. Sansen. "Distortion in single-, two- and three-stage amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.5 (May 2005), pp. 846–856. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.846214.

[30] S. C. Blaakmeer et al. "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling". In: *IEEE Journal of Solid-State Circuits* 43.6 (June 2008), pp. 1341–1350. ISSN: 0018-9200. DOI: 10.1109/JSSC.2008.922736.

[31] P. S. Crovetti. "Finite Common-Mode Rejection in Fully Differential Nonlinear Circuits". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 58.8 (Aug. 2011), pp. 507–511.

[32] P. S. Crovetti and F. Fiori. "Finite common-mode rejection in fully differential operational amplifiers". In: *Electronics Letters* 42.11 (May 2006), pp. 615–617.

[33] F. Fiori and P. S. Crovetti. "Nonlinear effects of radio-frequency interference in operational amplifiers". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 49.3 (Mar. 2002), pp. 367–372.

[34] B. Perez-Verdu et al. "Nonlinear time-domain macromodeling of OTA circuits". In: *IEEE International Symposium on Circuits and Systems* 1989 (May 1989), 1441–1444 vol.2.

[35] N. Scheinberg and A. Pinkhasov. "A computer simulation model for simulating distortion in FET resistors". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 19.9 (Sept. 2000), pp. 981–989.

[36] Harold Wayne Sorenson. *Parameter Estimation: Principles and Problems*. Vol. 9. Control and Systems Theory. M. Dekker, 1980.

[37] Peter Lancaster and Miron Tismenetsky. *The Theory of Matrices with Applications*. 2nd ed. Computer Science and Scientific Computing. Academic Press, 1985.

[38] Roger A. Horn and Charles R. Johnson. *Matrix Analysis*. 2nd ed. Cambridge University Press, 2013.

2 Intermodulation Distortion Estimation in CMOS Circuits

This chapter presents a general, time–domain method for intermodulation distortion estimation offering a fast, systematic and compact formulation. It can be applied to any linear CMOS circuit architecture, with any number of stages, ranging from amplifiers and transconductors to filters, that are characterized by weakly nonlinear behavior. Each CMOS stage of the circuit is modeled as a G_m–stage with an output current expressed as a more involved function of its input and output voltages, taking into account both powers and cross–product terms necessary to accurately capture the nonlinear behavior. The proposed method is easily implemented in numerical computing environments like MATLAB or Python, and results in a very fast distortion estimation. A number of example topologies simulated in Cadence Spectre illustrate the application of the method and demonstrate its accuracy.

2.1 Introduction

Intermodulation distortion is a quantity of major significance in circuit design; intermodulation and harmonic distortion characterize the linearity of a circuit, and thus their behavior is considered crucial in the performance of power amplifiers, radio–frequency amplifiers [1], low–noise amplifiers, filters, and more.

The most popular test to measure intermodulation distortion is the two–tone test [2, 3], where two sinusoidal signals at frequencies ω_1 and ω_2 drive the circuit under consideration. The result is the generation of intermodulation products at frequencies

$\pm m\omega_1 \pm n\omega_2$, where $m, n = 1, 2, 3, \ldots$; the sum $m+n$ is the order of the corresponding intermodulation product.

Of particular interest is the behavior of the third–order intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, since these frequencies are very close to the original input signals, should $\omega_1 = \omega - \delta_\omega$ and $\omega_2 = \omega + \delta_\omega$, with $\delta_\omega \ll \omega$. As a consequence, the third–order intermodulation distortion IM_3, defined as the ratio of the power of the aforementioned third–order intermodulation products to the power of the input signals, is one of the most common intermodulation distortion metrics, and the estimation subject of this work.

Usually, the estimation of intermodulation distortion is performed by simulation methods like harmonic balance or shooting [4, 5]. However, these methods can be time–consuming and computationally expensive [6, 7], which has favored the development of dedicated methods for distortion estimation. The use of the Volterra series [2, 8, 9] remains a popular approach, yielding very accurate distortion results. Its drawback is that the mathematical expressions of the involved operators become very complicated as the number of circuit elements rises, making their manipulation practically unmanageable.

Other existing methods include the use of linear–centric circuit models to account for individual distortion contributions [10]; the method is based on the Volterra analysis framework and gives very accurate results. However, it requires a steady–state analysis to be initially performed. For weakly nonlinear fully–differential G_m–C filters of any order, a systematic state–space approach has been proposed [11]; the approach results in a fast distortion estimation, but it is developed for this particular circuit family. A distortion contribution analysis by means of the best linear approximation has been recently proposed [12]; it distinguishes itself from classic distortion methods by adopting a noise–like analysis, being able to handle complex excitation signals and strong nonlinearities. Its trade-off is an increased simulation time. Various harmonic distortion estimation methods that rely on algebraic manipulation of simplified amplifier models [13, 14, 15, 16, 17, 18, 19, 20, 21] offer circuit intuition and could be modified to account for intermodulation distortion, but they are usually tailored for specific amplifier topologies, requiring extensive algebraic manipulation in order to be used for more general cases.

This chapter uses the same principles as the work on harmonic distortion estimation [22] and presents its standalone counterpart for the more complex problem of estimating the intermodulation distortion in CMOS circuits that exhibit weakly nonlinear behavior. The proposed method offers a compact and systematic way applicable to general circuit structures with any number of stages, ranging from simple transconductor stages to filters and cascaded amplifiers. The estimation of IM_3 is characterized by a high level of accuracy and is performed on a G_m–stage equivalent model of the circuit under consideration. Each G_m–stage captures its correspond-

ing stage's current–characteristic accurately by employing a more involved current model, and curve–fitting. All the necessary mathematical expressions are provided to the potential reader, enabling the immediate application of the proposed method. The method is easily implemented in numerical computing environments like MATLAB or Python, and gives a very fast distortion estimation due to its formulation.

This chapter is organized as follows. Section 2.2 presents the modeling of CMOS stages and the derivation of the model coefficients, while Section 2.3 introduces the proposed method for the estimation of intermodulation distortion. Section 2.4 validates the method's accuracy by comparison with simulation, and Section 2.5 summarizes the chapter.

2.2 Modeling CMOS Stages as G_m–Stages

CMOS circuits are eventually interconnections of distinct CMOS stages. A CMOS stage that produces an output current as a response to an input voltage can be considered and modeled as a G_m–stage, like the one presented in Figure 2.1. Generally, the output

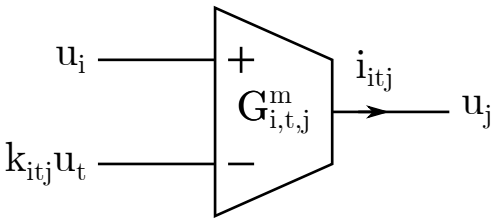

Figure 2.1: G_m–stage representation [22].

current of a CMOS stage is a nonlinear function of its input and output voltages. This nonlinear nature causes distortion generation; thus, it comprises the vital behavior to be captured by the stage's corresponding G_m–stage model.

It is reported that parasitic capacitances in MOS transistors do not substantially contribute to the generation of distortion; mainly, they reduce the magnitude of a stage's output impedance at high frequencies [23, 24]. This makes possible the formation of a G_m–stage model that is based solely on the DC–characteristics of its corresponding CMOS stage. A way of obtaining such a model is by approximating the stage's output current with a power–series expansion around its DC–operating point.

2.2.1 Proposed G_m–Stage Model

Throughout this work, $G^m_{i,t,j}$ marks the G_m–stage that has positive input, u_i, at node i; negative input, $k_{itj}u_t$, from node t, with k_{itj} a real feedback factor[1]; and produces

[1]This particular notation is adopted to capture a range of popular topologies.

output current, i_{itj}, at node j. The stage's differential input voltage is

$$\widetilde{u}_{itj} = u_i - k_{itj} u_t. \tag{2.1}$$

The *itj*–triplet[2] of notation is included in all of the characteristics of a particular G_m–stage, whereas the ac–ground is marked as r (reference potential). The tilde symbol ($\sim$) placed above a quantity is used to highlight that that specific quantity is input–related. It is also used to mark coupling capacitances, as will be stated later.

Most G_m–stage models express the stage's output current as a power–series of its input and output voltages, where input– and output–related terms are independent of one another [14, 15, 17, 18, 20]. The absence of cross–terms between the two voltages can however lead to significant deviations and errors [25, 22, 26].

An accurate model must include cross–products of the input and output voltages of the stage. This has been done at transistor–level [23, 24, 27, 28, 1], where the MOS device acting as amplifier is supposed to admit a two– or three–dimensional Taylor series expansion, and the coefficients of the approximation are calculated by means of the partial derivatives of the transistor's current relationship.

In this work, it is assumed that each G_m–stage's operation is characterized by weakly nonlinear behavior, and that its output current is considered to have a time–domain [29, 30, 31, 32, 11] power–series expression[3] of [26, 22]

$$i_{itj} = \sum_{\substack{k,\ell \geq 0 \\ k+\ell \geq 1}} g_{itj}^{k\ell} \widetilde{u}_{itj}^{k} u_j^{\ell}. \tag{2.2}$$

In order to combine good accuracy with reasonable complexity it is set $k+\ell = 1, 2, 3$, and (2.2) becomes

$$i_{itj} = g_{itj}^{10}\widetilde{u}_{itj} + g_{itj}^{20}\widetilde{u}_{itj}^2 + g_{itj}^{30}\widetilde{u}_{itj}^3 + g_{itj}^{01}u_j + g_{itj}^{02}u_j^2 + g_{itj}^{03}u_j^3 + g_{itj}^{11}\widetilde{u}_{itj}u_j + g_{itj}^{21}\widetilde{u}_{itj}^2 u_j + g_{itj}^{12}\widetilde{u}_{itj}u_j^2. \tag{2.3}$$

The $g_{itj}^{k\ell}$–coefficients of (2.3) characterize each G_m–stage.

2.2.2 G_m–Stage Equivalent Circuit Representation

An equivalent G_m–stage representation of a circuit can be constructed by identifying the CMOS stages that the circuit is comprised of, and their interconnections. Standard CMOS stages include the differential pair, the common–source, common–gate, and source–follower stages; stages that result from combinations of them, such as a cascode stage, can either be represented by the individual G_m–stages of their basic blocks, or even be treated as a single, individual stage. Fully–differential structures

[2] Commas between i, t, and j are omitted in coefficients, voltages and currents for simplicity.
[3] The $k\ell$–superscript in $g_{itj}^{k\ell}$–coefficients indicates the corresponding power of $\widetilde{u}_{itj}^{k}$ and u_j^{ℓ}.

can be easily modeled by single–ended G_m–stages. More details on the formulation of CMOS stages as G_m–stages and the construction of a circuit's G_m–stage equivalent can be found in the chapter on harmonic distortion estimation [22].

A specific procedure for identifying the CMOS stages and decomposing a circuit automatically is out of the scope of this work. A possible, semi–automatic option would require the designer to mark each distinct stage during the design process, in the same way different subcircuits are represented and connected by their higher–level symbols. Then, the process of deriving the $g_{itj}^{k\ell}$–coefficients of each stage and the mapping of the circuit's G_m–stage equivalent could be automated.

2.2.3 G_m–Stage Model Coefficients

Most of the works in the literature as well as various analyses derive the model's coefficients by a Taylor series expansion at the DC–operating point of the stage. Such an approach, however, yields accurate results only locally and for small signal amplitudes [33]. In order to capture in detail the amplitude–adjusted nonlinearities of each stage, the $g_{itj}^{k\ell}$–coefficients of (2.3) of each model are instead derived by curve–fitting, through a three–step derivation procedure[4] that involves the following.

1. AC–Analysis for Estimation of Amplitude Levels

Given the decomposition of the complete circuit into its distinct CMOS stages, an initial ac–analysis is performed in order to estimate the maximum expected signal amplitude at the input and the output of each stage, in the frequency range of interest.

2. 2D DC–Sweeps for Model Coefficients Derivation

Each stage of the circuit is set to its input and output DC–operating points, and a 2D DC–sweep of its unloaded output current is performed. The sweeping ranges for the stage's input and output voltages are the maximum input and output amplitudes derived in the ac–analysis, with r_1 and r_2 number of steps, respectively.

3. Model Coefficients Extraction via Linear Regression

The acquired data from the 2D DC–sweeps are processed in a linear regression fashion to derive each stage's $g_{itj}^{k\ell}$–coefficients. More specifically, a linear least-squares problem [34] is formed

$$I_g = UG \tag{2.4}$$

[4] A more detailed description of the proposed derivation procedure can be found in the chapter on harmonic distortion estimation [22].

where $I_g \in \mathbb{R}^{(r_1 \cdot r_2)\times 1}$ is a column matrix with the values of the stage's output current, and the matrices U and G are defined as

$$U = \left[\widetilde{u}_{itj},\ \widetilde{u}^2_{itj},\ \widetilde{u}^3_{itj},\ u_j,\ u_j^2,\ u_j^3,\ \widetilde{u}_{itj}u_j,\ \widetilde{u}^2_{itj}u_j,\ \widetilde{u}_{itj}u_j^2\right] \in \mathbb{R}^{(r_1 \cdot r_2)\times 9} \tag{2.5}$$

$$G = \left[g^{10}_{itj},\ g^{20}_{itj},\ g^{30}_{itj},\ g^{01}_{itj},\ g^{02}_{itj},\ g^{03}_{itj},\ g^{11}_{itj},\ g^{21}_{itj},\ g^{12}_{itj}\right]^{\top} \in \mathbb{R}^{9\times 1}. \tag{2.6}$$

The solution of (2.4) gives the $g^{k\ell}_{itj}$–coefficients of the corresponding stage.

2.3 Intermodulation Distortion Estimation

The proposed intermodulation estimation method can be performed in general network structures, like the one of Figure 2.2 [22]. The circuit may be comprised of G_m–stages, resistors and capacitors. Each circuit node j, $j = 0, 1, \ldots, n$, can have a resistor, R_j, and a capacitor, C_j, connected to ground, while coupling between nodes ℓ and j can be provided by capacitor $\widetilde{C}_{\ell j}$. Each node can also have an excitation signal as an independent current source, $\hat{i}_j$.

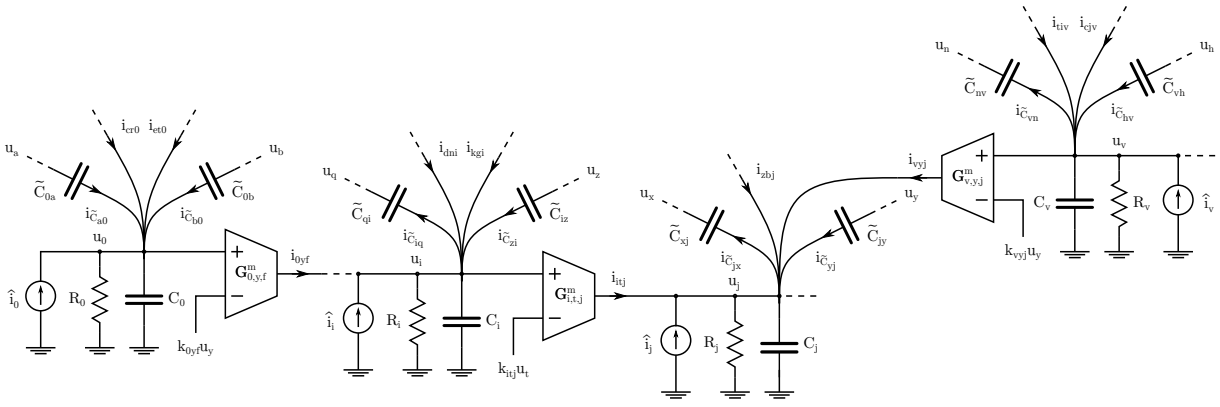

Figure 2.2: General circuit structure, composed of G_m–stages [22].

For each node j, it is

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} i_{\widetilde{C}_{\ell j}} = \frac{u_j}{R_j} + C_j \dot{u}_j \tag{2.7}$$

where current $i_{\widetilde{C}_{\ell j}}$ of coupling capacitor $\widetilde{C}_{\ell j}$ is given by

$$i_{\widetilde{C}_{\ell j}} = \widetilde{C}_{\ell j}\left(\dot{u}_\ell - \dot{u}_j\right) = -i_{\widetilde{C}_{j\ell}}. \tag{2.8}$$

Thus, (2.7) is reorganized as

$$\hat{i}_j + \sum_{i,t} i_{itj} + \sum_{\ell} \widetilde{C}_{\ell j} \dot{u}_\ell = \frac{u_j}{R_j} + \left(C_j + \sum_{\ell} \widetilde{C}_{\ell j} \right) \dot{u}_j. \tag{2.9}$$

In order to estimate the intermodulation distortion IM_3, it is assumed that the circuit operates in steady–state, and that the voltage of node j is of the form

$$u_j = u_j^f + u_j^m \tag{2.10a}$$
$$u_j^f = \theta^f S_j^f \tag{2.10b}$$
$$u_j^m = \theta^m S_j^m. \tag{2.10c}$$

That is, it is assumed that the voltage of each node j has two components. The first component, u_j^f, includes the fundamental tones at frequencies ω_1 and ω_2. The component of u_j^m represents the desired intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, and also includes the dominant harmonic and intermodulation tones that are involved with their generation; due to the nature of intermodulation distortion, including only $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ in u_j^m would result in a poor estimation of IM_3. The additional tones interact with the fundamental ones and significantly contribute to the power levels at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$.

For a combination of good accuracy and reasonable complexity, the additional terms that are taken into account are products of up to the third–order. Given the assumption of weakly nonlinear stage behavior, products of higher order than that will have much smaller power, and so, negligible contribution to the desired intermodulation products. Thus, the additional tones considered are $\omega_2 - \omega_1$, $2\omega_1$, $2\omega_2$, $2\omega_1 + \omega_2$, $2\omega_2 + \omega_1$, $3\omega_1$ and $3\omega_2$, where it is assumed that $\omega_2 > \omega_1$.

Returning to (2.10b) and (2.10c), vectors[5] θ^f and θ^m contain the sin and cos terms for the two components, while vectors S_j^f and S_j^m feature the corresponding amplitude coefficients. So, it is

$$S_j^f = \left[a_{j,1},\ b_{j,1},\ c_{j,1},\ d_{j,1} \right]^\top \in \mathbb{R}^{4\times 1} \tag{2.11}$$
$$\begin{aligned} S_j^m = \big[& \ell_j,\ m_j,\ a_{j,2},\ b_{j,2},\ c_{j,2},\ d_{j,2},\ e_j,\ f_j,\ h_j,\ r_j, \\ & p_j,\ \nu_j,\ x_j,\ y_j,\ a_{j,3},\ b_{j,3},\ c_{j,3},\ d_{j,3} \big]^\top \in \mathbb{R}^{18\times 1} \end{aligned} \tag{2.12}$$
$$\theta^f = \left[\sin\omega_1 t,\ \cos\omega_1 t,\ \sin\omega_2 t,\ \cos\omega_2 t \right] \in \mathbb{R}^{1\times 4} \tag{2.13}$$
$$\begin{aligned} \theta^m = \big[& \sin\left(\omega_2 - \omega_1\right) t,\ \cos\left(\omega_2 - \omega_1\right) t, \\ & \sin 2\omega_1 t,\ \cos 2\omega_1 t, \\ & \sin 2\omega_2 t,\ \cos 2\omega_2 t, \end{aligned}$$

[5] Vectors θ^f and θ^m are functions of time, so a more accurate notation would be that of $\theta^f(t)$ and $\theta^m(t)$; time is omitted for simplicity.

$$\begin{aligned}
&\sin(2\omega_1-\omega_2)\,t,\ \cos(2\omega_1-\omega_2)\,t,\\
&\sin(2\omega_2-\omega_1)\,t,\ \cos(2\omega_2-\omega_1)\,t\\
&\sin(2\omega_1+\omega_2)\,t,\ \cos(2\omega_1+\omega_2)\,t,\\
&\sin(2\omega_2+\omega_1)\,t,\ \cos(2\omega_2+\omega_1)\,t,\\
&\sin 3\omega_1 t,\ \cos 3\omega_1 t,\\
&\sin 3\omega_2 t,\ \cos 3\omega_2 t\Big] \in \mathbb{R}^{1\times 18}. \qquad (2.14)
\end{aligned}$$

The excitation current source of node j, $\hat{i}_j$, is described in the same way by

$$\hat{i}_j = \hat{i}_j^f + \hat{i}_j^m \qquad (2.15a)$$

$$\hat{i}_j^f = \theta^f P_j^f \qquad (2.15b)$$

$$\hat{i}_j^m = \theta^m P_j^m \qquad (2.15c)$$

where

$$P_j^f = \left[\hat{a}_{j,1},\ \hat{b}_{j,1},\ \hat{c}_{j,1},\ \hat{d}_{j,1}\right]^\top \in \mathbb{R}^{4\times 1} \qquad (2.16)$$

$$\begin{aligned}
P_j^m = \Big[&\hat{\ell}_j,\ \hat{m}_j,\ \hat{a}_{j,2},\ \hat{b}_{j,2},\ \hat{c}_{j,2},\ \hat{d}_{j,2},\ \hat{e}_j,\ \hat{f}_j,\ \hat{h}_j,\ \hat{r}_j,\\
&\hat{p}_j,\ \hat{\nu}_j,\ \hat{x}_j,\ \hat{y}_j,\ \hat{a}_{j,3},\ \hat{b}_{j,3},\ \hat{c}_{j,3},\ \hat{d}_{j,3}\Big]^\top \in \mathbb{R}^{18\times 1}. \qquad (2.17)
\end{aligned}$$

For convenience, it is assumed that there is only one excitation signal in the circuit under consideration, and it is placed at node 0. If more than one excitation signals exist, they are included as independent current sources at the corresponding nodes.

The estimation of IM_3 requires the estimation of the fundamental tones coefficients and the coefficients of the intermodulation products; that is, it is required to know vector S_j^f and the elements e_j, f_j, h_j, and r_j of S_j^m, for all j; thus, to compute S_j^f and S_j^m, for all j.

2.3.1 Fundamental Tones Estimation

The fundamental tones at ω_1 and ω_2 are expected to be unaltered by involvement of intermodulation and harmonic products since all G_m–stages are assumed to have weakly nonlinear behavior [22]. As such, the component (2.10b) of each node j should satisfy the linear part of (2.9). Thus, the output current of stage $G_{i,t,j}^m$, i_{itj}^f, is considered to be the linear part of (2.3)

$$i_{itj}^f = \theta^f\left(g_{itj}^{10} S_i^f - g_{itj}^{10} k_{itj} S_t^f + g_{itj}^{01} S_j^f\right). \qquad (2.18)$$

Relying on (2.9), the above expression of i_{itj}^f can be exploited in order to form

a system of equations for the coefficients of the fundamental tones of the complete circuit. Let

$$L_\omega^f = \operatorname{diag}(\omega_1, \omega_2) \otimes \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \in \mathbb{R}^{4\times 4} \tag{2.19}$$

where diag(...) is a diagonal matrix, and $\otimes$ denotes the Kronecker's product [35]. Then, the derivative of (2.10b) can be expressed as

$$i_j^f = \dot{\theta}^f S_j^f = \theta^f L_\omega^f S_j^f. \tag{2.20}$$

The above results are valid for any $t \in \mathbb{R}$. Since θ^f consists of four linearly independent functions of time and embodies four independent equations with respect to the coefficients of sin and cos, it can be eliminated. Thus, the combination of (2.9), (2.18), and (2.20), followed by the elimination of θ^f, yields for node j

$$P_j^f + \sum_{i,t} g_{itj}^{10} S_i^f - \sum_{i,t} g_{itj}^{10} k_{itj} S_t^f + \sum_\ell \widetilde{C}_{\ell j} L_\omega^f S_\ell^f = \left(\frac{1}{R_j} - \sum_{i,t} g_{itj}^{01}\right) S_j^f + \left(C_j + \sum_\ell \widetilde{C}_{\ell j}\right) L_\omega^f S_j^f. \tag{2.21}$$

Let the vector of the coefficients of the fundamental tones of all voltages be

$$S^f = \left[\left(S_0^f\right)^\top, \left(S_1^f\right)^\top, \ldots, \left(S_n^f\right)^\top\right]^\top \in \mathbb{R}^{4(n+1)\times 1} \tag{2.22}$$

and, accordingly, consider the vector of the coefficients of the excitation current source[6]

$$P^f = \left[\left(P_0^f\right)^\top, \left(0,\ 0,\ 0,\ 0\right), \ldots, \left(0,\ 0,\ 0,\ 0\right)\right]^\top \in \mathbb{R}^{4(n+1)\times 1}. \tag{2.23}$$

Then, the equivalent of (2.21) for all nodes can be constructed in block–matrix form

$$P^f + \left(G^f + K^f + F^f\right) S^f = \left(T^f + W^f\right) S^f. \tag{2.24}$$

The matrices involved in (2.24) are defined as

$$G^f = \left[\sum_t g_{itj}^{10}\right]_{j,i=0}^{n} \otimes I_4 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{2.25}$$

$$K^f = \left[-\sum_i g_{itj}^{10} k_{itj}\right]_{j,t=0}^{n} \otimes I_4 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{2.26}$$

$$F^f = \left[\widetilde{C}_{\ell j}\right]_{j,\ell=0}^{n} \otimes L_\omega^f \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{2.27}$$

$$T^f = \operatorname{diag}\left(\left[\frac{1}{R_j} - \sum_{i,t} g_{itj}^{01}\right]_{j=0}^{n}\right) \otimes I_4 \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{2.28}$$

[6] If more than one excitation signals are present, they should be included at the corresponding entries of the vector.

$$W^f = \operatorname{diag}\left(\left[C_j + \sum_\ell \widetilde{C}_{\ell j}\right]_{j=0}^{n}\right) \otimes L_\omega^f \in \mathbb{R}^{4(n+1)\times 4(n+1)} \tag{2.29}$$

where I_n is the $n \times n$ identity matrix. The coefficients of the fundamental tones are immediately obtained by

$$S^f = \left[T^f - G^f - K^f + W^f - F^f\right]^{-1} P^f. \tag{2.30}$$

2.3.2 Intermodulation Products Estimation

The nonlinear terms of (2.3) are the cause of the generation of the intermodulation and harmonic products, (2.10c), in each node j. The estimation of the distortion terms by the inclusion of all generated terms in (2.3) after substitution of all voltages in the form of (2.10a) results in a nonlinear problem, that is challenging and not computationally efficient.

Inspecting (2.3) alongside (2.10a), it follows that the generated coefficients of the intermodulation and harmonic products will ultimately be a sum of products of

(a) only coefficients of fundamental tones,

(b) a single intermodulation or harmonic coefficient to the power of one and one or more fundamental tone coefficients,

(c) higher orders or products of intermodulation and harmonic coefficients.

Products (c) will contribute negligible power and can be safely ignored [22], for the amplitudes of the intermodulation and harmonic products are expected to be much smaller compared to the ones of the fundamental tones. As such, for the estimation of the intermodulation products, the output current of stage $G_{i,t,j}^m$ can be approximated by

$$i_{itj}^m = \theta^m \left[g_{itj}^{10} S_i^m - g_{itj}^{10} k_{itj} S_t^m + g_{itj}^{01} S_j^m + Z_{itj} + X_{itj}^\alpha S_i^m + X_{itj}^\beta S_t^m + X_{itj}^\gamma S_j^m\right]. \tag{2.31}$$

Equation (2.31) takes into account the linear part of (2.3) and the kept products (a) and (b), included in terms $\theta^m Z_{itj}$ and $\theta^m \left(X_{itj}^\alpha S_i^m + X_{itj}^\beta S_t^m + X_{itj}^\gamma S_j^m\right)$, respectively. The above reasoning results in a linear form of i_{itj}^m, making the estimation problem of the intermodulation coefficients linear. The terms introduced in (2.31) are given by

$$Z_{itj} = \left[\left(Z_{itj}^\alpha\right)^\top, \left(Z_{itj}^\beta\right)^\top, \left(Z_{itj}^\gamma\right)^\top\right]^\top \in \mathbb{R}^{18\times 1} \tag{2.32}$$

where

$$Z^{\alpha}_{itj} = g^{20}_{itj}\widetilde{A}_{itj} + g^{02}_{itj}A_j + g^{11}_{itj}\frac{1}{2}\widetilde{H}_{itj} \in \mathbb{R}^{6\times 1} \tag{2.33}$$

$$Z^{\beta}_{itj} = g^{30}_{itj}\frac{3}{2}\widetilde{Y}_{itj} + g^{03}_{itj}\frac{3}{2}Y_j + g^{21}_{itj}\frac{1}{2}\widetilde{V}_{itj} + g^{12}_{itj}\frac{1}{2}V_{itj} \in \mathbb{R}^{8\times 1} \tag{2.34}$$

$$Z^{\gamma}_{itj} = g^{30}_{itj}\frac{1}{4}\widetilde{R}_{itj} \odot \widetilde{S}^{f}_{itj} + g^{03}_{itj}\frac{1}{4}R_j \odot S^{f}_{j} + g^{21}_{itj}\frac{1}{2}\widetilde{E}_{itj}S^{f}_{j} + g^{12}_{itj}\frac{1}{2}E_j\widetilde{S}^{f}_{itj} \in \mathbb{R}^{4\times 1} \tag{2.35}$$

and $\odot$ denotes the Hadamard's product [36]. Matrices X^{α}_{itj}, X^{β}_{itj}, and X^{γ}_{itj} are defined as

$$X^{\alpha}_{itj} = g^{20}_{itj}\widetilde{N}_{itj} + g^{30}_{itj}\frac{3}{2}\widetilde{M}_{itj} + g^{11}_{itj}\frac{1}{2}N_j + g^{21}_{itj}\frac{1}{2}Q_{itj} + g^{12}_{itj}\frac{1}{2}M_j \in \mathbb{R}^{18\times 18} \tag{2.36}$$

$$X^{\beta}_{itj} = -k_{itj}X^{\alpha}_{itj} \in \mathbb{R}^{18\times 18} \tag{2.37}$$

$$X^{\gamma}_{itj} = g^{02}_{itj}N_j + g^{03}_{itj}\frac{3}{2}M_j + g^{11}_{itj}\frac{1}{2}\widetilde{N}_{itj} + g^{21}_{itj}\frac{1}{2}\widetilde{M}_{itj} + g^{12}_{itj}\frac{1}{2}Q_{itj} \in \mathbb{R}^{18\times 18}. \tag{2.38}$$

The quantities that form the matrices of (2.33)–(2.38) are omitted for reading comprehension purposes. They can be found in the Appendix of this chapter.

In a similar manner to the estimation procedure of the coefficients of the fundamental tones, the expression (2.31) of i^{m}_{itj} is used to form the corresponding system of equations for the intermodulation coefficients, relying again on (2.9). Let

$$L^{m}_{\omega} = \operatorname{diag}\left(\omega_2 - \omega_1, 2\omega_1, 2\omega_2, 2\omega_1 - \omega_2, 2\omega_2 - \omega_1, 2\omega_1 + \omega_2, 2\omega_2 + \omega_1, 3\omega_1, 3\omega_2\right) \otimes \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.39}$$

to express the derivative of (2.10c)

$$\dot{u}^{m}_{j} = \dot{\theta}^{m}S^{m}_{j} = \theta^{m}L^{m}_{\omega}S^{m}_{j}. \tag{2.40}$$

By similar reasoning as earlier, vector function θ^{m} can be eliminated. Combining (2.9), (2.31), and (2.40), while eliminating θ^{m}, results in the following equation for node j

$$\left(P^{m}_{j} + \sum_{i,t} Z_{itj}\right) + \sum_{i,t} g^{10}_{itj}S^{m}_{i} - \sum_{i,t} g^{10}_{itj}k_{itj}S^{m}_{t} + \sum_{i,t}\left(X^{\alpha}_{itj}S^{m}_{i} + X^{\beta}_{itj}S^{m}_{t} + X^{\gamma}_{itj}S^{m}_{j}\right) + \sum_{\ell}\widetilde{C}_{\ell j}L^{m}_{\omega}S^{m}_{\ell} = \left(\frac{1}{R_j} - \sum_{i,t} g^{01}_{itj}\right)S^{m}_{j} + \left(C_j + \sum_{\ell}\widetilde{C}_{\ell j}\right)L^{m}_{\omega}S^{m}_{j}. \tag{2.41}$$

Consider the vector of the coefficients of the intermodulation products of all voltages of the circuit

$$S^m = \left[\left(S_0^m\right)^\top,\ \left(S_1^m\right)^\top,\ \ldots,\ \left(S_n^m\right)^\top \right]^\top \in \mathbb{R}^{18(n+1)\times 1} \tag{2.42}$$

and the vector of the excitation current source[7]

$$P^m = \left[\left(P_0^m\right)^\top,\ \overbrace{\left(0,\ \ldots,\ 0\right)}^{1\times 18},\ \ldots,\ \overbrace{\left(0,\ \ldots,\ 0\right)}^{1\times 18} \right]^\top \in \mathbb{R}^{18(n+1)\times 1}. \tag{2.43}$$

Moreover, define

$$B^m = P^m + Z^m \in \mathbb{R}^{18(n+1)\times 1} \tag{2.44}$$

where

$$Z^m = \left[\sum_{i,t} Z_{itj}\right]_{j=0}^{n} \in \mathbb{R}^{18(n+1)\times 1}. \tag{2.45}$$

As with the case of the fundamental tones, the equivalent of (2.21) for the complete circuit is grouped in block–matrix form

$$B^m + \left(G^m + K^m + X^m + F^m\right) S^m = \left(T^m + W^m\right) S^m \tag{2.46}$$

where

$$G^m = \left[\sum_t g_{itj}^{10}\right]_{j,i=0}^{n} \otimes I_{18} \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.47}$$

$$K^m = \left[-\sum_i g_{itj}^{10} k_{itj}\right]_{j,t=0}^{n} \otimes I_{18} \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.48}$$

$$F^m = \left[\widetilde{C}_{\ell j}\right]_{j,\ell=0}^{n} \otimes L_\omega^m \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.49}$$

$$T^m = \operatorname{diag}\left(\left[\tfrac{1}{R_j} - \sum_{i,t} g_{itj}^{01}\right]_{j=0}^{n}\right) \otimes I_{18} \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.50}$$

$$W^m = \operatorname{diag}\left(\left[C_j + \sum_\ell \widetilde{C}_{\ell j}\right]_{j=0}^{n}\right) \otimes L_\omega^m \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.51}$$

$$X^m = \left[\sum_t X_{itj}^\alpha\right]_{j,i=0}^{n} + \left[\sum_i X_{itj}^\beta\right]_{j,t=0}^{n} + \bigoplus_{j=0}^{n} \left[\sum_{i,t} X_{itj}^\gamma\right] \in \mathbb{R}^{18(n+1)\times 18(n+1)} \tag{2.52}$$

and $\bigoplus$ denotes the direct sum of matrices [36]. The desired coefficients of the intermodulation products are given by

$$S^m = \left[T^m - G^m - K^m - X^m + W^m - F^m\right]^{-1} B^m \tag{2.53}$$

[7] In the case of more than one excitation signals being present, they should be added at the corresponding entries of the vector.

and the IM_3 can be estimated at any node j as

$$\mathrm{IM}_3^j = 10\log_{10}\left(\frac{e_j^2+f_j^2+h_j^2+r_j^2}{a_{j,1}^2+b_{j,1}^2+c_{j,1}^2+d_{j,1}^2}\right). \tag{2.54}$$

An advantage of (2.54) over the classic approach of estimating IM_3 by the power ratio of the tone at $2\omega_1-\omega_2$ over that at ω_1, is that (2.54) takes into account the behavior of both input signals and the corresponding intermodulation products with respect to frequency. Moreover, it allows the input signals to feature different amplitude values.

The method offers a very fast distortion estimation due to its formulation; the estimation of IM_3 is acquired by the solution of two linear problems. Thus, the proposed method gives a closed–form solution, while methods like harmonic balance or shooting are iterative, and converge to a solution subject to a specific tolerance. Another advantage of the proposed method over methods like the aforementioned ones is that it is unaffected by the value of the beat frequency that may significantly slow down the latter.

2.4 Simulation Results

Two simulation cases validate the proposed intermodulation distortion estimation method. The two circuit examples are implemented in TSMC 90 nm technology, and the distortion results are obtained by Cadence Spectre parametric PSS–analysis in harmonic balance mode. In both cases, supply rails are set to $\pm 0.9\,\mathrm{V}$. The proposed method is implemented in MATLAB. The time of distortion estimation dropped from the order of minutes required during the parametric PSS–analysis, to the order of seconds when using the proposed method.

2.4.1 Two–Stage Feedback Amplifier

As a first example, the two–stage feedback amplifier of Figure 2.3 is tested. The amplifier has a feedback factor of $\beta = 0.10$, a DC–gain of 19.07 dB, and a unity–gain frequency of 7.03 MHz, under a load of $10\,\mathrm{k\Omega} \parallel 2\,\mathrm{pF}$.

Its equivalent G_m–stage representation is that of Figure 2.4; the differential–pair of M_0–M_4 is $G_{0,2,1}^m$, and the common–source stage of M_5–M_6 forms $G_{1,r,2}^m$. Miller capacitor C_C is represented by $\widetilde{C}_{12}$, $R_{L_1}+R_{L_2}=R_L$ by R_2, and C_L by C_2. Finally, the amplifier's feedback factor is captured by $k_{021} = {}^{R_{L_2}}/_{(R_{L_1}+R_{L_2})}$, and the ac–input signal is realized by the current source $\hat{i}_0 = u_{in}/R_0$ that is injected in $R_0 = 1\,\Omega$.

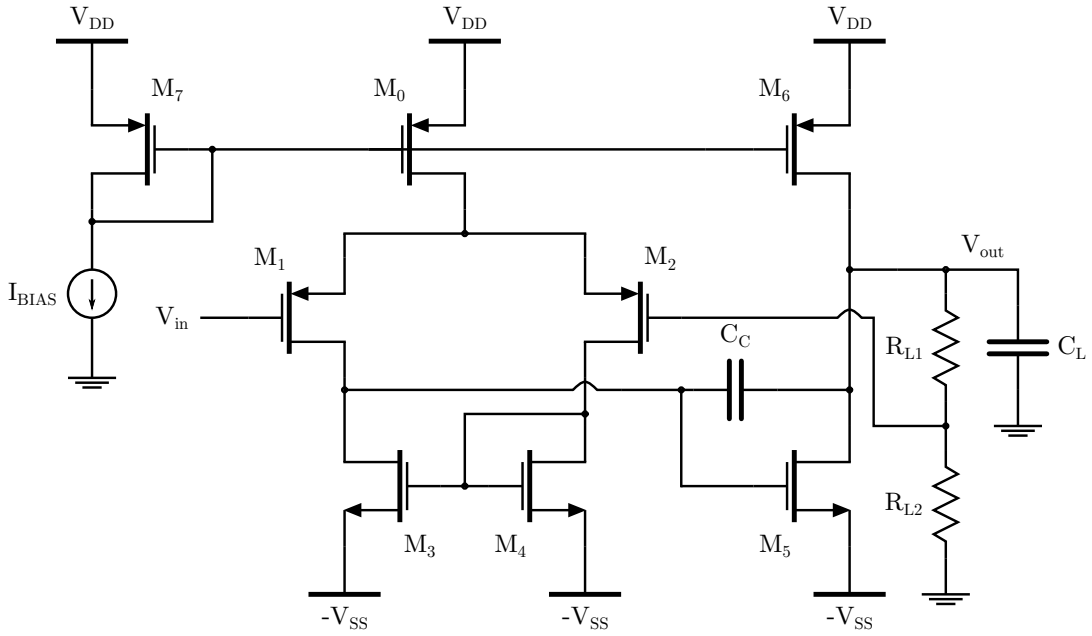

Figure 2.3: Two–stage feedback amplifier.

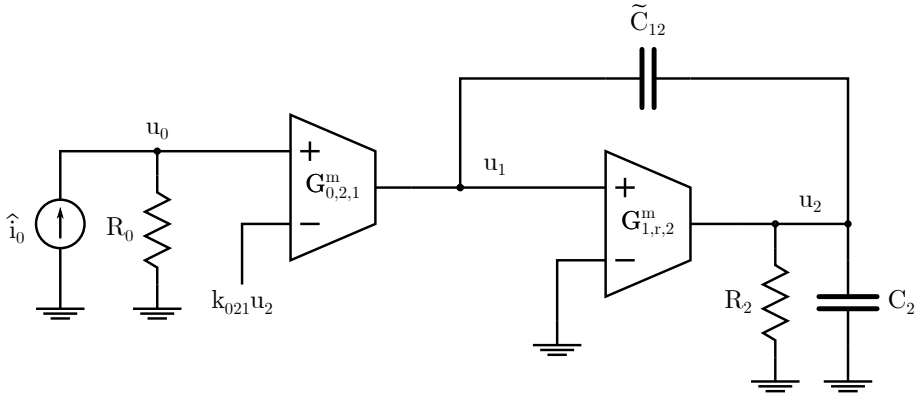

Figure 2.4: G_m–stage equivalent representation of the two–stage feedback amplifier.

The amplifier is driven by two signals with an amplitude of 20 mV peak, and fundamental frequencies of $\omega_1 = 2\pi\left(1-\delta_f\right)f$ and $\omega_2 = 2\pi\left(1+\delta_f\right)f$. Figures 2.5–2.7 depict the comparison of the IM_3 results obtained by simulation to the ones of the proposed method, for $\delta_f = 0.01$, $\delta_f = 0.05$, and $\delta_f = 0.10$. The error in the entire frequency range is found to be less than 0.41 dB for all three cases of δ_f, indicating a good agreement between the two results.

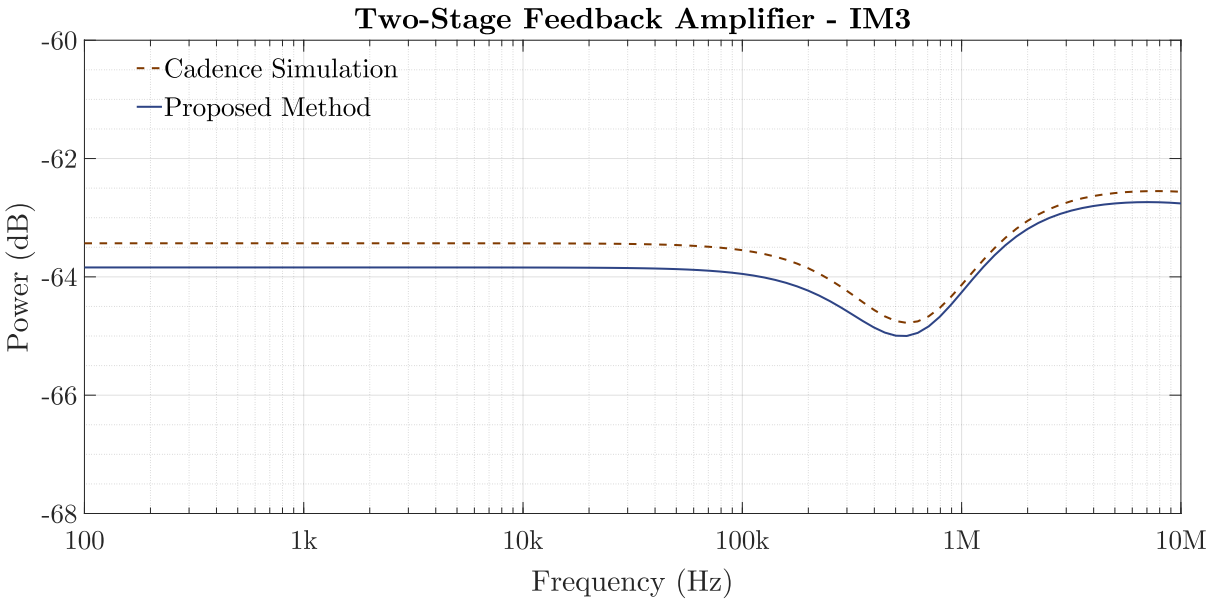

Figure 2.5: IM_3 of the two–stage feedback amplifier for $\delta_f = 0.01$.

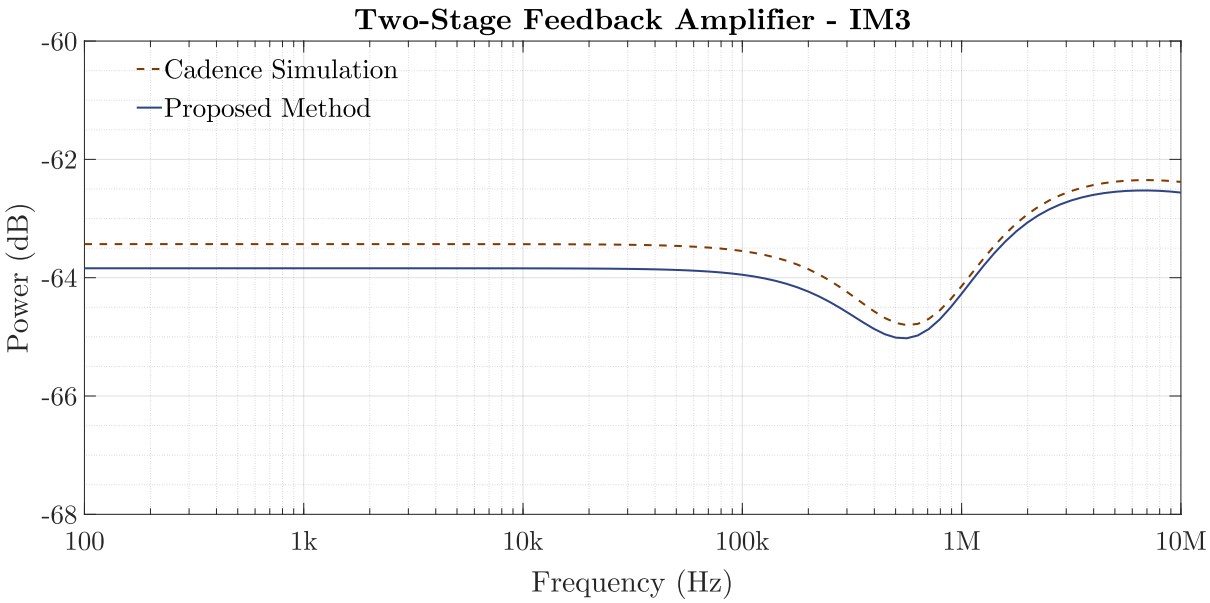

Figure 2.6: IM_3 of the two–stage feedback amplifier for $\delta_f = 0.05$.

2.4.2 Fourth–Order Butterworth Low–Pass Filter

Next, a fourth–order butterworth low–pass filter is simulated. The filter's architecture [37, 38] is shown in Figure 2.8, and the employed operational transconductance amplifier (OTA) is presented in Figure 2.9. The filter has a cut–off frequency of 98.82 kHz, and its G_m–stage equivalent representation of Figure 2.10 is immediately derived; each OTA is handled as a single G_m–stage, and the ac–input signal of the

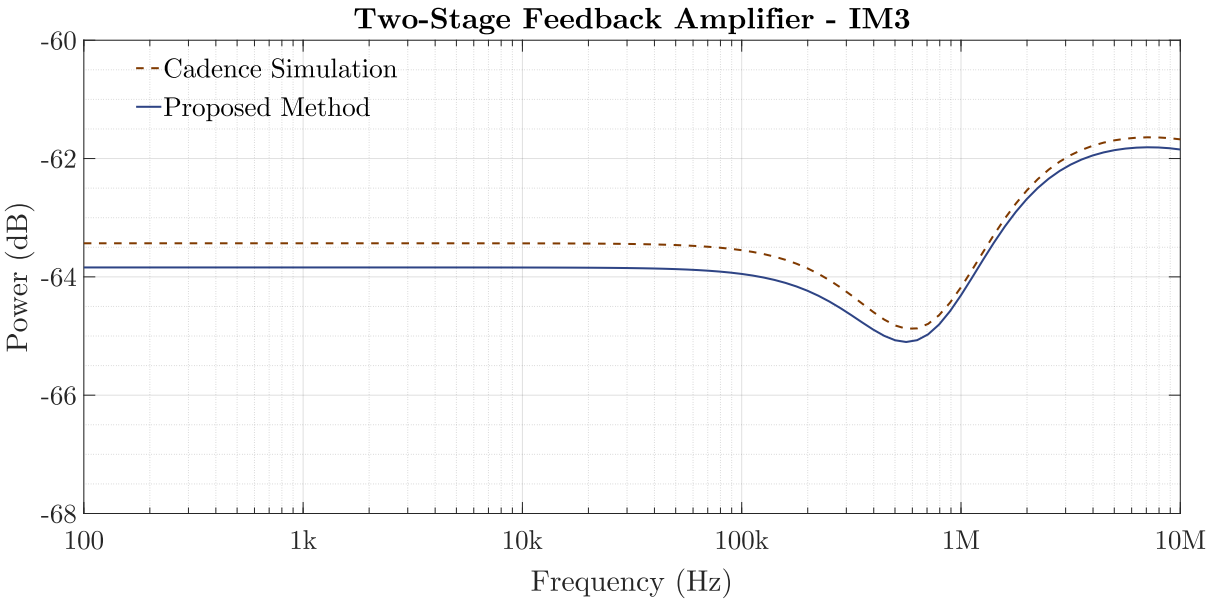

Figure 2.7: IM_3 of the two–stage feedback amplifier for $\delta_f = 0.10$.

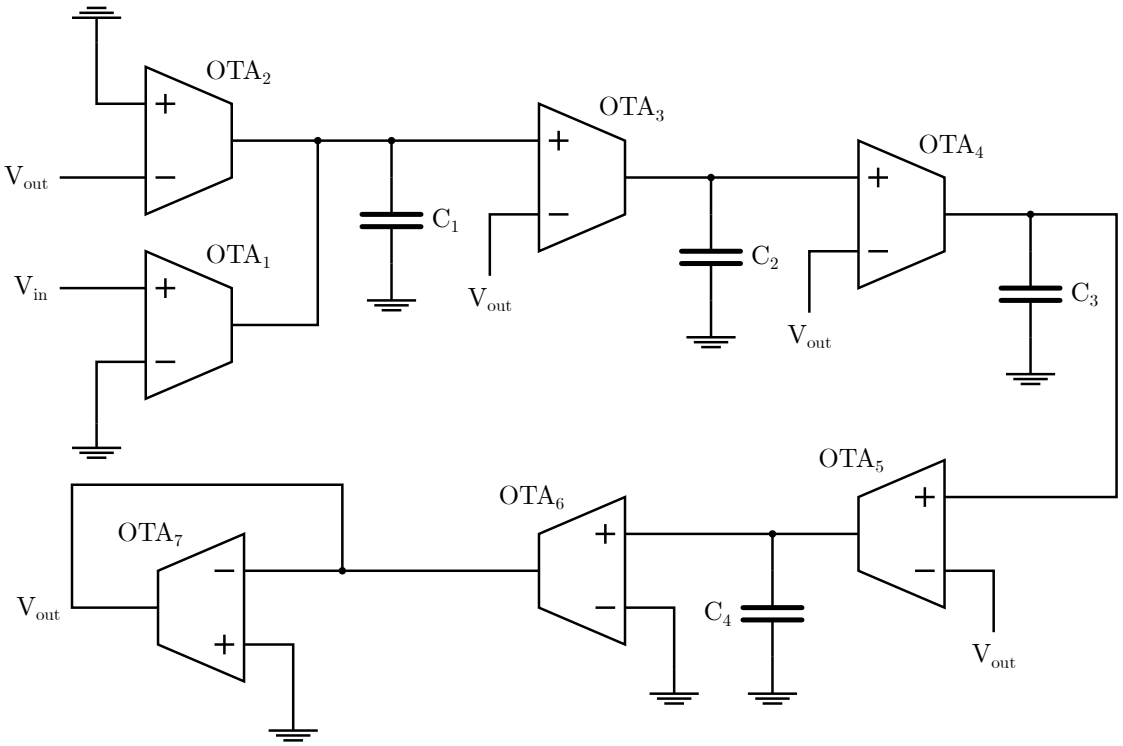

Figure 2.8: Fourth–order butterworth low–pass filter.

structure is again realized by the current source $\hat{i}_0 = u_{in}/R_0$ acting on $R_0 = 1\,\Omega$.

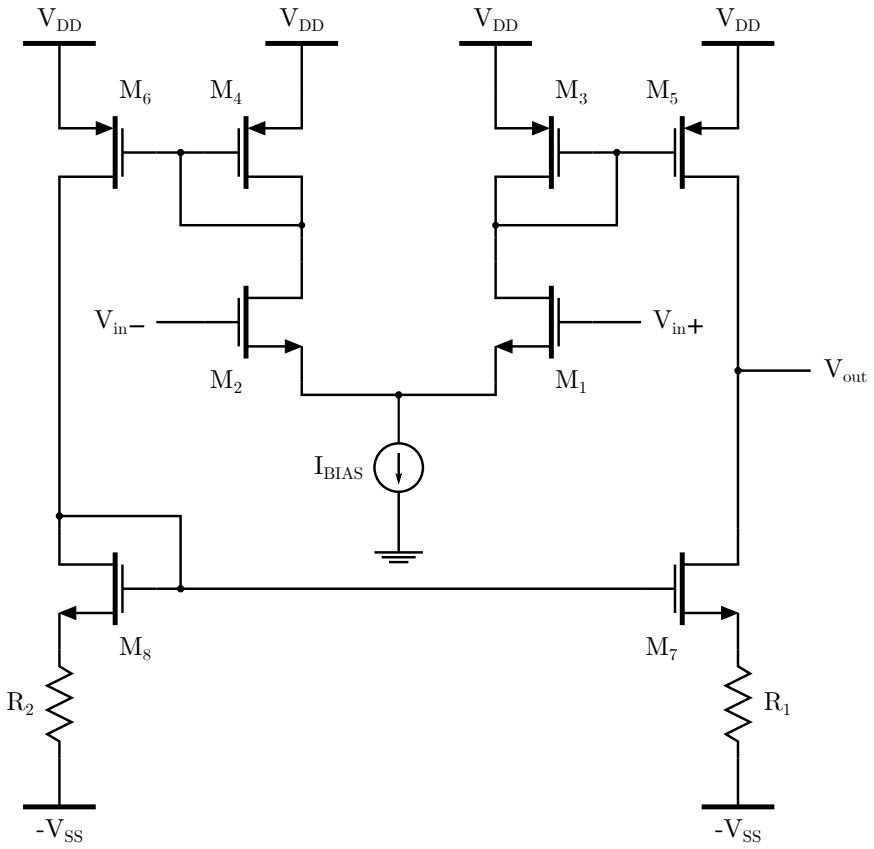

Figure 2.9: Employed OTA in the fourth–order butterworth low–pass filter.

With two signals of 100 mV peak amplitude, and fundamental frequencies of $\omega_1 = 2\pi\left(1-\delta_f\right)f$ and $\omega_2 = 2\pi\left(1+\delta_f\right)f$, the obtained IM_3 results for $\delta_f = 0.01$, $\delta_f = 0.05$, and $\delta_f = 0.10$ are given in Figures 2.11–2.13. The results of the proposed method are found to be in fine agreement with the simulation ones. In the entire frequency range the error is less than 0.67 dB for the case of $\delta_f = 0.01$, less than 0.58 dB for $\delta_f = 0.05$, and less than 0.51 dB for $\delta_f = 0.10$.

2.5 Summary

In this chapter, a general, time–domain method for estimation of intermodulation distortion in CMOS circuits is presented, that can be systematically applied to circuit topologies with any number of stages. It can be easily implemented in numerical computing environments like MATLAB or Python, and provides fast distortion results that are in good agreement with the ones obtained by Cadence Spectre simulation.

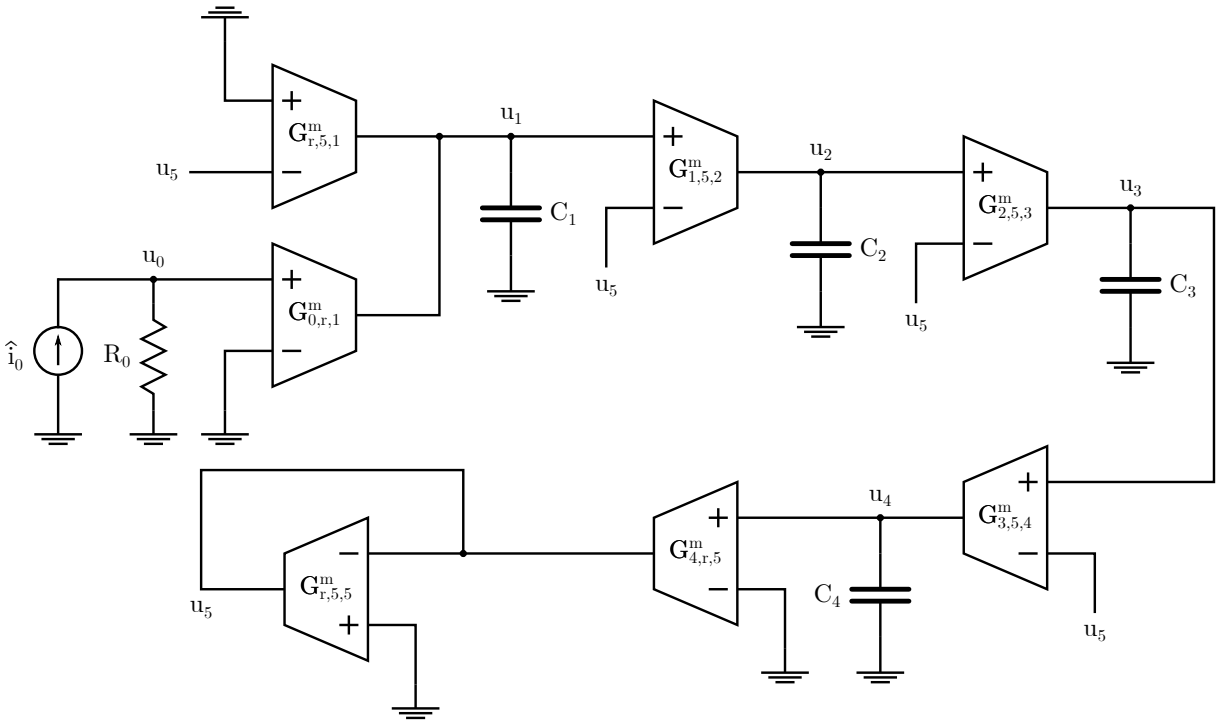

Figure 2.10: G_m–stage equivalent representation of the fourth–order butterworth low–pass filter.

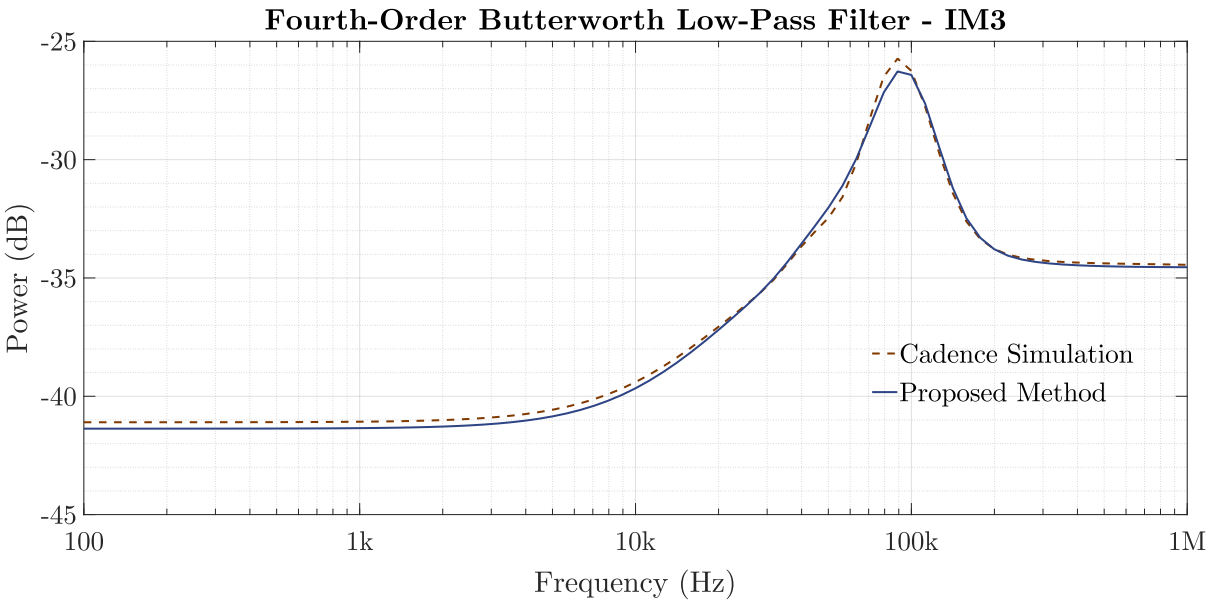

Figure 2.11: IM_3 of the fourth–order butterworth low–pass filter for $\delta_f = 0.01$.

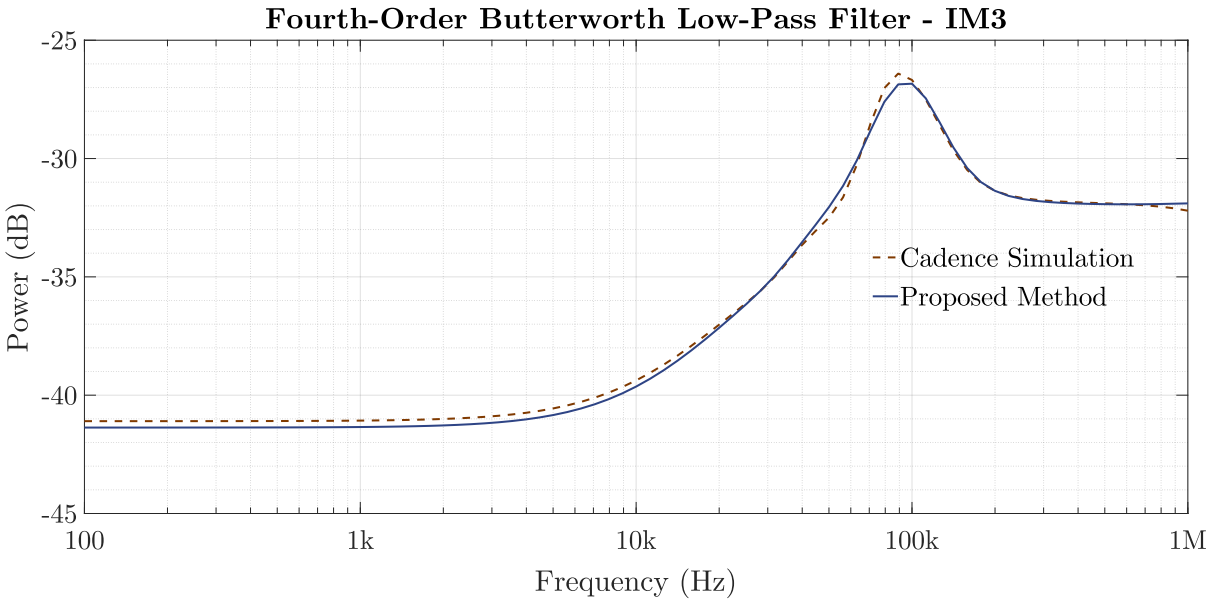

Figure 2.12: IM_3 of the fourth–order butterworth low–pass filter for $\delta_f = 0.05$.

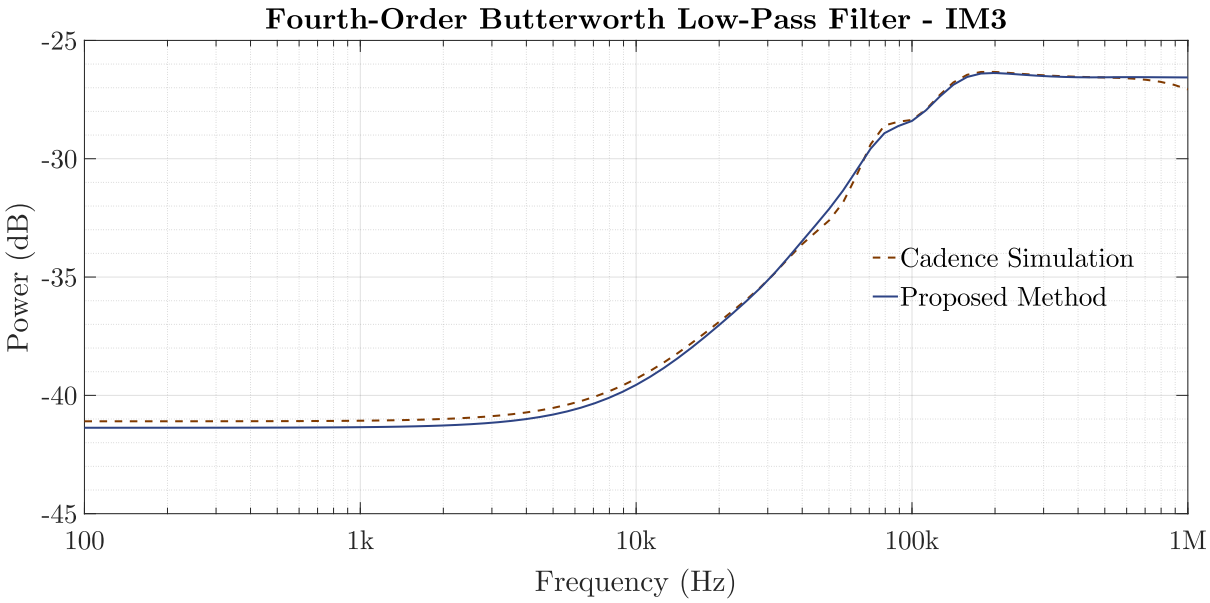

Figure 2.13: IM_3 of the fourth–order butterworth low–pass filter for $\delta_f = 0.10$.

Appendix: Quantities Forming (2.33)–(2.38)

Matrices (2.33)–(2.35) are formed by

$$\widetilde{A}_{itj} = \left[-\widetilde{m}^{\gamma}_{itj},\ \widetilde{m}^{\delta}_{itj},\ \widetilde{f}^{\alpha}_{itj},\ \widetilde{f}^{\beta}_{itj},\ \widetilde{f}^{\gamma}_{itj},\ \widetilde{f}^{\delta}_{itj}\right]^{\top} \in \mathbb{R}^{6\times 1} \tag{2.55}$$

$$A_j = \left[-m^{\gamma}_{j},\ m^{\delta}_{j},\ f^{\alpha}_{j},\ f^{\beta}_{j},\ f^{\gamma}_{j},\ f^{\delta}_{j}\right]^{\top} \in \mathbb{R}^{6\times 1} \tag{2.56}$$

$$\widetilde{H}_{itj} = \left[-q^{\gamma}_{itj},\ q^{\delta}_{itj},\ o^{\beta}_{itj},\ -o^{\alpha}_{itj},\ o^{\delta}_{itj},\ -o^{\gamma}_{itj}\right]^{\top} \in \mathbb{R}^{6\times 1} \tag{2.57}$$

$$\widetilde{Y}_{itj} = \widetilde{D}_{itj}\widetilde{S}^{f}_{itj} \in \mathbb{R}^{8\times 1} \tag{2.58}$$

$$Y_{j} = D_{j}S^{f}_{j} \in \mathbb{R}^{8\times 1} \tag{2.59}$$

$$\widetilde{V}_{itj} = \widetilde{D}_{itj}S^{f}_{j} + O_{itj}\widetilde{S}^{f}_{itj} \in \mathbb{R}^{8\times 1} \tag{2.60}$$

$$V_{itj} = D_{j}\widetilde{S}^{f}_{itj} + O_{itj}S^{f}_{j} \in \mathbb{R}^{8\times 1} \tag{2.61}$$

$$\widetilde{D}_{itj} = \begin{bmatrix} 0 & 0 & -\widetilde{f}^{\delta}_{itj} & \widetilde{f}^{\gamma}_{itj} & 0 & 0 & \widetilde{f}^{\delta}_{itj} & -\widetilde{f}^{\gamma}_{itj} \\ 0 & 0 & \widetilde{f}^{\gamma}_{itj} & \widetilde{f}^{\delta}_{itj} & 0 & 0 & \widetilde{f}^{\gamma}_{itj} & \widetilde{f}^{\delta}_{itj} \\ -\widetilde{f}^{\beta}_{itj} & \widetilde{f}^{\alpha}_{itj} & 0 & 0 & \widetilde{f}^{\beta}_{itj} & -\widetilde{f}^{\alpha}_{itj} & 0 & 0 \\ \widetilde{f}^{\alpha}_{itj} & \widetilde{f}^{\beta}_{itj} & 0 & 0 & \widetilde{f}^{\alpha}_{itj} & \widetilde{f}^{\beta}_{itj} & 0 & 0 \end{bmatrix}^{\top} \in \mathbb{R}^{8\times 4} \tag{2.62}$$

$$D_{j} = \begin{bmatrix} 0 & 0 & -f^{\delta}_{j} & f^{\gamma}_{j} & 0 & 0 & f^{\delta}_{j} & -f^{\gamma}_{j} \\ 0 & 0 & f^{\gamma}_{j} & f^{\delta}_{j} & 0 & 0 & f^{\gamma}_{j} & f^{\delta}_{j} \\ -f^{\beta}_{j} & f^{\alpha}_{j} & 0 & 0 & f^{\beta}_{j} & -f^{\alpha}_{j} & 0 & 0 \\ f^{\alpha}_{j} & f^{\beta}_{j} & 0 & 0 & f^{\alpha}_{j} & f^{\beta}_{j} & 0 & 0 \end{bmatrix}^{\top} \in \mathbb{R}^{8\times 4} \tag{2.63}$$

$$O_{itj} = \begin{bmatrix} 0 & 0 & o^{\gamma}_{itj} & o^{\delta}_{itj} & 0 & 0 & -o^{\gamma}_{itj} & -o^{\delta}_{itj} \\ 0 & 0 & o^{\delta}_{itj} & -o^{\gamma}_{itj} & 0 & 0 & o^{\delta}_{itj} & -o^{\gamma}_{itj} \\ o^{\alpha}_{itj} & o^{\beta}_{itj} & 0 & 0 & -o^{\alpha}_{itj} & -o^{\beta}_{itj} & 0 & 0 \\ o^{\beta}_{itj} & -o^{\alpha}_{itj} & 0 & 0 & o^{\beta}_{itj} & -o^{\alpha}_{itj} & 0 & 0 \end{bmatrix}^{\top} \in \mathbb{R}^{8\times 4} \tag{2.64}$$

$$\widetilde{R}_{itj} = \begin{bmatrix} -\widetilde{a}^{2}_{itj,1} + 3\widetilde{b}^{2}_{itj,1} \\ -3\widetilde{a}^{2}_{itj,1} + \widetilde{b}^{2}_{itj,1} \\ -\widetilde{c}^{2}_{itj,1} + 3\widetilde{d}^{2}_{itj,1} \\ -3\widetilde{c}^{2}_{itj,1} + \widetilde{d}^{2}_{itj,1} \end{bmatrix} \in \mathbb{R}^{4\times 1} \tag{2.65}$$

$$R_{j} = \begin{bmatrix} -a^{2}_{j,1} + 3b^{2}_{j,1} \\ -3a^{2}_{j,1} + b^{2}_{j,1} \\ -c^{2}_{j,1} + 3d^{2}_{j,1} \\ -3c^{2}_{j,1} + d^{2}_{j,1} \end{bmatrix} \in \mathbb{R}^{4\times 1} \tag{2.66}$$

$$\widetilde{E}_{itj} = \begin{bmatrix} \widetilde{f}^{\beta}_{itj} & \widetilde{f}^{\alpha}_{itj} & 0 & 0 \\ -\widetilde{f}^{\alpha}_{itj} & \widetilde{f}^{\beta}_{itj} & 0 & 0 \\ 0 & 0 & \widetilde{f}^{\delta}_{itj} & \widetilde{f}^{\gamma}_{itj} \\ 0 & 0 & -\widetilde{f}^{\gamma}_{itj} & \widetilde{f}^{\delta}_{itj} \end{bmatrix} \in \mathbb{R}^{4\times 4} \tag{2.67}$$

$$E_{j} = \begin{bmatrix} f^{\beta}_{j} & f^{\alpha}_{j} & 0 & 0 \\ -f^{\alpha}_{j} & f^{\beta}_{j} & 0 & 0 \\ 0 & 0 & f^{\delta}_{j} & f^{\gamma}_{j} \\ 0 & 0 & -f^{\gamma}_{j} & f^{\delta}_{j} \end{bmatrix} \in \mathbb{R}^{4\times 4} \tag{2.68}$$

where

$$\widetilde{m}^{\alpha}_{itj} = \widetilde{a}_{itj,1}\widetilde{c}_{itj,1} - \widetilde{b}_{itj,1}\widetilde{d}_{itj,1} \tag{2.69}$$
$$m^{\alpha}_{j} = a_{j,1}c_{j,1} - b_{j,1}d_{j,1} \tag{2.70}$$
$$\widetilde{m}^{\beta}_{itj} = \widetilde{a}_{itj,1}\widetilde{d}_{itj,1} + \widetilde{b}_{itj,1}\widetilde{c}_{itj,1} \tag{2.71}$$
$$m^{\beta}_{j} = a_{j,1}d_{j,1} + b_{j,1}c_{j,1} \tag{2.72}$$
$$\widetilde{m}^{\gamma}_{itj} = \widetilde{a}_{itj,1}\widetilde{d}_{itj,1} - \widetilde{b}_{itj,1}\widetilde{c}_{itj,1} \tag{2.73}$$
$$m^{\gamma}_{j} = a_{j,1}d_{j,1} - b_{j,1}c_{j,1} \tag{2.74}$$
$$\widetilde{m}^{\delta}_{itj} = \widetilde{a}_{itj,1}\widetilde{c}_{itj,1} + \widetilde{b}_{itj,1}\widetilde{d}_{itj,1} \tag{2.75}$$
$$m^{\delta}_{j} = a_{j,1}c_{j,1} + b_{j,1}d_{j,1} \tag{2.76}$$
$$\widetilde{f}^{\alpha}_{itj} = \widetilde{a}_{itj,1}\widetilde{b}_{itj,1} \tag{2.77}$$
$$f^{\alpha}_{j} = a_{j,1}b_{j,1} \tag{2.78}$$
$$\widetilde{f}^{\beta}_{itj} = \frac{-\widetilde{a}^{2}_{itj,1} + \widetilde{b}^{2}_{itj,1}}{2} \tag{2.79}$$
$$f^{\beta}_{j} = \frac{-a^{2}_{j,1} + b^{2}_{j,1}}{2} \tag{2.80}$$
$$\widetilde{f}^{\gamma}_{itj} = \widetilde{c}_{itj,1}\widetilde{d}_{itj,1} \tag{2.81}$$
$$f^{\gamma}_{j} = c_{j,1}d_{j,1} \tag{2.82}$$
$$\widetilde{f}^{\delta}_{itj} = \frac{-\widetilde{c}^{2}_{itj,1} + \widetilde{d}^{2}_{itj,1}}{2} \tag{2.83}$$
$$f^{\delta}_{j} = \frac{-c^{2}_{j,1} + d^{2}_{j,1}}{2} \tag{2.84}$$
$$o^{\alpha}_{itj} = \widetilde{a}_{itj,1}a_{j,1} - \widetilde{b}_{itj,1}b_{j,1} \tag{2.85}$$
$$q^{\alpha}_{itj} = \widetilde{a}_{itj,1}c_{j,1} + \widetilde{c}_{itj,1}a_{j,1} - \widetilde{b}_{itj,1}d_{j,1} - \widetilde{d}_{itj,1}b_{j,1} \tag{2.86}$$
$$o^{\beta}_{itj} = \widetilde{a}_{itj,1}b_{j,1} + \widetilde{b}_{itj,1}a_{j,1} \tag{2.87}$$
$$q^{\beta}_{itj} = \widetilde{a}_{itj,1}d_{j,1} + \widetilde{d}_{itj,1}a_{j,1} + \widetilde{b}_{itj,1}c_{j,1} + \widetilde{c}_{itj,1}b_{j,1} \tag{2.88}$$
$$o^{\gamma}_{itj} = \widetilde{c}_{itj,1}c_{j,1} - \widetilde{d}_{itj,1}d_{j,1} \tag{2.89}$$
$$q^{\gamma}_{itj} = \widetilde{a}_{itj,1}d_{j,1} + \widetilde{d}_{itj,1}a_{j,1} - \widetilde{b}_{itj,1}c_{j,1} - \widetilde{c}_{itj,1}b_{j,1} \tag{2.90}$$
$$o^{\delta}_{itj} = \widetilde{c}_{itj,1}d_{j,1} + \widetilde{d}_{itj,1}c_{j,1} \tag{2.91}$$
$$q^{\delta}_{itj} = \widetilde{a}_{itj,1}c_{j,1} + \widetilde{c}_{itj,1}a_{j,1} + \widetilde{b}_{itj,1}d_{j,1} + \widetilde{d}_{itj,1}b_{j,1} \tag{2.92}$$

and

$$\widetilde{S}^{f}_{itj} = S^{f}_{i} - k_{itj}S^{f}_{t} \in \mathbb{R}^{4\times 1}$$

that also implies $\widetilde{a}_{itj,1} = a_{i,1} - k_{itj}a_{t,1}$, $\widetilde{b}_{itj,1} = b_{i,1} - k_{itj}b_{t,1}$, $\widetilde{c}_{itj,1} = c_{i,1} - k_{itj}c_{t,1}$, and $\widetilde{d}_{itj,1} = d_{i,1} - k_{itj}d_{t,1}$. All vectors S_i^f, S_t^f, and S_j^f are known from the solution of S^f by (2.30).

Finally, the forming matrices of (2.36)–(2.38) are defined as

$$\widetilde{N}_{itj} = \begin{bmatrix} 0_6 & \widetilde{\Theta}_{itj}^{\widetilde{N}} & \widetilde{\Xi}_{itj}^{\widetilde{N}} \\ \left(\widetilde{\Theta}_{itj}^{\widetilde{N}}\right)^\top & 0_6 & 0_6 \\ \left(\widetilde{\Xi}_{itj}^{\widetilde{N}}\right)^\top & 0_6 & 0_6 \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.93}$$

$$N_j = \begin{bmatrix} 0_6 & \Theta_j^N & \Xi_j^N \\ \left(\Theta_j^N\right)^\top & 0_6 & 0_6 \\ \left(\Xi_j^N\right)^\top & 0_6 & 0_6 \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.94}$$

$$\widetilde{M}_{itj} = \left(\widetilde{S}_{itj}^f\right)^\top \widetilde{S}_{itj}^f I_{18} + \begin{bmatrix} \widetilde{\Theta}_{itj}^{\widetilde{M}} & 0_6 & 0_6 \\ 0_6 & \widetilde{\Xi}_{itj}^{\widetilde{M}} & \widetilde{\Phi}_{itj}^{\widetilde{M}} \\ 0_6 & \left(\widetilde{\Phi}_{itj}^{\widetilde{M}}\right)^\top & \widetilde{\Psi}_{itj}^{\widetilde{M}} \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.95}$$

$$M_j = \left(S_j^f\right)^\top S_j^f I_{18} + \begin{bmatrix} \Theta_j^M & 0_6 & 0_6 \\ 0_6 & \Xi_j^M & \Phi_j^M \\ 0_6 & \left(\Phi_j^M\right)^\top & \Psi_j^M \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.96}$$

$$Q_{itj} = 2\left(\widetilde{S}_{itj}^f\right)^\top S_j^f I_{18} + \begin{bmatrix} \Theta_{itj}^Q & 0_6 & 0_6 \\ 0_6 & \Xi_{itj}^Q & \Phi_{itj}^Q \\ 0_6 & \left(\Phi_{itj}^Q\right)^\top & \Psi_{itj}^Q \end{bmatrix} \in \mathbb{R}^{18\times 18} \tag{2.97}$$

where 0_n denotes the $n \times n$ zero matrix, and

$$\widetilde{\Theta}_{itj}^{\widetilde{N}} = \begin{bmatrix} -\widetilde{b}_{itj,1} & \widetilde{a}_{itj,1} & \widetilde{d}_{itj,1} & -\widetilde{c}_{itj,1} & 0 & 0 \\ \widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} & \widetilde{c}_{itj,1} & \widetilde{d}_{itj,1} & 0 & 0 \\ \widetilde{d}_{itj,1} & \widetilde{c}_{itj,1} & 0 & 0 & \widetilde{d}_{itj,1} & -\widetilde{c}_{itj,1} \\ -\widetilde{c}_{itj,1} & \widetilde{d}_{itj,1} & 0 & 0 & \widetilde{c}_{itj,1} & \widetilde{d}_{itj,1} \\ 0 & 0 & \widetilde{b}_{itj,1} & \widetilde{a}_{itj,1} & 0 & 0 \\ 0 & 0 & -\widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.98}$$

$$\Theta_j^N = \begin{bmatrix} -b_{j,1} & a_{j,1} & d_{j,1} & -c_{j,1} & 0 & 0 \\ a_{j,1} & b_{j,1} & c_{j,1} & d_{j,1} & 0 & 0 \\ d_{j,1} & c_{j,1} & 0 & 0 & d_{j,1} & -c_{j,1} \\ -c_{j,1} & d_{j,1} & 0 & 0 & c_{j,1} & d_{j,1} \\ 0 & 0 & b_{j,1} & a_{j,1} & 0 & 0 \\ 0 & 0 & -a_{j,1} & b_{j,1} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.99}$$

$$\widetilde{\Xi}_{itj}^{\widetilde{N}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \widetilde{b}_{itj,1} & -\widetilde{a}_{itj,1} & 0 & 0 \\ 0 & 0 & \widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} & 0 & 0 \\ \widetilde{b}_{itj,1} & -\widetilde{a}_{itj,1} & 0 & 0 & \widetilde{d}_{itj,1} & -\widetilde{c}_{itj,1} \\ \widetilde{a}_{itj,1} & \widetilde{b}_{itj,1} & 0 & 0 & \widetilde{c}_{itj,1} & \widetilde{d}_{itj,1} \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.100}$$

$$\Xi_{j}^{N} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & b_{j,1} & -a_{j,1} & 0 & 0 \\ 0 & 0 & a_{j,1} & b_{j,1} & 0 & 0 \\ b_{j,1} & -a_{j,1} & 0 & 0 & d_{j,1} & -c_{j,1} \\ a_{j,1} & b_{j,1} & 0 & 0 & c_{j,1} & d_{j,1} \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.101}$$

$$\widetilde{\Theta}_{itj}^{\widetilde{M}} = \begin{bmatrix} 0 & 0 & \widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & -\widetilde{m}_{itj}^{\beta} \\ 0 & 0 & \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} \\ \widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & 0 & 0 & 0 & 0 \\ \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & 0 & 0 & 0 & 0 \\ -\widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & 0 & 0 & 0 & 0 \\ -\widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.102}$$

$$\Theta_{j}^{M} = \begin{bmatrix} 0 & 0 & m_{j}^{\alpha} & m_{j}^{\beta} & -m_{j}^{\alpha} & -m_{j}^{\beta} \\ 0 & 0 & m_{j}^{\beta} & -m_{j}^{\alpha} & m_{j}^{\beta} & -m_{j}^{\alpha} \\ m_{j}^{\alpha} & m_{j}^{\beta} & 0 & 0 & 0 & 0 \\ m_{j}^{\beta} & -m_{j}^{\alpha} & 0 & 0 & 0 & 0 \\ -m_{j}^{\alpha} & m_{j}^{\beta} & 0 & 0 & 0 & 0 \\ -m_{j}^{\beta} & -m_{j}^{\alpha} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.103}$$

$$\widetilde{\Xi}_{itj}^{\widetilde{M}} = \begin{bmatrix} 0 & 0 & \widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & \widetilde{f}_{itj}^{\delta} & -\widetilde{f}_{itj}^{\gamma} \\ 0 & 0 & \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & \widetilde{f}_{itj}^{\gamma} & \widetilde{f}_{itj}^{\delta} \\ \widetilde{m}_{itj}^{\alpha} & \widetilde{m}_{itj}^{\beta} & 0 & 0 & 0 & 0 \\ \widetilde{m}_{itj}^{\beta} & -\widetilde{m}_{itj}^{\alpha} & 0 & 0 & 0 & 0 \\ \widetilde{f}_{itj}^{\delta} & \widetilde{f}_{itj}^{\gamma} & 0 & 0 & 0 & 0 \\ -\widetilde{f}_{itj}^{\gamma} & \widetilde{f}_{itj}^{\delta} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.104}$$

$$\Xi_{j}^{M} = \begin{bmatrix} 0 & 0 & m_{j}^{\alpha} & m_{j}^{\beta} & f_{j}^{\delta} & -f_{j}^{\gamma} \\ 0 & 0 & m_{j}^{\beta} & -m_{j}^{\alpha} & f_{j}^{\gamma} & f_{j}^{\delta} \\ m_{j}^{\alpha} & m_{j}^{\beta} & 0 & 0 & 0 & 0 \\ m_{j}^{\beta} & -m_{j}^{\alpha} & 0 & 0 & 0 & 0 \\ f_{j}^{\delta} & f_{j}^{\gamma} & 0 & 0 & 0 & 0 \\ -f_{j}^{\gamma} & f_{j}^{\delta} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.105}$$

$$\widetilde{\Phi}^{\widetilde{M}}_{itj} = \begin{bmatrix} 0 & 0 & -\widetilde{m}^{\alpha}_{itj} & -\widetilde{m}^{\beta}_{itj} & 0 & 0 \\ 0 & 0 & \widetilde{m}^{\beta}_{itj} & -\widetilde{m}^{\alpha}_{itj} & 0 & 0 \\ \widetilde{f}^{\beta}_{itj} & -\widetilde{f}^{\alpha}_{itj} & 0 & 0 & -\widetilde{m}^{\alpha}_{itj} & -\widetilde{m}^{\beta}_{itj} \\ \widetilde{f}^{\alpha}_{itj} & \widetilde{f}^{\beta}_{itj} & 0 & 0 & \widetilde{m}^{\beta}_{itj} & -\widetilde{m}^{\alpha}_{itj} \\ \widetilde{m}^{\delta}_{itj} & \widetilde{m}^{\gamma}_{itj} & \widetilde{m}^{\delta}_{itj} & -\widetilde{m}^{\gamma}_{itj} & 0 & 0 \\ -\widetilde{m}^{\gamma}_{itj} & \widetilde{m}^{\delta}_{itj} & \widetilde{m}^{\gamma}_{itj} & \widetilde{m}^{\delta}_{itj} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.106}$$

$$\Phi^{M}_{j} = \begin{bmatrix} 0 & 0 & -m^{\alpha}_{j} & -m^{\beta}_{j} & 0 & 0 \\ 0 & 0 & m^{\beta}_{j} & -m^{\alpha}_{j} & 0 & 0 \\ f^{\beta}_{j} & -f^{\alpha}_{j} & 0 & 0 & -m^{\alpha}_{j} & -m^{\beta}_{j} \\ f^{\alpha}_{j} & f^{\beta}_{j} & 0 & 0 & m^{\beta}_{j} & -m^{\alpha}_{j} \\ m^{\delta}_{j} & m^{\gamma}_{j} & m^{\delta}_{j} & -m^{\gamma}_{j} & 0 & 0 \\ -m^{\gamma}_{j} & m^{\delta}_{j} & m^{\gamma}_{j} & m^{\delta}_{j} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.107}$$

$$\widetilde{\Psi}^{\widetilde{M}}_{itj} = \begin{bmatrix} 0 & 0 & 0 & 0 & \widetilde{m}^{\delta}_{itj} & \widetilde{m}^{\gamma}_{itj} \\ 0 & 0 & 0 & 0 & -\widetilde{m}^{\gamma}_{itj} & \widetilde{m}^{\delta}_{itj} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \widetilde{m}^{\delta}_{itj} & -\widetilde{m}^{\gamma}_{itj} & 0 & 0 & 0 & 0 \\ \widetilde{m}^{\gamma}_{itj} & \widetilde{m}^{\delta}_{itj} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.108}$$

$$\Psi^{M}_{j} = \begin{bmatrix} 0 & 0 & 0 & 0 & m^{\delta}_{j} & m^{\gamma}_{j} \\ 0 & 0 & 0 & 0 & -m^{\gamma}_{j} & m^{\delta}_{j} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ m^{\delta}_{j} & -m^{\gamma}_{j} & 0 & 0 & 0 & 0 \\ m^{\gamma}_{j} & m^{\delta}_{j} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.109}$$

$$\Theta^{Q}_{itj} = \begin{bmatrix} 0 & 0 & q^{\alpha}_{itj} & q^{\beta}_{itj} & -q^{\alpha}_{itj} & -q^{\beta}_{itj} \\ 0 & 0 & q^{\beta}_{itj} & -q^{\alpha}_{itj} & q^{\beta}_{itj} & -q^{\alpha}_{itj} \\ q^{\alpha}_{itj} & q^{\beta}_{itj} & 0 & 0 & 0 & 0 \\ q^{\beta}_{itj} & -q^{\alpha}_{itj} & 0 & 0 & 0 & 0 \\ -q^{\alpha}_{itj} & q^{\beta}_{itj} & 0 & 0 & 0 & 0 \\ -q^{\beta}_{itj} & -q^{\alpha}_{itj} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.110}$$

$$\Xi^{Q}_{itj} = \begin{bmatrix} 0 & 0 & q^{\alpha}_{itj} & q^{\beta}_{itj} & -o^{\gamma}_{itj} & -o^{\delta}_{itj} \\ 0 & 0 & q^{\beta}_{itj} & -q^{\alpha}_{itj} & o^{\delta}_{itj} & -o^{\gamma}_{itj} \\ q^{\alpha}_{itj} & q^{\beta}_{itj} & 0 & 0 & 0 & 0 \\ q^{\beta}_{itj} & -q^{\alpha}_{itj} & 0 & 0 & 0 & 0 \\ -o^{\gamma}_{itj} & o^{\delta}_{itj} & 0 & 0 & 0 & 0 \\ -o^{\delta}_{itj} & -o^{\gamma}_{itj} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.111}$$

$$\Phi^{Q}_{itj} = \begin{bmatrix} 0 & 0 & -q^{\alpha}_{itj} & -q^{\beta}_{itj} & 0 & 0 \\ 0 & 0 & q^{\beta}_{itj} & -q^{\alpha}_{itj} & 0 & 0 \\ -o^{\alpha}_{itj} & -o^{\beta}_{itj} & 0 & 0 & -q^{\alpha}_{itj} & -q^{\beta}_{itj} \\ o^{\beta}_{itj} & -o^{\alpha}_{itj} & 0 & 0 & q^{\beta}_{itj} & -q^{\alpha}_{itj} \\ q^{\delta}_{itj} & q^{\gamma}_{itj} & q^{\delta}_{itj} & -q^{\gamma}_{itj} & 0 & 0 \\ -q^{\gamma}_{itj} & q^{\delta}_{itj} & q^{\gamma}_{itj} & q^{\delta}_{itj} & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6} \tag{2.112}$$

$$\Psi^{Q}_{itj} = \begin{bmatrix} 0 & 0 & 0 & 0 & q^{\delta}_{itj} & q^{\gamma}_{itj} \\ 0 & 0 & 0 & 0 & -q^{\gamma}_{itj} & q^{\delta}_{itj} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ q^{\delta}_{itj} & -q^{\gamma}_{itj} & 0 & 0 & 0 & 0 \\ q^{\gamma}_{itj} & q^{\delta}_{itj} & 0 & 0 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{6\times 6}. \tag{2.113}$$

References

[1] P. Dobrovolny et al. "Analysis and compact behavioral modeling of nonlinear distortion in analog communication circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 22.9 (Sept. 2003), pp. 1215–1227.

[2] Piet Wambacq and Willy Sansen. *Distortion Analysis of Analog Integrated Circuits*. 1st ed. Vol. 451. The Springer International Series in Engineering and Computer Science. Springer US, 1998.

[3] Tony Chan Carusone, David Johns, and Kenneth Martin. *Analog Integrated Circuit Design*. 2nd ed. John Wiley & Sons, Inc., 2011.

[4] Rowan J. Gilmore and Michael B. Steer. "Nonlinear circuit analysis using the method of harmonic balance—A review of the art. Part I. Introductory concepts". In: *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering* 1.1 (1991), pp. 22–37.

[5] Stephen A. Maas. *Nonlinear Microwave and RF Circuits*. 2nd ed. Artech House, 2003.

[6] D. Tannir and R. Khazaka. "Moments-Based Computation of Intermodulation Distortion of RF Circuits". In: *IEEE Transactions on Microwave Theory and Techniques* 55.10 (Oct. 2007), pp. 2135–2146. DOI: 10.1109/tmtt.2007.906480.

[7] Dani Tannir and Roni Khazaka. "Computation of Intermodulation Distortion in RF Circuits Using Single-Tone Moments Analysis". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 29.7 (July 2010), pp. 1121–1125. DOI: 10.1109/tcad.2010.2044672.

[8] S. Narayanan. "Application of Volterra series to intermodulation distortion analysis of transistor feedback amplifiers". In: *IEEE Transactions on Circuit Theory* 17.4 (1970), pp. 518–527. DOI: 10.1109/tct.1970.1083157.

[9] J.J. Bussgang, L. Ehrman, and J.W. Graham. "Analysis of nonlinear systems with multiple inputs". In: *Proceedings of the IEEE* 62.8 (1974), pp. 1088–1119. DOI: 10.1109/proc.1974.9572.

[10] Peng Li and L. T. Pileggi. "Efficient per-nonlinearity distortion analysis for analog and RF circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 22.10 (Oct. 2003), pp. 1297–1309.

[11] Abdullah Elik, Zhaonian Zhang, and Paul P. Sotiriadis. "A State-Space Approach to Intermodulation Distortion Estimation in Fully Balanced Bandpass G_m– C Filters With Weak Nonlinearities". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 54.4 (Apr. 2007), pp. 829–844. DOI: 10.1109/tcsi.2006.887630.

[12] A. Cooman et al. "Distortion Contribution Analysis With the Best Linear Approximation". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.12 (Dec. 2018), pp. 4133–4146. ISSN: 1549-8328. DOI: 10.1109/TCSI.2018.2834139.

[13] G. Palumbo and S. Pennisi. "Feedback amplifiers: a simplified analysis of harmonic distortion in the frequency domain". In: *ICECS 2001. 8th IEEE International Conference on Electronics, Circuits and Systems (Cat. No.01EX483)*. Vol. 1. Sept. 2001, 209–212 vol.1. DOI: 10.1109/ICECS.2001.957717.

[14] G. Giustolisi, G. Palumbo, and S. Pennisi. "Harmonic distortion in single-stage amplifiers". In: *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*. Vol. 2. May 2002, pp. II–II. DOI: 10.1109/ISCAS.2002.1010916.

[15] G. Palumbo and S. Pennisi. "High-frequency harmonic distortion in feedback amplifiers: analysis and applications". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 50.3 (Mar. 2003), pp. 328–340. ISSN: 1057-7122. DOI: 10.1109/TCSI.2003.808835.

[16] G. Palumbo and S. Pennisi. "Harmonic distortion in three-stage nested-Miller-compensated amplifiers". In: *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*. Vol. 1. May 2004, pp. I–485. DOI: 10.1109/ISCAS.2004.1328237.

[17] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Accurate estimation of high-frequency harmonic distortion in two-stage Miller OTAs". In: *IEE Proceedings - Circuits, Devices and Systems* 152.5 (Oct. 2005), pp. 417–424. ISSN: 1350-2409. DOI: 10.1049/ip-cds:20045057.

[18] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Distortion analysis of three-stage amplifiers with reversed nested-Miller compensation". In: *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.* Vol. 3. Sept. 2005, III/93–III/96 vol. 3. DOI: 10.1109/ECCTD.2005.1523068.

[19] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "New analytical approach to evaluate harmonic distortion in nonlinear feedback amplifiers". In: *Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005.* Vol. 3. Sept. 2005, III/97–III100 vol. 3. DOI: 10.1109/ECCTD.2005.1523069.

[20] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "Distortion analysis of Miller-compensated three-stage amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 53.5 (May 2006), pp. 961–976. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.862287.

[21] S. O. Cannizzaro, G. Palumbo, and S. Pennisi. "An approach to model high-frequency distortion in negative-feedback amplifiers". In: *International Journal of Circuit Theory and Applications* 36.1 (2008), pp. 3–18.

[22] Dimitrios Baxevanakis and Paul P. Sotiriadis. "A General Time-Domain Method for Harmonic Distortion Estimation in CMOS Circuits". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 40.1 (Jan. 2021), pp. 157–170. DOI: 10.1109/tcad.2020.2988414.

[23] Sanghoon Kang, Byounggi Choi, and Bumman Kim. "Linearity analysis of CMOS for RF application". In: *IEEE Transactions on Microwave Theory and Techniques* 51.3 (Mar. 2003), pp. 972–977. ISSN: 0018-9480. DOI: 10.1109/TMTT.2003.808709.

[24] B. Toole, C. Plett, and M. Cloutier. "RF circuit implications of moderate inversion enhanced linear region in MOSFETs". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 51.2 (Feb. 2004), pp. 319–328. ISSN: 1549-8328. DOI: 10.1109/TCSI.2003.822400.

[25] G. Shi. "Symbolic Distortion Analysis of Multistage Amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.1 (Jan. 2019), pp. 369–382.

[26] Dimitrios Baxevanakis and Paul P. Sotiriadis. "Accurate Harmonic Distortion Estimation in CMOS Circuits using a Cross-Product Gm-Stage Modeling". In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS).* IEEE, Oct. 2020. DOI: 10.1109/iscas45731.2020.9181113.

[27] B. Hernes and W. Sansen. "Distortion in single-, two- and three-stage amplifiers". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.5 (May 2005), pp. 846–856. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.846214.

[28] S. C. Blaakmeer et al. "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling". In: *IEEE Journal of Solid-State Circuits* 43.6 (June 2008), pp. 1341–1350. ISSN: 0018-9200. DOI: 10.1109/JSSC.2008.922736.

[29] B. Perez-Verdu et al. "Nonlinear time-domain macromodeling of OTA circuits". In: *IEEE International Symposium on Circuits and Systems* 1989 (May 1989), 1441–1444 vol.2.

[30] Z. Zhang, A. Celik, and P. Sotiriadis. "A fast state-space algorithm to estimate harmonic distortion in fully differential weakly nonlinear G_m–C filters". In: *2006 IEEE International Symposium on Circuits and Systems (ISCAS)*. May 2006, 4 pp.–2956. DOI: 10.1109/ISCAS.2006.1693244.

[31] Zhaonian Zhang, A. Celik, and P. P. Sotiriadis. "State-space harmonic distortion modeling in weakly nonlinear, fully balanced G_m–C filters-a modular approach resulting in closed-form solutions". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 53.1 (Jan. 2006), pp. 48–59. ISSN: 1549-8328. DOI: 10.1109/TCSI.2005.854296.

[32] P. P. Sotiriadis et al. "Fast State-Space Harmonic-Distortion Estimation in Weakly Nonlinear G_m–C Filters". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 54.1 (Jan. 2007), pp. 218–228. ISSN: 1549-8328. DOI: 10.1109/TCSI.2006.887458.

[33] N. Scheinberg and A. Pinkhasov. "A computer simulation model for simulating distortion in FET resistors". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 19.9 (Sept. 2000), pp. 981–989.

[34] Harold Wayne Sorenson. *Parameter Estimation: Principles and Problems*. Vol. 9. Control and Systems Theory. M. Dekker, 1980.

[35] Peter Lancaster and Miron Tismenetsky. *The Theory of Matrices with Applications*. 2nd ed. Computer Science and Scientific Computing. Academic Press, 1985.

[36] Roger A. Horn and Charles R. Johnson. *Matrix Analysis*. Cambridge University Press, 2013.

[37] Slawomir Koziel, Stanislaw Szczepanski, and Rolf Schaumann. "Structure generation and performance comparison of elliptic Gm-C filters". In: *International Journal of Circuit Theory and Applications* 32.6 (2004), pp. 565–589. DOI: 10.1002/cta.296.

[38] Georgia Tsirimokou et al. "Comparative Study of Discrete Component Realizations of Fractional-Order Capacitor and Inductor Active Emulators". In: *Journal of Circuits, Systems and Computers* 27.11 (June 2018), p. 1850170. DOI: 10.1142/s0218126618501700.

Part II

A High–Linearity & High–Efficiency Power Stage Architecture

3 A High–Linearity, High–Efficiency Power Stage Architecture

This chapter presents a power stage architecture that combines high–linearity with high–efficiency. The power stage is configured as a push–pull Class–A topology with two buck–converters providing its supply rails. The buck–converters continuously track the stage's output with a small constant margin, creating a minimum, constant voltage drop on the output devices; thus, the stage's efficiency is increased and its linearity is improved. Theoretical analysis of the topology and its feedback control are presented, while a design example is implemented and simulated in Cadence Spectre in ON Semi CMOS 0.35 μm technology as proof–of–concept.

3.1 Introduction

Power amplifiers are one of the most commonly used blocks in electronic applications, with their power stage having a major impact on their overall linearity and power consumption [1]; two factors that are often in conflict. Linearity plays a crucial role in measurement applications and consumer ones, like audio, where power is always a constraint. Various power stage classes try to excel in one or both of these two aspects: Class–A stages offer superior linearity at the expense of efficiency; Class–B stages improve on efficiency but suffer from crossover distortion, while Class–AB topologies stay in between Class–A and Class–B in the efficiency metric. Switching output stages like Class–D and its variants, like Class–E (used mostly for RF applications), feature very high power efficiency, but lack in linearity compared to their non–switching counterparts.

An attempt to boost the efficiency of the linear family of output stages comes in the form of Class–G and Class–H power stages. These architectures usually feature an output stage biased in Class–AB (or more rarely, in Class–B), with multiple supply rails or a dynamic one. Class–G employs different supply levels with discrete steps based on the output signal's amplitude through a switching–selection mechanism, and has established itself to both audio [2, 3, 4] and RF applications [5, 6, 7]. One

aspect that requires attention is the switching noise introduced during the supply rails' selection [8], since it can severely degrade linearity.

Class–H stages use a dynamic approach. In their most common form, for small signal amplitudes a minimum fixed supply level is set; when the signal exceeds a threshold value, the supply rail dynamically tracks it with an added offset to keep the output devices in the appropriate operational region. When both positive and negative supply rails are available, they both stay fixed at low absolute voltages for small output level, and one of them tracks the output with an offset, when the output level exceeds certain thresholds [9, 10]. The same approach can be implemented in a fully–differential bridge configuration with a single supply rail [11, 12, 13].

Another flavor of Class–H power stages employs envelope–tracking of the output by the dynamic supply rail. For audio and low–frequency measurement purposes, envelope–tracking has been used in single–rail [14] implementations, and also in a mirrored dual–rail fashion [15], where both rails simultaneously increase or decrease in absolute value. It has also been used in RF applications where more sophisticated tracking schemes can cope with the more demanding signal bandwidths [16].

In this work, a high–linearity and high–efficiency power stage architecture based on the Class–H principles is presented. Instead of being biased in Class–AB or Class–B, the proposed stage's output devices are in a push–pull Class–A scheme (full–cycle conduction) to ensure high linearity. Two buck–converters constantly track the output voltage towards the same direction with an appropriate margin and generate the two supply rails; this way a constant voltage drop on the power transistors is maintained, maximizing the stage's efficiency and further increasing linearity.

This chapter is organized as follows. Section 3.2 presents the concept of the proposed power stage architecture, and Section 3.3 outlines its theoretical analysis and a feedback control scheme that can serve as a design guide. A proof–of–concept circuit implementation of the topology is given in Section 3.4, accompanied by Cadence Spectre simulation results in ON Semi CMOS 0.35 μm technology. Finally, a summary is given in Section 3.5.

3.2 Proposed Power Stage Architecture

The concept of the proposed power stage architecture is depicted in Figure 3.1. Both positive (u_R^+) and negative (u_R^-) supply rails continuously track the output signal, creating a constant voltage drop (u_M) on the output devices at all times. This scheme offers two advantages. First, power loss on output transistors is minimized; this has a profound effect for a push–pull Class–A topology where both devices conduct during a full cycle and unavoidably decrease the efficiency potential of the stage. Secondly, modulation of the transistors' currents due to the Early effect is ideally eliminated; thus, overall linearity of the stage is improved. The small error in the achieved margin

results in a minimal current modulation effect; the smaller this error, the better the stage's achieved linearity.

The system–level architecture of the proposed power stage is given in Figure 3.2. The two supply rails are generated by two buck–converters that track the output signal plus/minus a margin voltage, u_M. The power stage is biased in Class–A and is a push–pull configuration. The proposed architecture is general; it can employ MOSFET or BJT devices (or a combination of them), and can be implemented in either discrete–component or integrated circuit designs. Given the popularity and widespread use of MOSFETs, this work presents and analyzes a MOSFET version of the topology. For a MOSFET power stage, the selected u_M can be as small as the u_{DS} saturation value of the output devices plus a safety margin to prevent them from entering the triode region throughout the entire output range. The converters' duty cycles are shaped through feedback and pulse–width modulation (PWM). Buck–Boost–converters can also be used to provide larger output swing, but require a more complex driver for the output stage.

Given the continuous tracking of the output voltage by the power stage rails and the stage's Class–A biasing, the proposed topology is referred to as Class–CTA (*Continuously Tracking A*).

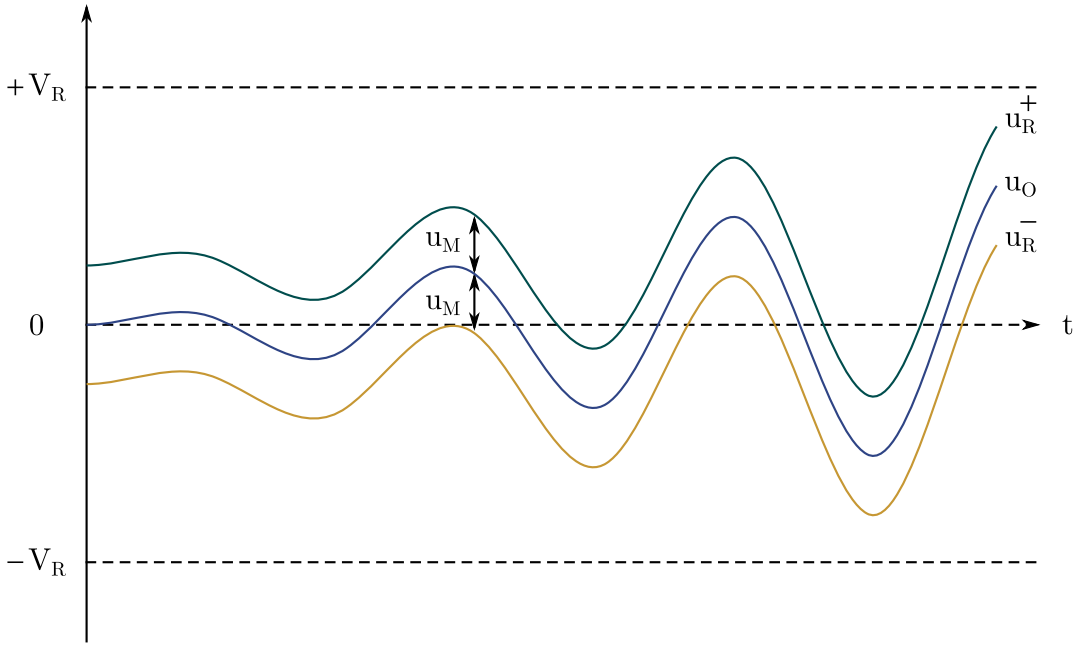

Figure 3.1: Proposed power stage's continuously tracking rails.

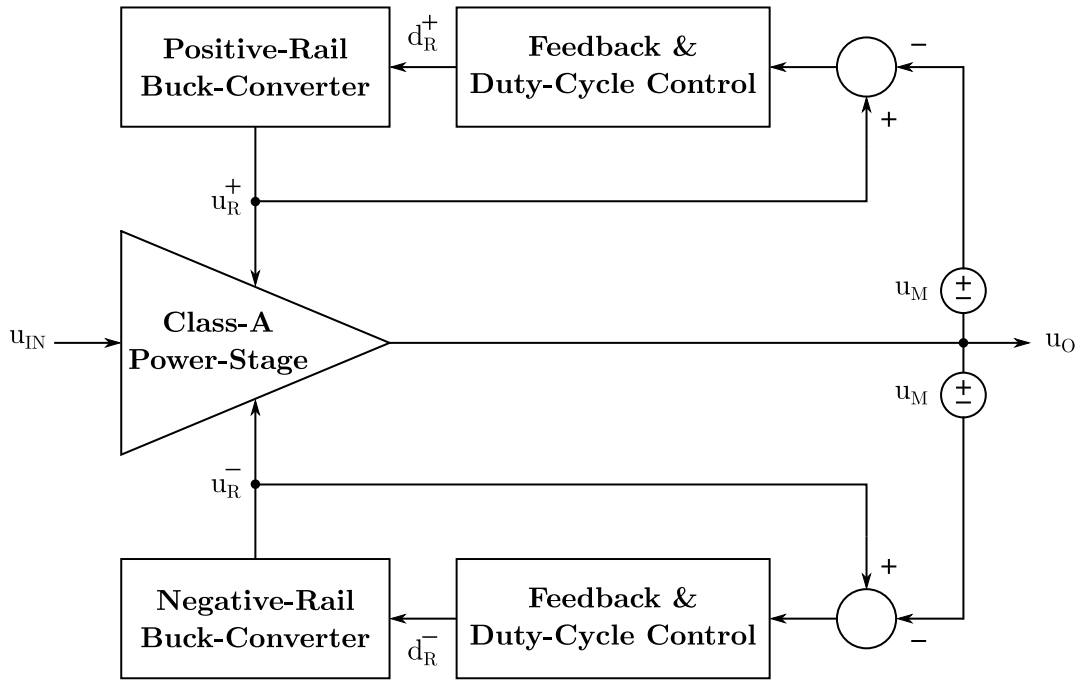

Figure 3.2: Proposed power stage's system–level architecture.

3.3 Class–CTA Theoretical Analysis

The proposed power stage can be divided into three blocks: the push–pull Class–A MOSFET power stage, the positive–rail buck–converter, and the negative–rail one. The blocks are modeled as shown in Figure 3.3. The analysis of Class–CTA starts with the power stage's biasing and its drawn current expressions, and continues on to the buck–converters. All equations required to implement the Class–CTA architecture are provided, so apart from establishing its theoretical background, the foregoing analysis also serves as a complete design guide for sizing the involved components.

3.3.1 MOSFET Push–Pull Class–A Power Stage

The push–pull power stage of the proposed design is formed by MOSFETs M_n and M_p in Figure 3.3. No degeneration resistances are present at their sources, given the smoother current square–law of MOSFETs versus the abrupt exponential–law of BJT devices. This also simplifies the foregoing large–signal, low–frequency analysis.

Note that the two feedback loops in Figure 3.2 maintain constant u_{DS} voltage for M_n and M_p, equal to u_M. Moreover, both M_n and M_p are desired to operate in strong–inversion and also to avoid mobility degradation; with these design requirements in mind, their drain currents are expressed as

$$i_{DS_n} = \zeta_n \left(u_{GS_n} - V_{tn}\right)^2$$

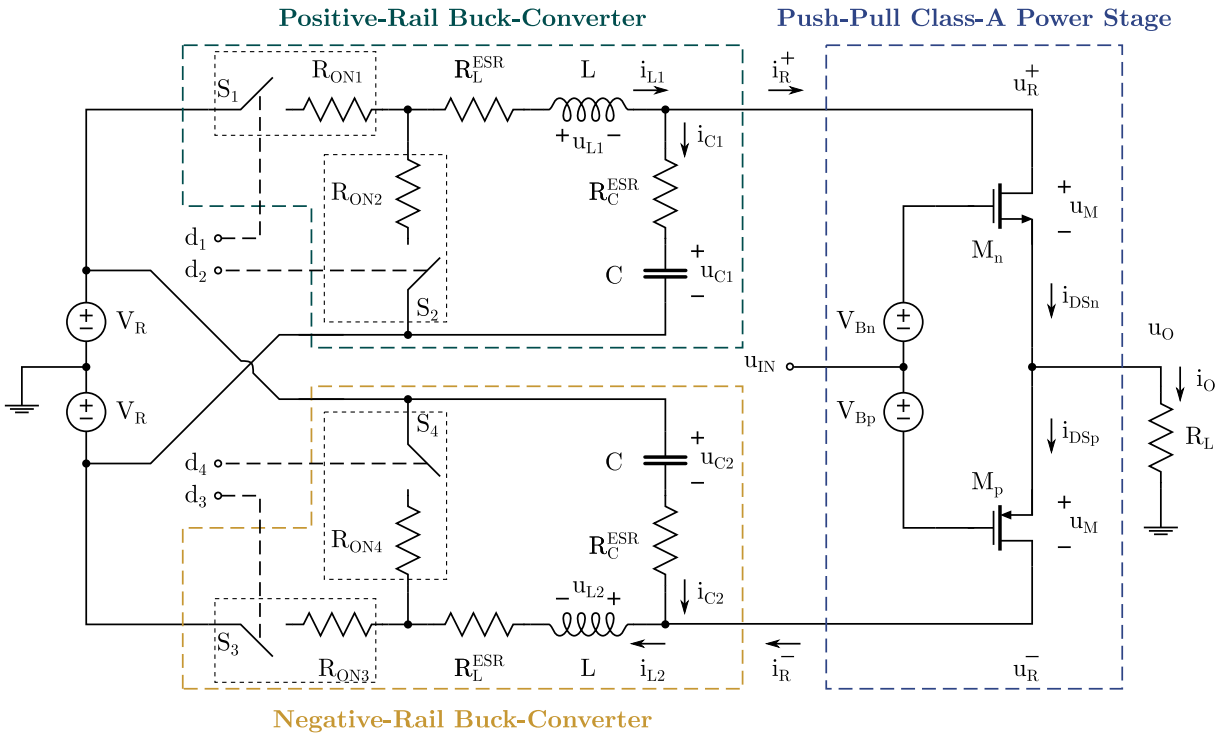

Figure 3.3: Class–CTA model.

$$i_{DS_p} = \zeta_p \left(u_{SG_p} - |V_{tp}|\right)^2, \tag{3.1}$$

where it is defined

$$\begin{aligned} \zeta_n &\triangleq \frac{i_{DS_n}}{V_{eff_n}^2} = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left(1+\lambda_n u_M\right) \\ \zeta_p &\triangleq \frac{i_{DS_p}}{V_{eff_p}^2} = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}\left(1+\lambda_p u_M\right). \end{aligned} \tag{3.2}$$

In the above expressions, V_{tn}, V_{tp} are the transistors' threshold voltages, and V_{eff_n}, V_{eff_p} are their effective voltages, equal to $(u_{GS_n} - V_{tn})$ and $(u_{SG_p} - |V_{tp}|)$, respectively. Finally, W_n, W_p, L_n, L_p represent the transistors' gate width and length values, μ_n, μ_p are their carrier mobilities, λ_n, λ_p depict their output impedance constants, and C_{ox} is the gate capacitance per unit area. [17]

Pure Class–A Biasing Conditions

The biasing of the output stage is set by the sum of voltages V_{B_n} and V_{B_p}, and it holds that

$$V_{B_n} + V_{B_p} = u_{GS_n} + u_{SG_p}. \tag{3.3}$$

It is convenient to define the positive DC bias voltage

$$V_A \triangleq V_{B_n} - V_{tn} + V_{B_p} - |V_{tp}| = V_{eff_n} + |V_{eff_p}|. \tag{3.4}$$

Then, using equation (3.1) that is desired to hold over the entire voltage range of operation, voltage V_A can be expressed as

$$V_A = \sqrt{\frac{i_{DS_n}}{\zeta_n}} + \sqrt{\frac{i_{DS_p}}{\zeta_p}}. \tag{3.5}$$

In order to have high–linearity Class–A operation, both transistors M_n and M_p must always be in strong–inversion. To achieve this, it is required that their currents are always larger than some minimum values, i.e. $i_{DS_n}^{min} > i_{lim}^{sat_n}$, $i_{DS_p}^{min} > i_{lim}^{sat_p}$, where

$$i_{lim}^{sat_{n,p}} = 16\mu_{n,p}C_{ox}\frac{W_{n,p}}{L_{n,p}}AU_T^2, \tag{3.6}$$

A is the weak–inversion slope factor, and $U_T = k_b T/q$ is the thermal voltage [18]. From Figure 3.3 it is

$$i_{DS_n} = i_{DS_p} + i_O, \tag{3.7}$$

where $i_O = u_O/R_L$ and $i_{DS_n}, i_{DS_p} \geq 0$. Let the minimum and maximum output voltage be $\pm u_O^{max}$, with $u_O^{max} > 0$. Due to i_{DS_n} being strictly increasing with u_{IN} and i_{DS_p} being strictly decreasing with u_{IN}, the minimum and maximum currents of the transistors appear in pairs, $\{i_{DS_n}^{min}, i_{DS_p}^{max}\}$, $\{i_{DS_n}^{max}, i_{DS_p}^{min}\}$; then, from (3.7)

$$\begin{aligned} i_{DS_n}^{min} &= i_{DS_p}^{max} - \frac{u_O^{max}}{R_L} \\ i_{DS_p}^{min} &= i_{DS_n}^{max} - \frac{u_O^{max}}{R_L}, \end{aligned} \tag{3.8}$$

where it may very well be $i_{DS_n}^{min} \neq i_{DS_p}^{min}$ and $i_{DS_n}^{max} \neq i_{DS_p}^{max}$.

For the maximum and minimum output voltage, equation (3.5) implies through (3.8) that

$$\begin{aligned} V_A &= \sqrt{\frac{i_{DS_n}^{min}}{\zeta_n}} + \sqrt{\frac{i_{DS_n}^{min} + \frac{u_O^{max}}{R_L}}{\zeta_p}} \\ V_A &= \sqrt{\frac{i_{DS_p}^{min} + \frac{u_O^{max}}{R_L}}{\zeta_n}} + \sqrt{\frac{i_{DS_p}^{min}}{\zeta_p}}. \end{aligned} \tag{3.9}$$

Since it is required that $i_{DS_n}^{min} > i_{lim}^{sat_n}$, $i_{DS_p}^{min} > i_{lim}^{sat_p}$, it must be selected

$$V_A > \max\left\{V_{A_1}, V_{A_2}\right\}, \tag{3.10}$$

where

$$\begin{aligned} V_{A_1} &= \sqrt{\frac{i_{lim}^{sat_n}}{\zeta_n}} + \sqrt{\frac{i_{lim}^{sat_n} + \frac{u_O^{max}}{R_L}}{\zeta_p}} \\ V_{A_2} &= \sqrt{\frac{i_{lim}^{sat_p} + \frac{u_O^{max}}{R_L}}{\zeta_n}} + \sqrt{\frac{i_{lim}^{sat_p}}{\zeta_p}}. \end{aligned} \tag{3.11}$$

Consider again the drain currents and the output voltage of the power stage in Figure 3.3,

$$\begin{aligned} i_{DS_n} &= \zeta_n \left(u_{IN} + V_{B_n} - u_O - V_{tn}\right)^2 \\ i_{DS_p} &= \zeta_p \left(u_O - u_{IN} + V_{B_p} - |V_{tp}|\right)^2 \\ u_O &= \left(i_{DS_n} - i_{DS_p}\right) R_L. \end{aligned} \tag{3.12}$$

For $u_{IN} = 0$ it is desired to be $u_O = 0$, which effectively means that $i_{DS_n} = i_{DS_p}$. This in combination with (3.12) implies that

$$\zeta_n \left(V_{B_n} - V_{tn}\right)^2 = \zeta_p \left(V_{B_p} - |V_{tp}|\right)^2. \tag{3.13}$$

As both MOSFETs operate in strong–inversion, it is $V_{B_n} - V_{tn} > 0$ and $V_{B_p} - |V_{tp}| > 0$, leading to

$$V_{B_p} = \sqrt{\frac{\zeta_n}{\zeta_p}} \left(V_{B_n} - V_{tn}\right) + |V_{tp}|. \tag{3.14}$$

From (3.4) and (3.14) it is $V_A = \left(1 + \sqrt{\frac{\zeta_n}{\zeta_p}}\right)\left(V_{B_n} - V_{tn}\right)$, and so the two required bias voltages for the push–pull power stage are

$$\begin{aligned} V_{B_n} &= \frac{V_A}{1 + \sqrt{\frac{\zeta_n}{\zeta_p}}} + V_{tn} \\ V_{B_p} &= \frac{V_A}{1 + \sqrt{\frac{\zeta_p}{\zeta_n}}} + |V_{tp}|. \end{aligned} \tag{3.15}$$

Power Stage Currents

Assuming that the DC bias voltage V_A has been selected according to equation (3.10), and that V_{B_n} and V_{B_p} are set following (3.15), the power stage currents i_{DS_n} and i_{DS_p}

are derived. It is important to know their expressions since they are the loads of the buck–converters in Figure 3.3.

Setting $w_n \triangleq V_{B_n} - V_{tn}$ and $w_p \triangleq -V_{B_p} + |V_{tp}|$ in equation (3.12) implies that

$$\begin{aligned} u_O = R_L \{ & \zeta_n \left[w_n^2 + u_{IN}^2 + u_O^2 + 2w_n u_{IN} - 2w_n u_O - 2u_{IN} u_O \right] \\ & - \zeta_p \left[w_p^2 + u_{IN}^2 + u_O^2 + 2w_p u_{IN} - 2w_p u_O - 2u_{IN} u_O \right] \Big\}. \end{aligned} \tag{3.16}$$

From (3.13) it is $\zeta_n w_n^2 - \zeta_p w_p^2 = 0$, and from (3.15) it is derived that $\zeta_n w_n - \zeta_p w_p = V_A \sqrt{\zeta_n \zeta_p}$. Thus, after some algebra, equation (3.16) gives

$$\begin{aligned} & \left(\zeta_n - \zeta_p\right) u_O^2 - \left[2V_A \sqrt{\zeta_n \zeta_p} + 2\left(\zeta_n - \zeta_p\right) u_{IN} + \frac{1}{R_L} \right] u_O \\ & \quad + \left(\zeta_n - \zeta_p\right) u_{IN}^2 + \left(2V_A \sqrt{\zeta_n \zeta_p} \right) u_{IN} = 0. \end{aligned} \tag{3.17}$$

Dividing this equality with $\sqrt{\zeta_n \zeta_p} > 0$ results in

$$\phi u_O^2 - \left(2V_A + 2\phi u_{IN} + \frac{1}{R_L \sqrt{\zeta_n \zeta_p}} \right) u_O + \phi u_{IN}^2 + 2V_A u_{IN} = 0, \tag{3.18}$$

where

$$\phi \triangleq \frac{\zeta_n - \zeta_p}{\sqrt{\zeta_n \zeta_p}}. \tag{3.19}$$

Two cases can be distinguished; $\zeta_n = \zeta_p$ and $\zeta_n \neq \zeta_p$. Assuming that $\zeta_n = \zeta_p = \zeta$ implies that $\phi = 0$ and (3.18) is transformed to

$$-\left(2V_A + \frac{1}{\zeta R_L} \right) u_O + 2V_A u_{IN} = 0, \tag{3.20}$$

leading to

$$u_O = k u_{IN}, \text{ with } k \triangleq \frac{2V_A \zeta R_L}{2V_A \zeta R_L + 1}. \tag{3.21}$$

The current–gain match of M_n and M_p results in a linear input–output relationship. Deviations between ζ_n and ζ_p will result in a nonlinear relationship, as $\phi \neq 0$ and the squared terms of u_{IN} and u_O in (3.18) will not be eliminated. This will in turn introduce distortion, which makes the sizing of the output devices for very close ζ_n and ζ_p values a desired and targeted design choice. Finally, for $\zeta_n = \zeta_p = \zeta$, equations (3.12), (3.15), and (3.21) result to the expressions of currents i_{DS_n} and i_{DS_p}

$$\begin{aligned} i_{DS_n} &= \left[\zeta \left(1 - k\right)^2 \right] u_{IN}^2 + \left[\zeta \left(1 - k\right) V_A \right] u_{IN} + \zeta \frac{V_A^2}{4} \\ i_{DS_p} &= \left[\zeta \left(1 - k\right)^2 \right] u_{IN}^2 - \left[\zeta \left(1 - k\right) V_A \right] u_{IN} + \zeta \frac{V_A^2}{4}. \end{aligned} \tag{3.22}$$

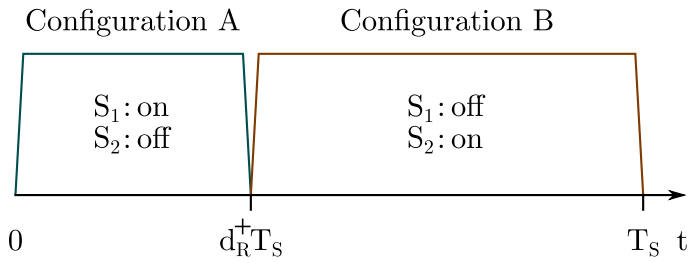

Figure 3.4: Positive–rail buck–converter configurations and timing.

3.3.2 Positive– & Negative–Rail Buck–Converters

Analysis now turns to the converters that generate the tracking supply rails of the Class–CTA power stage. For simplicity, focus will be primarily on the positive–rail buck–converter, as the circuit is symmetrical; only the final results for the negative–rail one will be presented.

State–Space Modeling

Within a switching period, T_S, the positive–rail buck–converter has two configurations, A and B, as depicted in Figure 3.4. During configuration A, when $t \in \left[0, d_R^+ T_S\right)$, switch S_1 is on and switch S_2 is off, with $d_R^+ \in [0,1]$ being the converter's duty cycle. For this state, the equations that describe the circuit are

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ V_R &= i_{L_1}\left(R_{ON_1} + R_L^{ESR}\right) + u_{L_1} + u_R^+ \\ 2V_R &= i_{L_1}\left(R_{ON_1} + R_L^{ESR}\right) + u_{L_1} + i_{C_1} R_C^{ESR} + u_{C_1}. \end{aligned} \tag{3.23}$$

For configuration B of the converter, during $t \in \left[d_R^+ T_S, T_S\right)$, S_1 is off and S_2 is on; then, it is

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ -V_R &= i_{L_1}\left(R_{ON_2} + R_L^{ESR}\right) + u_{L_1} + u_R^+ \\ 0 &= i_{L_1}\left(R_{ON_2} + R_L^{ESR}\right) + u_{L_1} + i_{C_1} R_C^{ESR} + u_{C_1}. \end{aligned} \tag{3.24}$$

During both time intervals, the converter's output current is that of the NMOS transistor M_n in the Class–A power stage

$$i_R^+ = i_{DS_n}. \tag{3.25}$$

Given that the current relationship of i_R^+ and the desired tracking behavior of u_R^+ are known, one could attempt to solve the state–space equations (3.23) and (3.24) analytically, and acquire the exact solution over a switching period by means of con-

tinuity at the time of the configurations' switching. However, the design philosophy of the proposed architecture allows for a simpler analysis approach; given that the switching frequency, $f_S = 1/T_S$, is much higher than: (a) the maximum input signal frequency, (b) the natural frequencies of the converter, and (c) the frequencies of variations in the converter's inputs, it is concluded that time–averaging of (3.23) and (3.24) can be employed [19] instead of the more complicated exact solution. Thus, over a switching period, the time–averaging approach results in

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ \left(2d_R^+ - 1\right) V_R &= i_{L_1}\left[d_R^+ R_{ON_1} + \left(1 - d_R^+\right) R_{ON_2} + R_L^{ESR}\right] + u_{L_1} + u_R^+ \\ u_{C_1} + i_{C_1} R_C^{ESR} &= u_R^+ + V_R, \end{aligned} \tag{3.26}$$

where the third equation results from subtracting the second one from the third in (3.23) and (3.24), and time–averaging.

Defining $x^+ = \left[u_{C_1} \;\; i_{L_1}\right]^\top$, $y^+ = u_R^+ + V_R$, and replacing i_{C_1} and u_R^+ of the first and third equations in (3.26) into the second one, it is derived that

$$\begin{aligned} \dot{x}^+ &= \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{\left(R_L^{ESR} + R_C^{ESR} + R_{ON_2}\right)}{L} \end{bmatrix} x^+ + \begin{bmatrix} 0 \\ \frac{2V_R}{L} \end{bmatrix} d_R^+ + \begin{bmatrix} -\frac{1}{C} \\ \frac{R_C^{ESR}}{L} \end{bmatrix} i_R^+ + \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_2} - R_{ON_1}}{L} \end{bmatrix} x^+ d_R^+ \\ y^+ &= \left[1 \;\; R_C^{ESR}\right] x^+ + \left[-R_C^{ESR}\right] i_R^+. \end{aligned} \tag{3.27}$$

Equations in (3.27) form the (time–averaged) state–space representation of the positive–rail buck–converter when considering the duty cycle d_R^+ as the system's input and y^+ as its output. Similar analysis and reasoning leads to the corresponding state–space equation for the case of the negative–rail buck–converter

$$\begin{aligned} \dot{x}^- &= \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{\left(R_L^{ESR} + R_C^{ESR} + R_{ON_4}\right)}{L} \end{bmatrix} x^- + \begin{bmatrix} 0 \\ \frac{2V_R}{L} \end{bmatrix} d_R^- + \begin{bmatrix} -\frac{1}{C} \\ \frac{R_C^{ESR}}{L} \end{bmatrix} i_R^- + \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_4} - R_{ON_3}}{L} \end{bmatrix} x^- d_R^- \\ y^- &= \left[-1 \;\; -R_C^{ESR}\right] x^- + \left[R_C^{ESR}\right] i_R^-, \end{aligned} \tag{3.28}$$

where $x^- = \left[u_{C_2} \;\; i_{L_2}\right]^\top$ and $y^- = u_R^- - V_R$.

The term involving multiplication of the state vector and the input signal (duty cycle) makes systems (3.27) and (3.28) bilinear [20], and therefore their analysis and feedback design more challenging. However, the bilinear terms $x^+ d_R^+$ and $x^- d_R^-$ can be eliminated by sizing the switches such that $R_{ON_1} = R_{ON_2} = R_{ON_3} = R_{ON_4} = R_{ON}$; this is a convenient design choice. It is desirable to have similar voltage drop on the on–resistance of the converter's switches during its two operation states, and also to opt for similar behavior between the positive– and negative–rail buck–converters, as this favors the use of the same feedback scheme and the same L and C values.

Selection of Converters' L & C Values

Based on the assumption of equal R_{ON} values of the switches that led to the elimination of the bilinear term in (3.27) and (3.28), one can proceed with the initial selection of the inductor and capacitor values for the two buck–converters.

At equilibrium[1], $\dot{x}^+ = \dot{x}^- = 0$, and supply rails u_R^+ and u_R^- have reached their targeted values; thus, $u_R^+ = ku_{IN} + u_M$ and $u_R^- = ku_{IN} - u_M$ (recall that $u_O = ku_{IN}$). Replacing the above in the state–space equations (3.27) and (3.28), the equilibrium values of the converters' duty cycles are derived

$$\begin{aligned} d^+_{R_{|eq.}} &= \frac{1}{2V_R}\left[V_R + (ku_{IN} + u_M) + \left(R_L^{ESR} + R_{ON}\right) i_R^+\right] \\ d^-_{R_{|eq.}} &= \frac{1}{2V_R}\left[V_R - (ku_{IN} - u_M) + \left(R_L^{ESR} + R_{ON}\right) i_R^-\right]. \end{aligned} \tag{3.29}$$

Assuming small voltage ripple at the outputs of the two buck–converters, over a switching period the inductor current can be approximated by the superposition of a constant current component and a current ripple, $\tilde{i}_L$. The ripple can be approximated by a triangle waveform with zero mean value and maximum–minimum values of $\pm\Delta i_L$ [19], as depicted in Figure 3.5. In the positive–rail buck–converter, during time interval $\left[0, d^+_{R_{|eq.}} T_S\right)$ the derivative of i_{L_1}, $\dot{i}_{L_1}$, can be approximated by

$$\dot{i}_{L_1} = \frac{2\Delta i_{L_1}}{d^+_{R_{|eq.}} T_S}. \tag{3.30}$$

Within $\left[0, d^+_{R_{|eq.}} T_S\right)$, equilibrium condition $\dot{x}^+ = 0$ applied to (3.27) results in $i_{L_1} = i_R^+ + \tilde{i}_L$, which is simplified to $i_{L_1} \simeq i_R^+$ by assuming the desirable condition that $|\Delta i_{L_1}| \ll i_R^+$. Combining this with (3.30) and (3.23) (where $u_{L_1} = L\dot{i}_{L_1}$) gives

$$L\frac{2\Delta i_{L_1}}{d^+_{R_{|eq.}} T_S} = V_R - \left[ku_{IN} + u_M + \left(R_L^{ESR} + R_{ON}\right) i_R^+\right]. \tag{3.31}$$

To keep the current ripple below Δi_L^{max}, the inductor must be larger than the following bound

$$L > \frac{T_S}{4V_R\Delta i_L^{max}}\left\{V_R^2 - \left[ku_{IN} + u_M + \left(R_L^{ESR} + R_{ON}\right) i_R^+\right]^2\right\}. \tag{3.32}$$

Exactly the same result applies to the negative–rail buck–converter.

To keep voltage ripple small, capacitor C should be sufficiently large. A relation-

[1] According to the assumptions in subsection 3.3.2, the two converters must be sufficiently fast so that they always remain close to equilibrium independently of the power stage's input signal.

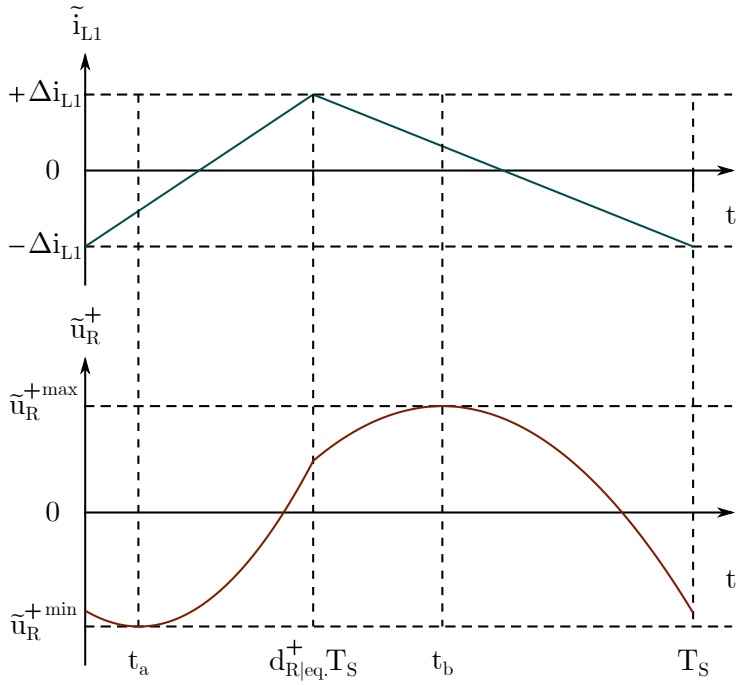

Figure 3.5: Positive–rail buck–converter's inductor current ripple and output voltage ripple waveforms.

ship between the voltage ripple and C is obtained by assuming that inductor's current ripple flows only through R_C^{ESR} and C, i.e. $\tilde{i}_{C_1} = \tilde{i}_{L_1}$, which is typically the case for a properly designed converter. For triangle–shaped inductor ripple current, in the case of the positive–rail buck–converter and for $t \in \left[0, d^+_{R_{|eq.}} T_S\right)$ it is

$$\begin{aligned} \tilde{i}_{C_1} = \tilde{i}_{L_1} &= \Delta i_{L_1} \left(\frac{2t}{d^+_{R_{|eq.}} T_S} - 1 \right) \\ \tilde{u}_{R_C^{ESR}} &= \tilde{i}_{C_1} R_C^{ESR} \\ \tilde{u}_{C_1} &= \frac{1}{C} \int_0^t \tilde{i}_{C_1}(\tau) d\tau = \frac{\Delta i_{L_1}}{C} \left(\frac{t^2}{d^+_{R_{|eq.}} T_S} - t \right). \end{aligned} \tag{3.33}$$

Similarly, for $t \in \left[d^+_{R_{|eq.}} T_S, T_S\right)$ it is

$$\begin{aligned} \tilde{i}_{C_1} = \tilde{i}_{L_1} &= \Delta i_{L_1} \left[\frac{1 + d^+_{R_{|eq.}}}{1 - d^+_{R_{|eq.}}} - \frac{2t}{\left(1 - d^+_{R_{|eq.}}\right) T_S} \right] \\ \tilde{u}_{R_C^{ESR}} &= \tilde{i}_{C_1} R_C^{ESR} \\ \tilde{u}_{C_1} &= \frac{1}{C} \int_{d^+_{R_{|eq.}} T_S}^t \tilde{i}_{C_1}(\tau) d\tau = \frac{\Delta i_{L_1}}{C} \left[\frac{\left(1 + d^+_{R_{|eq.}}\right) t - d^+_{R_{|eq.}} T_S}{1 - d^+_{R_{|eq.}}} - \frac{t^2}{\left(1 - d^+_{R_{|eq.}}\right) T_S} \right]. \end{aligned} \tag{3.34}$$

The total output voltage ripple is equal to $\tilde{u}_R^+ = \tilde{u}_{R_C^{ESR}} + \tilde{u}_{C_1}$ (Figure 3.5), and achieves its minimum and maximum values at $t_a = 0.5 d^+_{R_{|eq.}} T_S - C R_C^{ESR}$ and $t_b = 0.5(1 + d^+_{R_{|eq.}}) T_S - C R_C^{ESR}$, respectively, with

$$\begin{aligned} \tilde{u}_R^{+min} &= -\left(\frac{\Delta i_{L_1} R_C^{ESR\,2}}{d^+_{R_{|eq.}} T_S} C + \frac{\Delta i_{L_1} d^+_{R_{|eq.}} T_S}{4} \frac{1}{C} \right) \\ \tilde{u}_R^{+max} &= \frac{\Delta i_{L_1} R_C^{ESR\,2}}{\left(1 - d^+_{R_{|eq.}}\right) T_S} C + \frac{\Delta i_{L_1} \left(1 - d^+_{R_{|eq.}}\right) T_S}{4} \frac{1}{C}. \end{aligned} \tag{3.35}$$

Note that the expressions of the minimum and the maximum values of the ripple in (3.35) are valid when $t_a > 0$ and $t_b > d^+_{R_{|eq.}} T_S$, respectively; otherwise $\tilde{u}_R^{+min}$ and $\tilde{u}_R^{+max}$ are only lower and upper bounds of the minimum and the maximum values, respectively.

Thus, for a targeted maximum ripple value of Δu_R^{max}, it is recommended to select the capacitor's value C between the following two bounds derived from (3.35)

$$C_{a,b} = \frac{\left(1 - d^+_{R_{|eq.}}\right) T_S}{2 \Delta i_L^{max} R_C^{ESR\,2}} \times \left[\Delta u_R^{max} \pm \sqrt{\Delta u_R^{max\,2} - \left(\Delta i_L^{max} R_C^{ESR}\right)^2} \right]. \tag{3.36}$$

Equation (3.36) also implies a lower limit on the desired voltage ripple; it should be $\Delta u_R^{max} \geq \Delta i_L^{max} R_C^{ESR}$, which is of course expected. The same results can be obtained for the negative–rail buck–converter.

Even though one would want both ripples to be very small in value to improve the proposed power stage's linearity, an upper bound of the LC product must also be estimated, since very large values will pose difficulties in tracking input signals with high rise or fall rates (but always within a bandwidth low enough with respect to the converters' switching frequency), and thus, performance degradation. To this end, the following simplified case is considered.

Assume that at $t = 0$ the tracking rail voltage $u_R^+(0)$ is close to its maximum allowed value ($\simeq V_R$) and that its derivative is equal to 0, i.e., $\dot{u}_R^+(0) = 0$. Moreover, to make the problem tractable, lets assume that $R_{ON} = R_L^{ESR} = R_C^{ESR} = 0$. At $t = 0^+$, output voltage u_O starts to rise with its maximum rate, $\rho > 0$, forcing the converter to configuration A (Figure 3.4). Current i_R^+ is also close to its maximum value, $i_R^+ = I_R^+$, and for simplicity it is assumed almost constant for a brief period of time. Then, it is

$$\begin{aligned} V_R - u_R^+ &= L \dot{i}_{L_1} \\ i_{L_1} &= C \dot{u}_R^+ + I_R^+, \end{aligned} \tag{3.37}$$

leading to

$$V_R = u_R^+ + LC\ddot{u}_R^+. \tag{3.38}$$

Differential equation (3.38) has the solution $u_R^+ = h_s \sin(\psi t) + h_c \cos(\psi t) + V_R$, where $\psi \triangleq 1/\sqrt{LC}$. With the initial conditions of $u_R^+(0)$ and $\dot{u}_R^+(0) = 0$, one derives

$$u_R^+ = V_R - \left[V_R - u_R^+(0)\right] \cos(\psi t). \tag{3.39}$$

From (3.39) it is seen that u_R^+ is a convex function of time within a certain time period from $t = 0$ and also $\dot{u}_R^+(0) = 0$. Assuming a large ψ value, and so a fast tracking response due to fast increase of $\dot{u}_R^+$, along with a relatively slow, approximate linear increase of u_O with rate ρ, implies that the voltage margin $u_R^+ - u_O$ attends its minimum value when the slope of u_R^+ equals ρ. Based on the above assumptions, this equation of slopes happens for small t, motivating the approximation $\psi t \ll 1$, giving $\sin(\psi t) \simeq \psi t$. Thus,

$$\dot{u}_R^+ = \psi \left[V_R - u_R^+(0)\right] \sin(\psi t) \simeq \psi^2 \left[V_R - u_R^+(0)\right] t. \tag{3.40}$$

The slope of u_R^+ becomes equal to ρ at approximate time t_ρ

$$\psi^2 \left[V_R - u_R^+(0)\right] t_\rho = \rho \Rightarrow t_\rho = \frac{\rho}{\psi^2 \left[V_R - u_R^+(0)\right]}. \tag{3.41}$$

Therefore, the minimum margin voltage is

$$\begin{aligned} u_M^{min} &= u_R^+(t_\rho) - u_O(t_\rho) \\ &= V_R - \left[V_R - u_R^+(0)\right] \cos(\psi t_\rho) - [u_O(0) + \rho t_\rho] \\ &\simeq V_R - \left[V_R - u_R^+(0)\right] \left[1 - \frac{\psi^2 t_\rho^2}{2}\right] - u_O(0) - \rho t_\rho \\ &\simeq \underbrace{u_R^+(0) - u_O(0)}_{u_M} - \frac{\rho^2}{2\psi^2 \left[V_R - u_R^+(0)\right]}. \end{aligned} \tag{3.42}$$

Thus, for u_M^{min} being larger than a minimum limit, $u_M^{min,lim}$, (3.42) leads to

$$\psi^2 > \frac{\rho^2}{2\left[V_R - u_R^+(0)\right]\left(u_M - u_M^{min,lim}\right)}, \tag{3.43}$$

which results in the upper bound of the LC product

$$LC < \frac{2\left[V_R - u_R^+(0)\right]\left(u_M - u_M^{min,lim}\right)}{\rho^2}. \tag{3.44}$$

3.3.3 Output–Tracking Rails Control

Following the analysis of the buck–converters, one continues with the design of the feedback control scheme for the supply rails to track the output plus/minus the voltage margin, u_M. Given the previous simplifying assumption that all switches have the same on–resistance, both state–space systems of the two converters have the linear, time–invariant (LTI) form of[2]

$$\begin{aligned} \dot{x} &= Ax + Bd_R + Di_R \\ y &= Cx + Ei_R \end{aligned} \tag{3.45}$$

where the state vector is $x = [u_C \;\; i_L]^\top$, and matrices A, B, C, D, and E are defined in the obvious way according to equations (3.27) and (3.28).

Output Feedback Control Scheme

A common approach is to employ static output feedback with integral action [21], i.e.,

$$\begin{aligned} \dot{\sigma} &= e = y - r \\ d_R &= f_{sat}\left(k_I\sigma + k_P e\right) \in [0,1], \end{aligned} \tag{3.46}$$

with $k_I, k_P \in \mathbb{R}^{1\times 1}$ and $f_{sat}(\cdot)$ be a saturation function capturing the circuit–level behavior of duty cycle d_R; i.e., $f_{sat}(\eta) = \max\left[0, \min\left(\eta, 1\right)\right]$ implying that $d_R = k_I\sigma + k_P e$ under normal operating conditions with $k_I\sigma + k_P e \in (0,1)$, resulting in the classic PI controller, and, saturating to 0 or 1 when $k_I\sigma + k_P e$ exceeds normal values.

For the positive– and negative–rail buck–converters it is selected $r^+ = u_O + u_M + V_R$ and $r^- = u_O - u_M - V_R$, respectively. Then, the closed–loop system is described by the following equations

$$\begin{aligned} \begin{bmatrix} \dot{x} \\ \dot{\sigma} \end{bmatrix} &= \begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix} \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + \begin{bmatrix} -k_P B & D + k_P BE \\ -1 & E \end{bmatrix} \cdot \begin{bmatrix} r \\ i_R \end{bmatrix} \\ \begin{bmatrix} y \end{bmatrix} &= \begin{bmatrix} C & 0 \end{bmatrix} \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + \begin{bmatrix} 0 & E \end{bmatrix} \cdot \begin{bmatrix} r \\ i_R \end{bmatrix}. \end{aligned} \tag{3.47}$$

Scalar gain parameters k_I, k_P need to be selected such that the matrix

$$\begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix} \in \mathbb{R}^{3\times 3} \tag{3.48}$$

[2]Strictly speaking, (3.45) should be written as $\dot{x}^\pm = A^\pm x^\pm + B^\pm d_R^\pm + D^\pm i_R^\pm$, $y^\pm = C^\pm x^\pm + E^\pm i_R^\pm$. However, the "$\pm$" superscript is dropped for simplicity, keeping in mind that the matrix parameters have different values for the positive– and the negative–rail buck–converters.

is Hurwitz, while more elaborate placement of its eigenvalues can be done to optimize the controller's performance with respect to transient response and static error. If tracking proves insufficient, a complete PID controller should be considered. On the other hand, if static error is tolerable, the integral part of the control scheme can be omitted.

Control Scheme Robustness

The proposed control scheme (3.46)–(3.47) was derived based on the simplifying assumption that $R_{ON_1} = R_{ON_2} = R_{ON_3} = R_{ON_4} = R_{ON}$. A plausible question is whether the controller is acceptable should this condition be violated, where the simplified LTI state–space systems are replaced by the original bilinear ones in (3.27) and (3.28). From Figure 3.3 it is evident that switches S_1 and S_4 will be realized by PMOS devices, with NMOS ones being used for S_2 and S_3; as such, a mismatch in their on–resistor values due to them being realized by different transistor types is to some extent expected.

Here, the bilinear system (3.27) is investigated in terms of stability; similar analysis holds for system (3.28). Dropping superscript "+" for simplicity, equation (3.27) is rewritten as

$$\begin{aligned} \dot{x} &= (A + A_\delta d_R)\, x + B d_R + D i_R \\ y &= Cx + E i_R, \end{aligned} \tag{3.49}$$

where

$$A_\delta = \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_2} - R_{ON_1}}{L} \end{bmatrix}. \tag{3.50}$$

Note that the LTI system (3.45) results from (3.49) when the bilinear coefficient A_δ is eliminated.

By adopting the PI controller scheme which was discussed in the previous subsection, the following dynamics for the closed–loop system is obtained

$$\begin{aligned} \begin{bmatrix} \dot{x} \\ \dot{\sigma} \end{bmatrix} &= \begin{bmatrix} (A + A_\delta d_R) + k_P BC & k_I B \\ C & 0 \end{bmatrix} \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + \begin{bmatrix} -k_P B & D + k_P BE \\ -1 & E \end{bmatrix} \cdot \begin{bmatrix} r \\ i_R \end{bmatrix} \\ [y] &= [C \;\; 0] \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + [0 \;\; E] \cdot \begin{bmatrix} r \\ i_R \end{bmatrix}. \end{aligned} \tag{3.51}$$

Equation (3.51) is rewritten as

$$\begin{aligned} \dot{z} &= \mathcal{A}(d_R) z + \mathcal{B} u \\ y &= \mathcal{C} z + \mathcal{D} u, \end{aligned} \tag{3.52}$$

with $z = [x \quad \sigma]^\top$ and $u = [r \quad i_R]^\top$ being the augmented state and input vectors, respectively. Matrices $\mathcal{A}(d_R), \mathcal{B}, \mathcal{C}$, and $\mathcal{D}$ are defined accordingly.

Matrix function $\mathcal{A}(d_R)$ is affine in the control signal d_R, i.e. $\mathcal{A}(d_R) = \mathcal{A}_o + \mathcal{A}_\delta d_R$ with

$$\mathcal{A}_o = \begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix}, \quad \mathcal{A}_\delta = \begin{bmatrix} A_\delta & 0 \\ 0 & 0 \end{bmatrix}. \tag{3.53}$$

As imposed by (3.46), the time–varying duty cycle d_R belongs to the convex set $[0, 1]$.

Proposition 1 *If there exists a positive–definite symmetric matrix $P \in \mathbb{R}^{3\times3}$ such that*

$$\mathcal{A}^\top(\delta)P + P\mathcal{A}(\delta) < 0, \tag{3.54}$$

for $\delta = 0$ and $\delta = 1$, then, (3.54) is also valid for every value of δ in between, i.e. $\delta \in [0, 1]$. Moreover, due to the continuity of function $\mathcal{A}(\cdot)$ and that of the eigenvalues, as well as the compactness of $[0, 1]$, there exist constant $\gamma > 0$ such that

$$\mathcal{A}^\top(\delta)P + P\mathcal{A}(\delta) \leq -\gamma I \tag{3.55}$$

for every $\delta \in [0, 1]$, with I being the identity matrix.

Proof: This follows from the fact that $\mathcal{A}(\delta)$ is affine in δ and $[0, 1]$ is convex [22]. ■

Proposition 2 *Assuming there exist $P \succ 0$ such that (3.54) is satisfied, then the system (3.52) is BIBO (Bounded–Input u, Bounded–Output y) stable.*

Proof: Consider the Lyapunov Function V of the form

$$V = z^\top P z, \tag{3.56}$$

where z is the augmented state and P is the positive–definite matrix satisfying (3.54) and (3.55). Then, it holds that

$$\lambda_{\min}(P)\|z\|^2 \leq V \leq \lambda_{\max}(P)\|z\|^2. \tag{3.57}$$

Given a control input $d_R = d_R(t) \in [0, 1]$, the time–derivative of V is

$$\begin{aligned} \dot{V} &= (\mathcal{A}(d_R)z + \mathcal{B}u)^\top Pz + z^\top P(\mathcal{A}(d_R)z + \mathcal{B}u) \\ &= z^\top \left(\mathcal{A}^\top(d_R)P + P\mathcal{A}(d_R)\right) z + 2z^\top P\mathcal{B}u \\ &\leq -\gamma\|z\|^2 + 2\|z\|\|P\mathcal{B}\|\|u\| \\ &\leq -\gamma\|z\|^2 + 2\|z\|\|P\mathcal{B}\|M, \end{aligned} \tag{3.58}$$

where M is an upper bound of $\|u\|$ set by the circuit. The "quadratic" term $-\gamma\|z\|^2$

will dominate the "linear" term $2\|z\|\|P\mathcal{B}\|M$ for large values of $\|z\|$ and so

$$\dot{V} \leq 0 \text{ for } \|z\| \geq \frac{2\|P\mathcal{B}\|M}{\gamma}, \tag{3.59}$$

which implies that for large values of $\|z\|$, $\dot{V}$ is negative which yields that V stays finite. Following that, it can be seen from (3.57) that $\|z\|$ has to stay finite and BIBO stability is shown. ■

Due to the affine $\mathcal{A}(\cdot)$, ensuring the stability of the bilinear system (3.52) requires the verification of only two Linear Matrix Inequalities (LMIs), corresponding to the marginal values of d_R (this is encountered as Common Quadratic Lyapunov Function in the literature [22, 23]).

The set of LMIs described in (3.54) can be solved using any Semi–Definite Programming Suite (e.g. SDPT3 [24]) in standard computational platforms such as Python (e.g. cvxpy [25]), MATLAB (e.g. Yalmip [26]), etc. By checking condition (3.54), it can be ensured that the bilinear system is BIBO stable even for large mismatches in the on–resistances of the converters' switches that can result from their different transistor type characteristics.

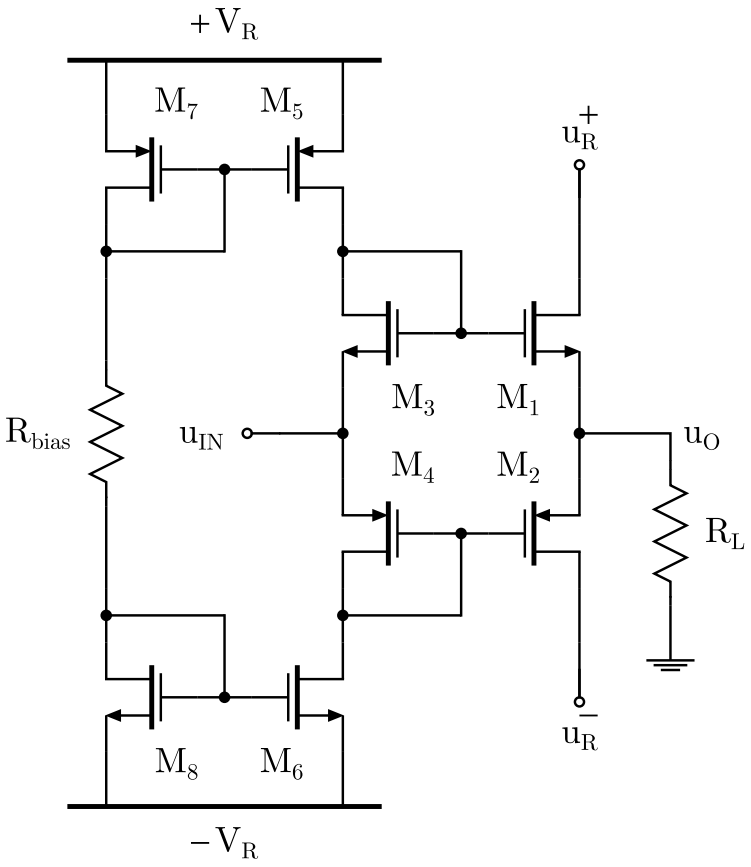

Figure 3.6: Class–CTA power stage.

3.4 Proof–of–Concept Implementation

To validate the concept of the proposed architecture and demonstrate its performance potential, a Class–CTA power stage design example is given. For the purposes of this work, this proof–of–concept design example is implemented and simulated at schematic–level in Cadence Spectre in ON Semi CMOS 0.35 µm technology, while its behavior is compared in terms of output spectrum (linearity) and efficiency versus the classic push–pull Class–A biasing scheme. Sizing of the involved elements was done using the theoretical analysis presented in the previous sections.

3.4.1 Circuit Implementation

The push–pull Class–A power stage core of the implemented Class–CTA with its biasing network is given in Figure 3.6. The output devices are biased with a quiescent current of 385 mA and drive a classic 8 Ω load encountered in audio applications, while supply rails, $\pm V_R$, are set to ±6 V.

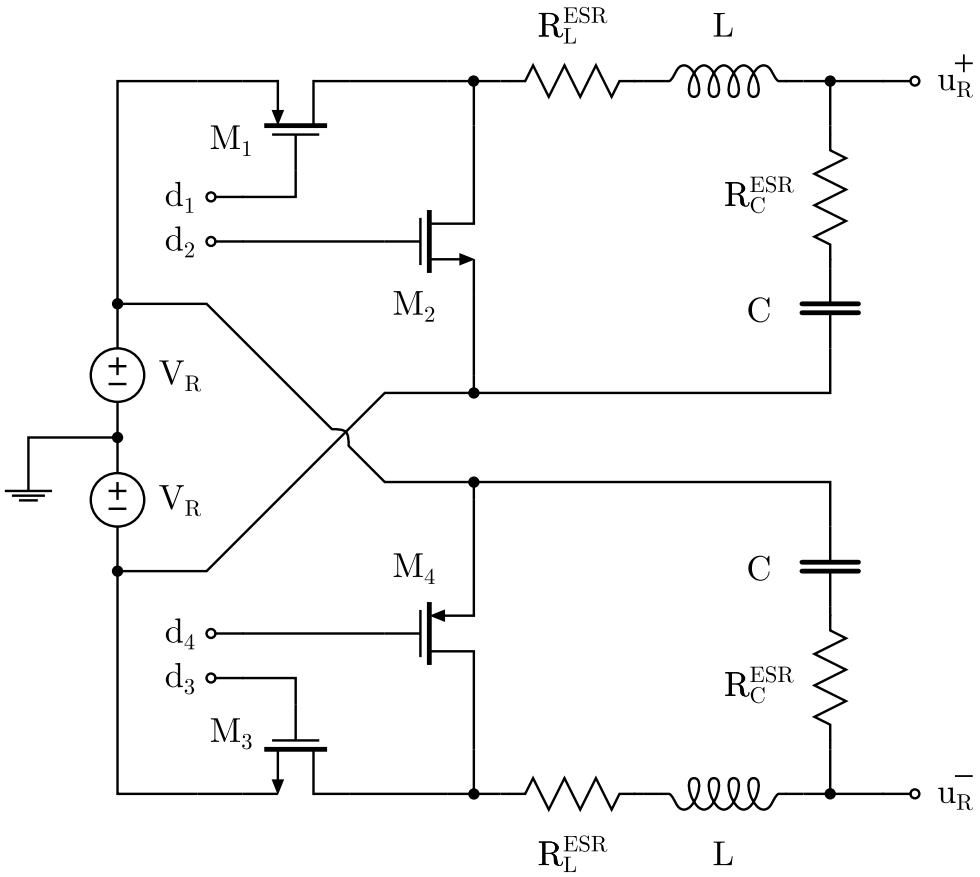

Figure 3.7: Positive– and negative–rail buck–converters of Class–CTA.

The two buck–converters in Figure 3.7 are equipped with $L = 33\,\mu H$ and

$C = 470\,\text{nF}$, while $R_L^{ESR} = 50\,\text{m}\Omega$ and $R_C^{ESR} = 0.5\,\Omega$. The switching frequency is set to 5 MHz, complying with the assumption of Subsection 3.3.2 that enabled the time–averaging of the state–space model; the maximum signal frequency for audio is 20 kHz. The switches feature an average on–resistance of 353 mΩ to minimize voltage drop, and their control signals, d_1, d_2, d_3, and d_4, are provided by two non–overlapping clock generators like the one depicted in Figure 3.8.

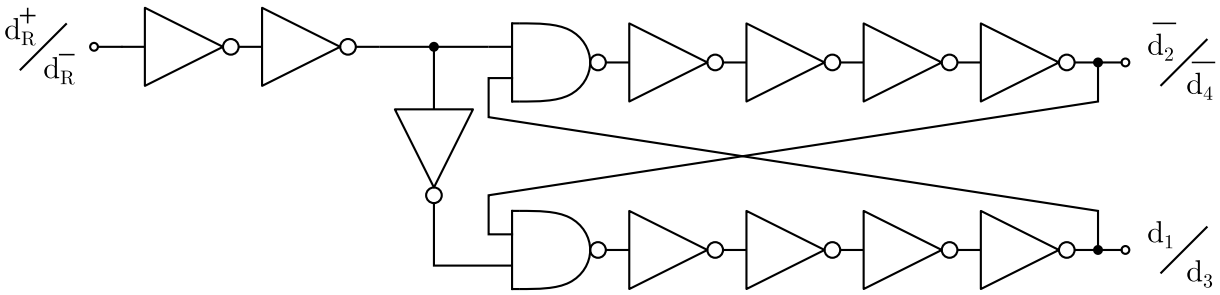

Figure 3.8: Non–overlapping clock generator.

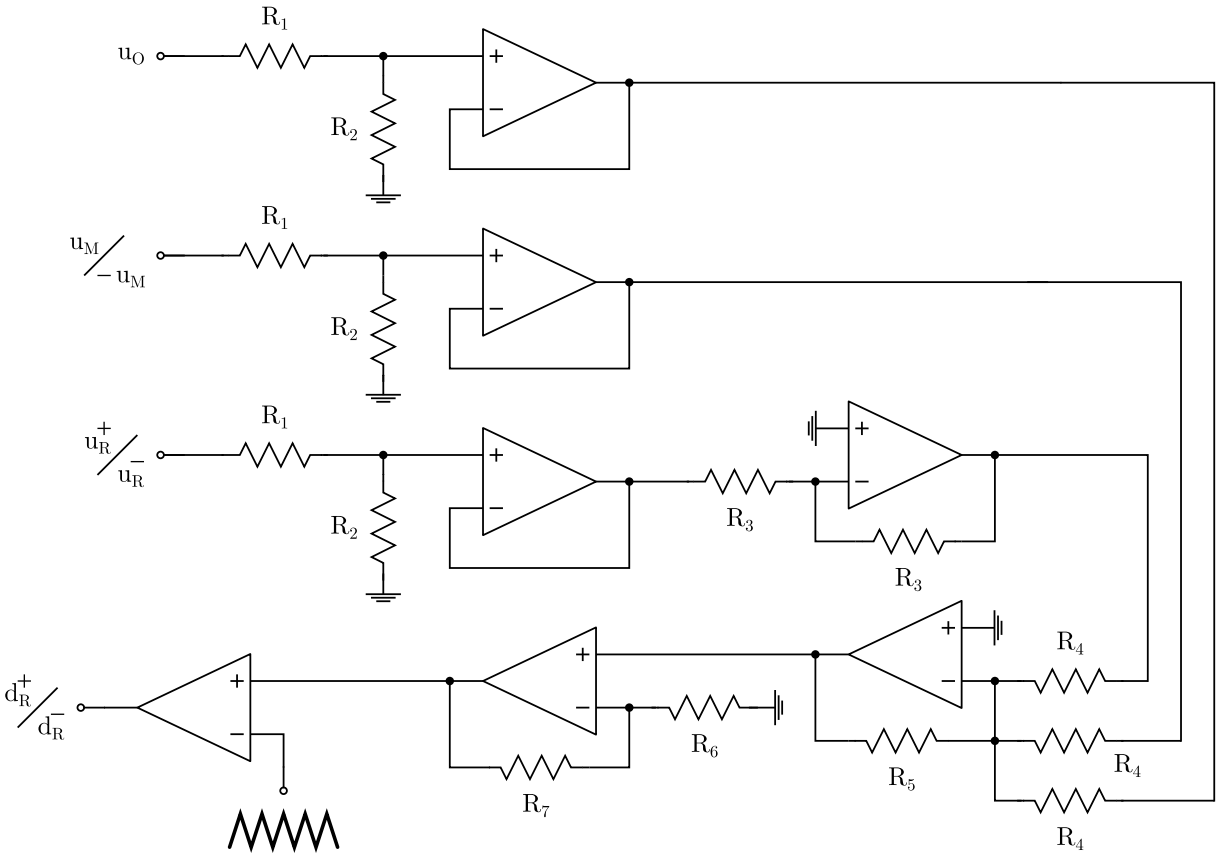

Figure 3.9: PWM control block.

Tracking margin voltage, u_M, is selected to be 1 V, giving about a few hundred mV of u_{DS} saturation margin for the output devices and ensuring that both of them

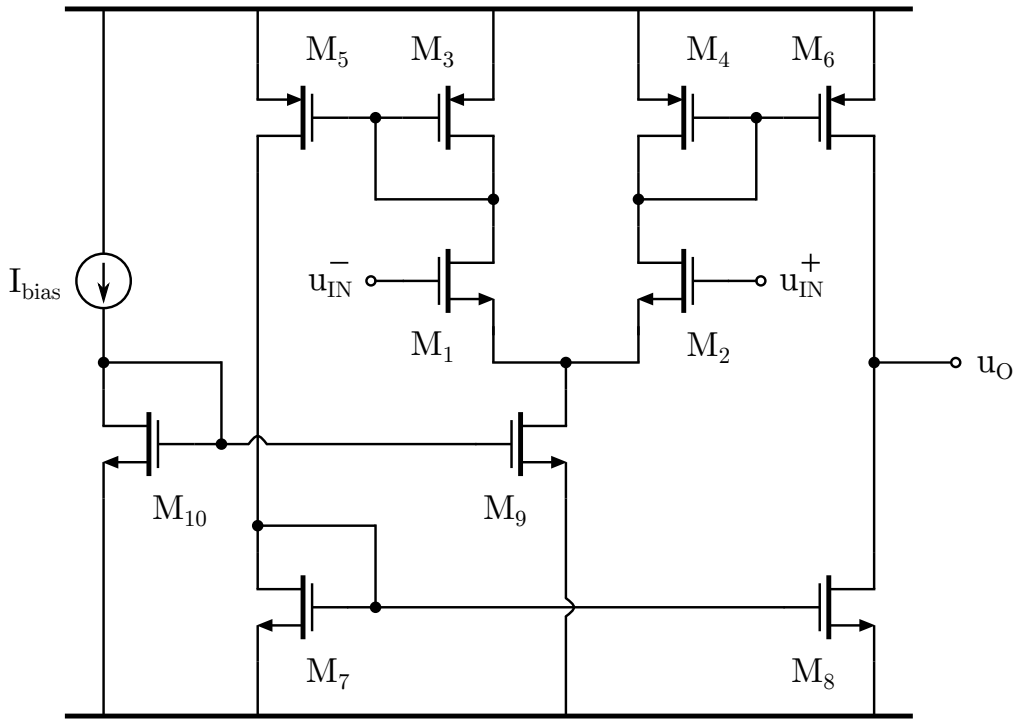

Figure 3.10: Current–mirror operational amplifier used in the PWM control block.

are always in strong–inversion. For this proof–of–concept implementation, a simple proportional–only feedback control scheme is used, implemented by the network in Figure 3.9. With a selected gain of $k_P = 40$, the maximum observed error in the supply rails' tracking is minimal, without impact on Class–CTA's performance. For the amplifiers and the comparator of the PWM control block, the current–mirror operational amplifier of Figure 3.10 is used.

3.4.2 Simulation Results

Figure 3.11 presents the transient response of the power stage's output, positive– , and negative–rail, with a 1 kHz, 1 V peak input after settling has been achieved. The corresponding tracking errors are given in Figure 3.12, showing a maximum error value of 18.2 mV and 10.1 mV for the positive– and negative–rail, respectively. The error, $\Delta u_R^{\pm}$, is defined as the actual rail value minus the ideal target of $u_O \pm u_M$; minimum error values are -2.7 mV for the positive–rail and -1.6 mV for the negative–rail. Spectra of the three signals by means of Discrete Fourier Transform (DFT) are available in Figure 3.13; the 5 MHz spur is at a -48.8 dBV level for the positive–rail, at -49.5 dBV for the negative–rail, and at -67.9 dBV for the output of the power stage, where no filtering or feedback is applied. Due to the switching frequency being two orders of magnitude larger than the maximum input signal frequency, the switching spur can be easily suppressed further by the inclusion of an

appropriate load capacitance without affecting performance.

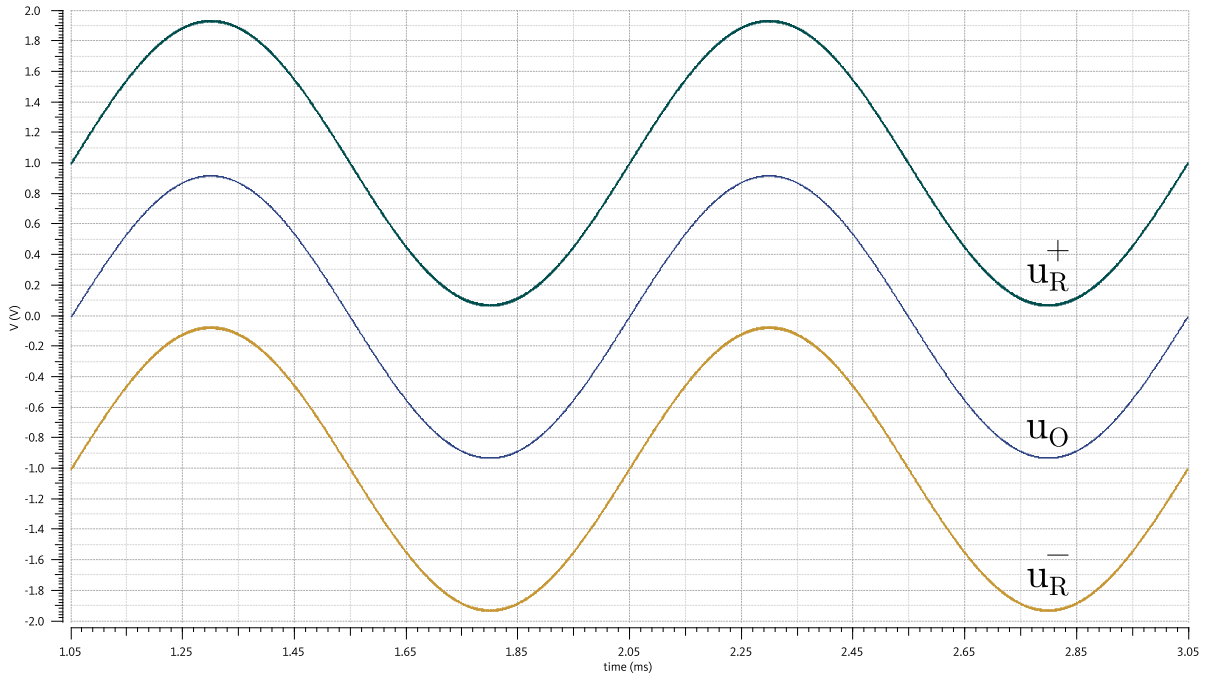

Figure 3.11: Class–CTA rails and output for an 1 kHz, 1 V input.

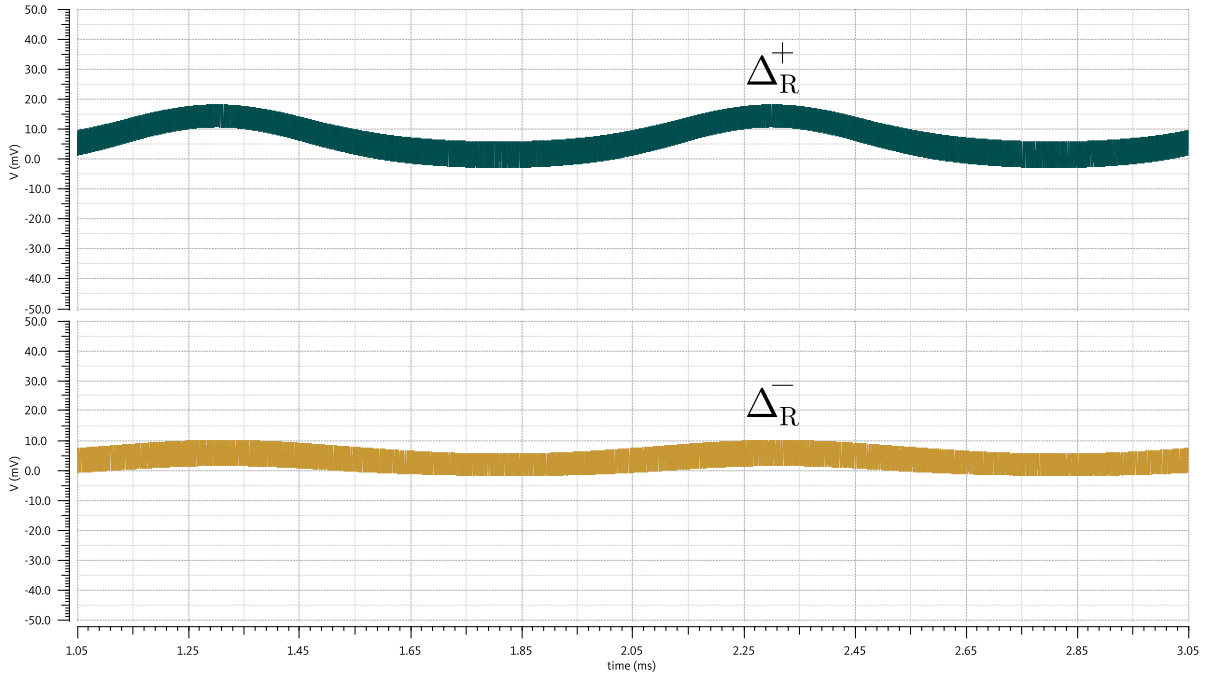

Figure 3.12: Class–CTA rails' error for an 1 kHz, 1 V input.

Transient performance for a 20 kHz, 3 V peak input signal is shown next in Figure 3.14. Tracking of the output signal by the buck–converters is again very good, with

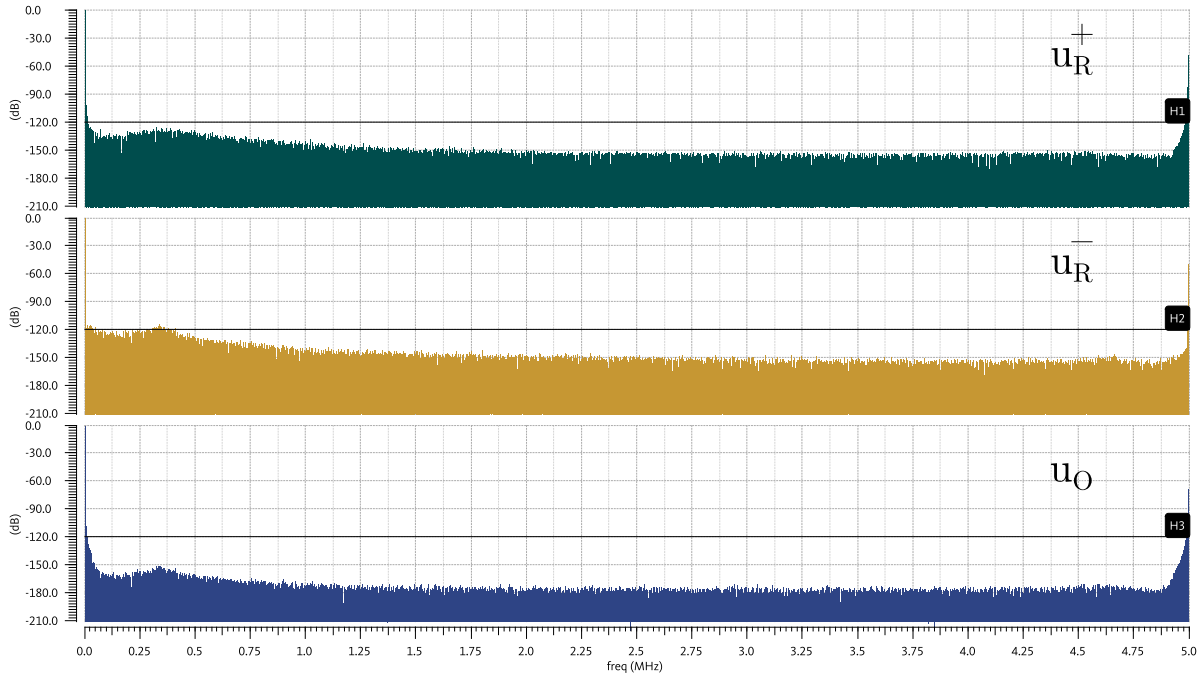

Figure 3.13: Class–CTA rails and output DFTs for an 1 kHz, 1 V input.

46.6 mV of maximum error for the positive–rail, and 28.3 mV for the negative–rail being observed in Figure 3.15; minimum error values are −20.0 mV and −18.5 mV, respectively. The strength of 5 MHz spur is similar to that in the previous case;

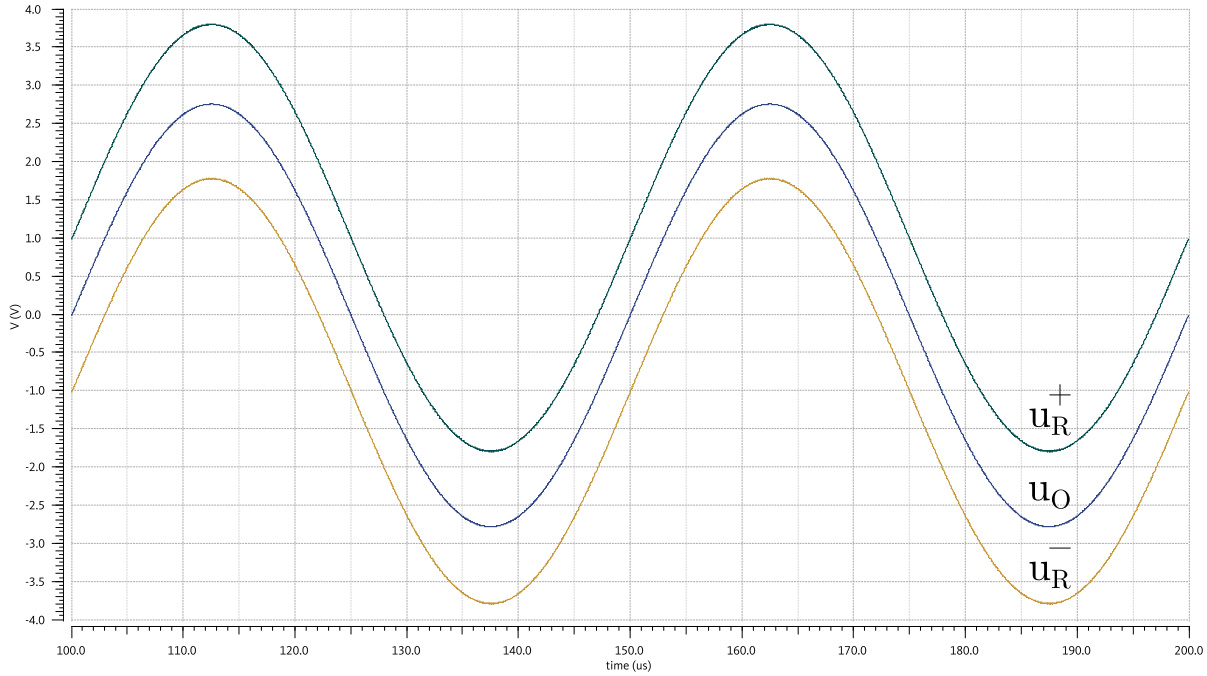

Figure 3.14: Class–CTA rails and output for a 20 kHz, 3 V input.

Figure 3.16 indicates levels of $-50.1\,\mathrm{dBV}$, $-49.9\,\mathrm{dBV}$, $-69.0\,\mathrm{dBV}$ for the positive–, negative–rail, and output, respectively.

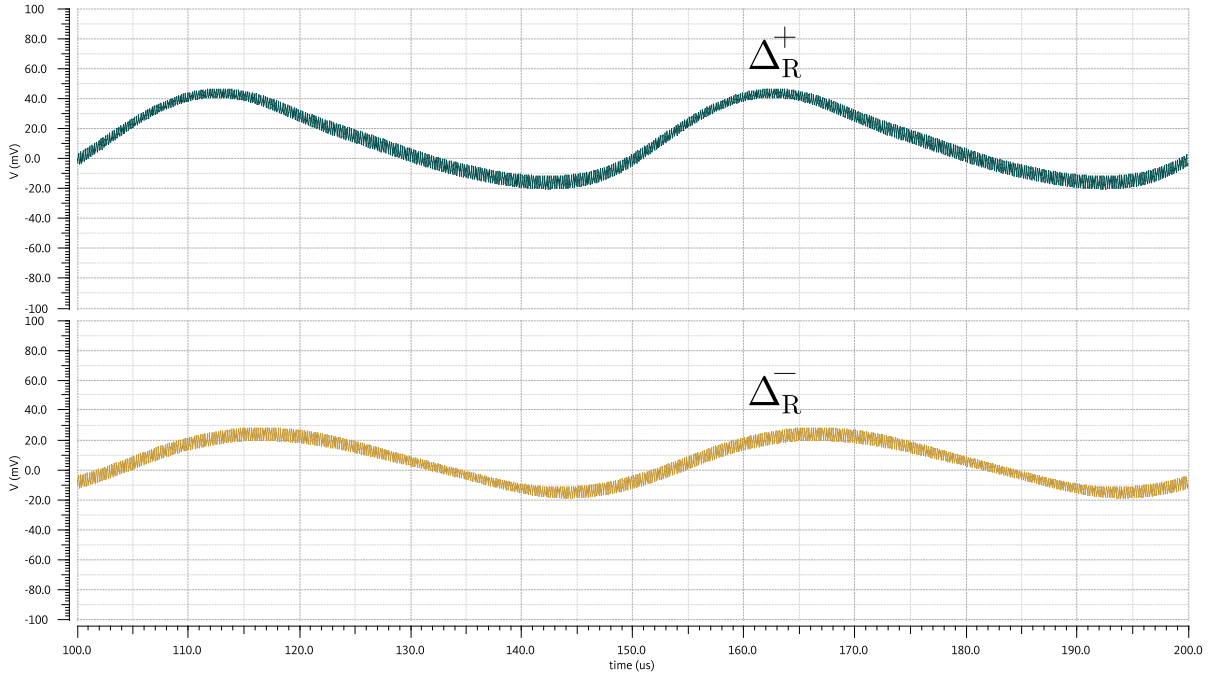

Figure 3.15: Class–CTA Rails' error for a 20 kHz, 3 V input.

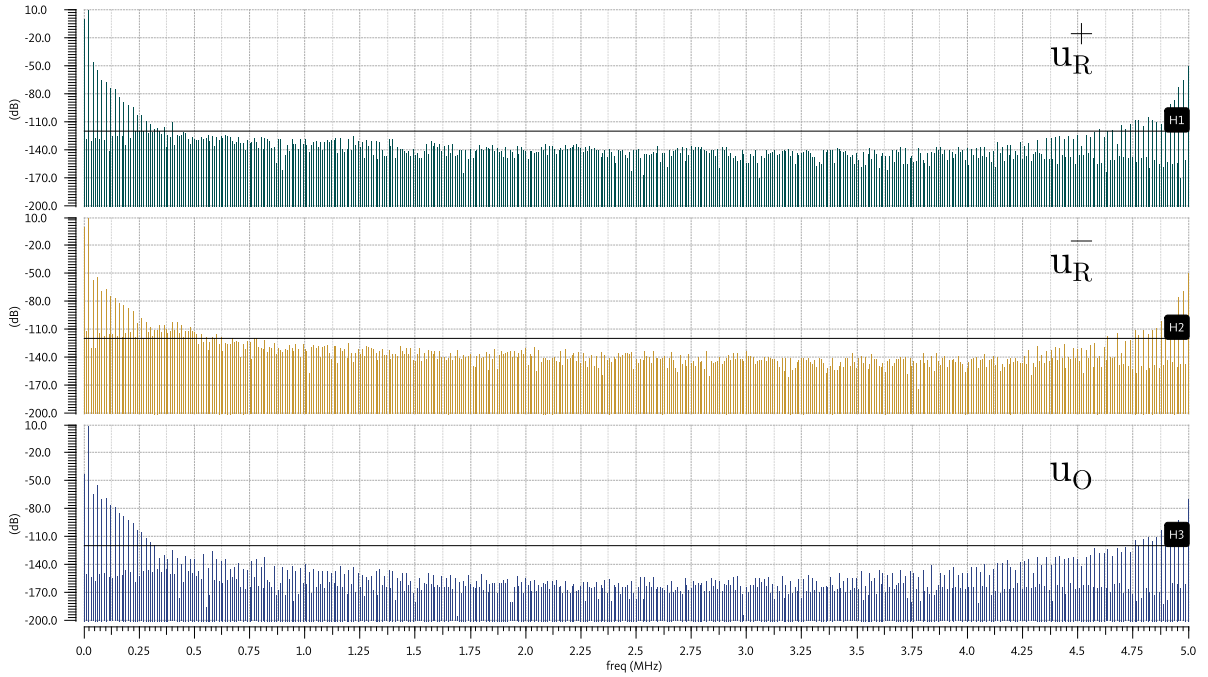

Figure 3.16: Class–CTA rails and output DFTs for a 20 kHz, 3 V input.

Finally, a comparison on the power stage's linearity and efficiency, when it is configured in the Class–CTA topology against a pure Class–A scheme (where the stage uses the fixed $\pm V_R$ supply), follows. Figures 3.17 and 3.18 depict the output DFT for the two schemes; horizontal lines at -120 dBV mark a practically negligible power level region. Linearity is excellent, with some indicative results on the levels of the fundamental (1st harmonic) and the dominant harmonic tones (2nd and 3rd) at the stage's output being gathered in Tables 3.1 and 3.2. The 2nd and 3rd harmonic tones of Class–CTA are at lower levels compared to the ones of Class–A operation, due to the almost constant u_{DS} of the output devices in the former case.

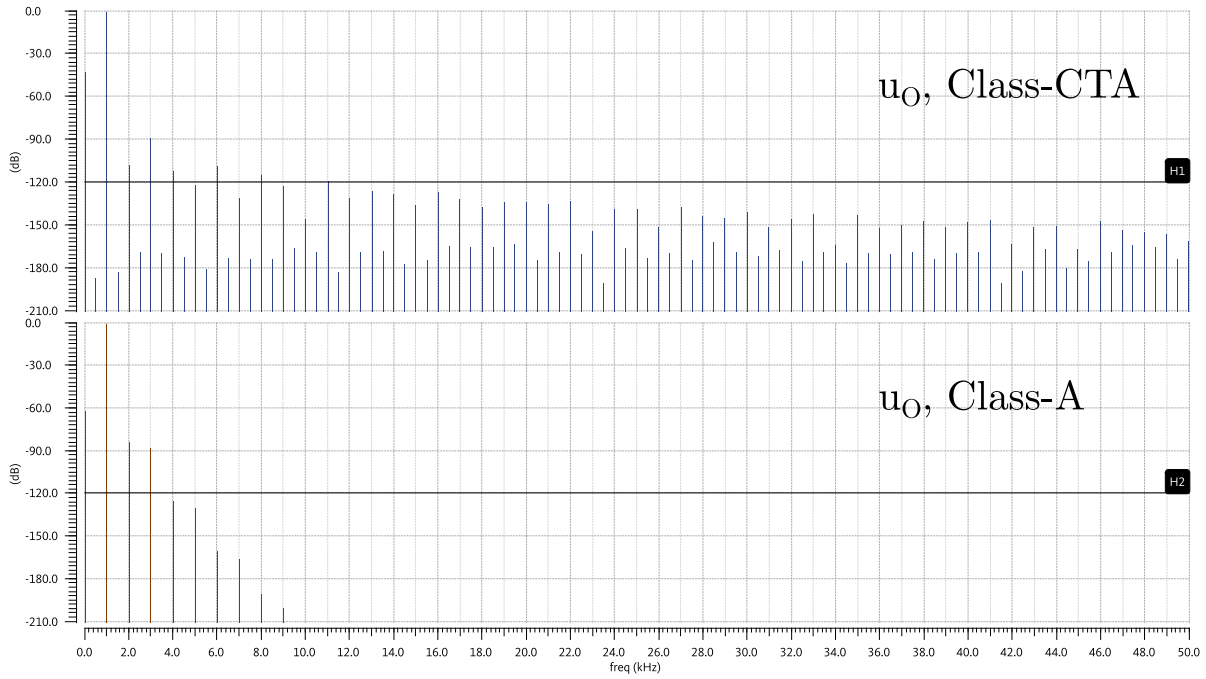

Figure 3.17: Class–CTA vs. Class–A output DFTs for an 1 kHz, 1 V input.

Table 3.1: 1st, 2nd, and 3rd output harmonic levels for an 1 kHz, 1 V input.

Harmonic	**Class–CTA**	**Class–A**
1st	-0.68 dBV	-0.66 dBV
2nd	-107.8 dBV	-84.0 dBV
3rd	-88.8 dBV	-87.9 dBV

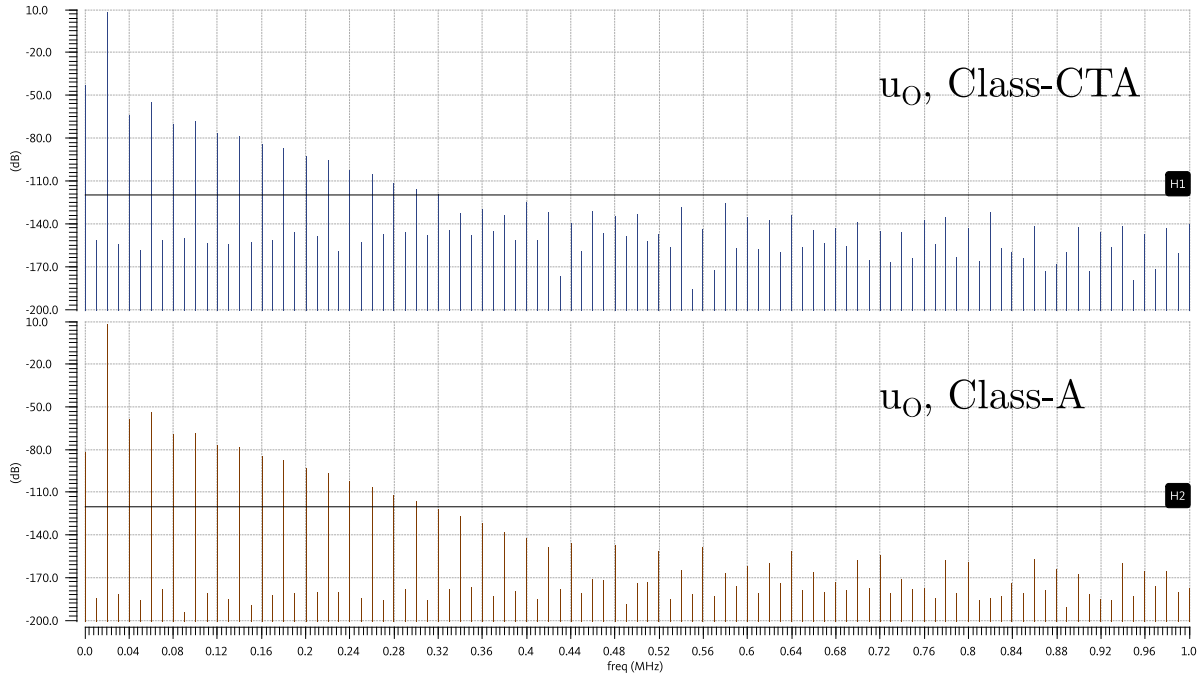

Figure 3.18: Class–CTA vs. Class–A output DFTs for a 20 kHz, 3 V input.

Table 3.2: 1st, 2nd, and 3rd output harmonic levels for a 20 kHz, 3 V input.

Harmonic	**Class–CTA**	**Class–A**
1st	8.85 dBV	8.87 dBV
2nd	−64.0 dBV	−58.1 dBV
3rd	−54.7 dBV	−53.7 dBV

The power stage efficiency, evaluated as the ratio of the load power over the load power plus the power dissipated at the output transistors, is also greatly improved. Figure 3.19 presents the peak efficiency as a function of the input signal amplitude, and indicates that Class–CTA achieves peak numbers of 12.3% and 54.7% at an input signal of 1 V and 3 V peak, respectively; the corresponding numbers for the push–pull Class–A variant are 2.2% and 19.4%. The peak efficiency improvement gets more pronounced at lower input amplitudes, where a Class–A scheme suffers more. Opting for a lower tracking margin voltage in Class–CTA will lead to further improvement in its power stage's efficiency, as u_M is the decisive factor to the peak efficiency that can be achieved by the architecture.

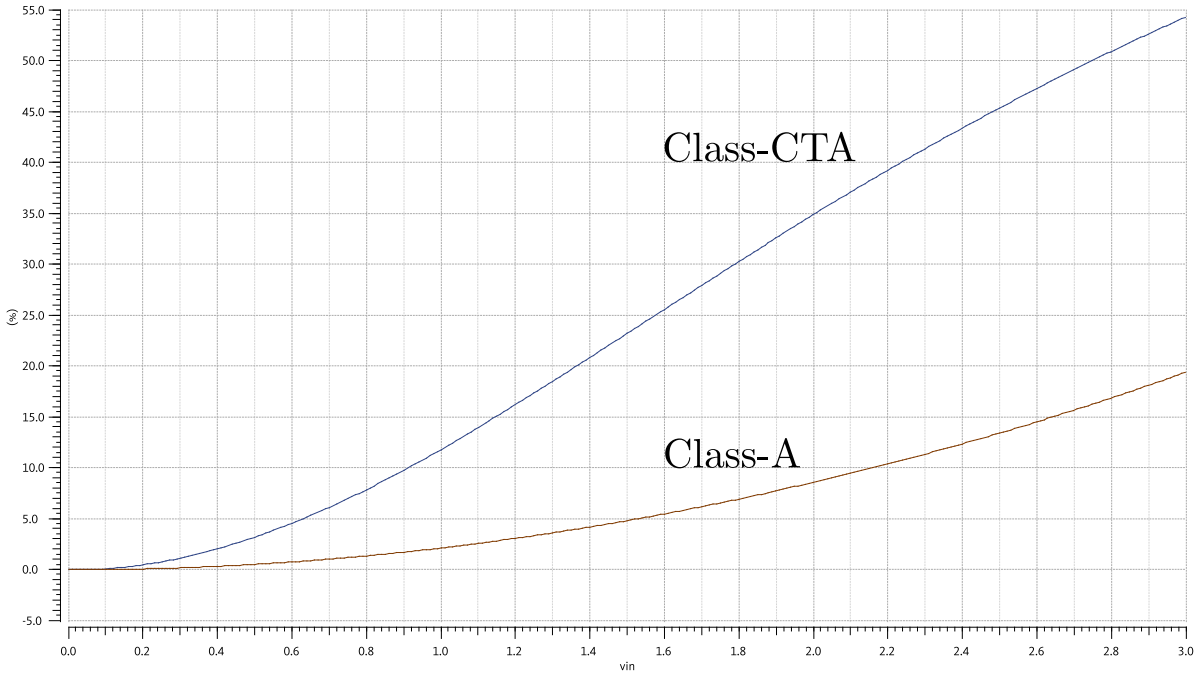

Figure 3.19: Class–CTA vs. Class–A power stage efficiency.

3.5 Summary

This chapter presented a power stage architecture able to combine high–linearity with high–efficiency. The topology uses a push–pull Class–A power stage core, and its supply rails are generated by two buck–converters that continuously track its output voltage with a small constant margin; thus, a minimum and constant voltage drop on the output devices is maintained, which in turn dramatically reduces power loses and improves linearity of the stage. Theoretical analysis of the topology and its feedback control are presented, while a proof–of–concept design example is implemented and simulated, highlighting the potential of the proposed architecture.

References

[1] Douglas Self. *Audio Power Amplifier Design*. 6th ed. Focal Press, 2013.

[2] Shon-Hang Wen et al. "A Load-Adaptive Class-G Headphone Amplifier With Supply-Rejection Bandwidth Enhancement Technique". In: *IEEE Journal of Solid-State Circuits* 51.10 (Oct. 2016), pp. 2241–2251. DOI: 10.1109/jssc.2016.2581802.

[3] Alex Lollio, Giacomino Bollati, and Rinaldo Castello. "Class-G headphone driver in 65nm CMOS technology". In: *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*. IEEE, Feb. 2010. DOI: 10.1109/isscc.2010.5434039.

[4] Shon-Hang Wen et al. “A 130dB PSRR, 108dB DR and 95dB SNDR, ground-referenced audio decoder with PSRR-enhanced load-adaptive Class-G 16Ohm headphone amplifiers”. In: *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. IEEE, Nov. 2015. DOI: 10.1109/asscc.2015.7387442.

[5] Kunhee Cho and Ranjit Gharpurey. “An Efficient Class-G Stage for Switching RF Power Amplifier Applications”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 66.4 (Apr. 2019), pp. 597–601. DOI: 10.1109/tcsii.2018.2870277.

[6] Nikolai Wolff, Wolfgang Heinrich, and Olof Bengtsson. “The efficiency/bandwidth trade-off in class-G supply-modulated power amplifiers”. In: *2017 47th European Microwave Conference (EuMC)*. IEEE, Oct. 2017. DOI: 10.23919/eumc.2017.8230892.

[7] Song Hu, Shouhei Kousai, and Hua Wang. “A Broadband Mixed-Signal CMOS Power Amplifier With a Hybrid Class-G Doherty Efficiency Enhancement Technique”. In: *IEEE Journal of Solid-State Circuits* 51.3 (Mar. 2016), pp. 598–613. DOI: 10.1109/jssc.2015.2508023.

[8] Sumati Sehajpal et al. “Impact of Switching Glitches in Class-G Power Amplifiers”. In: *IEEE Microwave and Wireless Components Letters* 22.6 (June 2012), pp. 282–284. DOI: 10.1109/lmwc.2012.2197383.

[9] K. Higashiyama. “SPICE simulation of variant class H hybrid power module”. In: *Proceedings of 1995 Japan International Electronic Manufacturing Technology Symposium*. IEEE. DOI: 10.1109/iemt.1995.541090.

[10] J. Gubelmann et al. “High-efficiency dynamic supply CMOS audio power amplifier for low-power applications”. In: *Microelectronics Journal* 40.8 (Aug. 2009), pp. 1175–1183. DOI: 10.1016/j.mejo.2009.03.003.

[11] Xiang Zhang and Liter Siek. “A highly efficient, 420mW class-H headphone amplifier with single power supply rail”. In: *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. IEEE, June 2015. DOI: 10.1109/edssc.2015.7285140.

[12] Xiang Zhang and Liter Siek. “An 80.4% Peak Power Efficiency Adaptive Supply Class H Power Amplifier for Audio Applications”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.6 (June 2017), pp. 1954–1965. DOI: 10.1109/tvlsi.2017.2666268.

[13] Nardi Utomo et al. “An 87% Peak Efficiency, 37W, Class H Audio Amplifier with GaN Output Stage”. In: *2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*. IEEE, Oct. 2018. DOI: 10.1109/norchip.2018.8573508.

[14] Jingqi Liu et al. "An envelope tracking H-bridged audio amplifier with improved efficiency and thd less than 0.1%". In: *2012 25th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*. IEEE, Apr. 2012. DOI: 10.1109/ccece.2012.6334867.

[15] Guillermo Velasco-Quesada et al. "Class H Power Amplifier for Power Saving in Fluxgate Current Transducers". In: *IEEE Sensors Journal* 16.8 (Apr. 2016), pp. 2322–2330. DOI: 10.1109/jsen.2016.2516399.

[16] Sankalp S. Modi, Poras T. Balsara, and Oren E. Eliezer. "Reduced bandwidth class H supply modulation for wideband RF power amplifiers". In: *WAMICON 2012 IEEE Wireless & Microwave Technology Conference*. IEEE, Apr. 2012. DOI: 10.1109/wamicon.2012.6208439.

[17] Tony Chan Carusone, David Johns, and Kenneth Martin. *Analog Integrated Circuit Design*. 2nd ed. John Wiley & Sons, Inc., 2011.

[18] Remco J. Wiegerink. *Analysis and Synthesis of MOS Translinear Circuits*. 1st. The Springer International Engineering and Computer Science. Springer Science+Business Media LLC, 1993.

[19] Robert W. Erickson and Dragan Marksimović. *Fundamentals of Power Electronics*. 2nd. Kluwer Academic Publishers, 2004.

[20] David L. Elliott. *Bilinear Control Systems - Matrices in Action*. 1st. Vol. 169. Applied Mathematical Sciences. Springer Science+Business Media B.V. 2009, 2000.

[21] Hassan K. Khalil. *Nonlinear Systems*. 3rd. Prentice Hall, 2002.

[22] Corentin Briat. *Linear Parameter-Varying and Time-Delay Systems*. Springer Berlin Heidelberg, 2015. DOI: 10.1007/978-3-662-44050-6.

[23] Javad Mohammadpour and Carsten W. Scherer, eds. *Control of Linear Parameter Varying Systems with Applications*. Springer US, 2012. DOI: 10.1007/978-1-4614-1833-7.

[24] K. C. Toh, M. J. Todd, and R. H. Tütüncü. "SDPT3 — A Matlab software package for semidefinite programming, Version 1.3". In: *Optimization Methods and Software* 11.1-4 (1999), pp. 545–581. DOI: 10.1080/10556789908805762. eprint: https://doi.org/10.1080/10556789908805762. URL: https://doi.org/10.1080/10556789908805762.

[25] Steven Diamond and Stephen Boyd. "CVXPY: A Python-embedded modeling language for convex optimization". In: *Journal of Machine Learning Research* 17.83 (2016), pp. 1–5.

[26] J. Löfberg. "YALMIP : A Toolbox for Modeling and Optimization in MATLAB". In: *In Proceedings of the CACSD Conference*. Taipei, Taiwan, 2004.

Conclusion and Further Research

In the first part of the thesis, two general methodologies for the estimation of harmonic and intermodulation distortion were presented. Both methods are general and systematic, rely on a modeling transformation of the examined circuit into a structure of interconnected G_m–stages, and through some approximation assumptions they provide highly accurate distortion estimation results while maintaining a fast computational profile. Some meaningful research directions stemming from this thematic axis are the following:

- The inclusion of inductors in both the harmonic and the intermodulation distortion estimation methods. The presented work does not account for the presence of inductors in the circuit under distortion examination; only resistors and capacitors are allowed to be present apart from G_m–stages. However, inductors can be accounted for in the same manner capacitors are. Starting with the modification of equations 1.24 and 2.7, matrices similar to F^f, W^f, F^h, W^h for the harmonic case, and F^f, W^f, F^m, W^m for the intermodulation case, can be constructed for inductors.

- A validation of the appropriately small magnitude of the corresponding approximation error in the case of the intermodulation distortion estimation method. The approximation regarding the dominant distortion factors in section 2.3.2 can be validated retrospectively in a similar fashion as in the harmonic distortion estimation case in section 1.4.3.

In the second part a high–linearity and high–efficiency power stage architecture was demonstrated. The topology employs two buck–converters to generate continuously tracking rails to supply its push–pull Class–A power stage core. This significantly reduces power losses and the output devices, while simultaneously improves the overall linearity of the stage due to the almost constant voltage drop on the output transistors. For this thematic axis, it would be interesting to explore:

- The addition of a digital control scheme for the buck–converters' duty cycles. In applications where digital circuitry and memory is available, a lookup table

could be created for the converters' duty cycle values to be available and selected on the fly based on the input signal. Presence of an auxiliary feedback loop would still be needed though, to take up control in cases where the programmed driving of the converters proves inadequate, as in cases of unpredicted exogenous disturbances.

- The inclusion of a feed–forward control path. Such an additional path could be seen as a means to relax the bandwidth requirements of the buck–converters' controllers, and could further improve the overall performance of the architecture.