NATIONAL TECHNICAL UNIVERSITY OF ATHENS

SCHOOL OF ELECTRICAL & COMPUTER ENGINEERING

DIVISION OF ELECTRIC POWER

LABORATORY OF ELECTRIC MACHINES & POWER ELECTRONICS

Resonant Converter: Power Conversion, Optimal Layout and Magnetic Component Design

DOCTORAL THESIS

THEOFILOS PAPADOPOULOS

Electrical and Computer Engineer

Athens, October 2023

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ADVISORY COMMITTEE	Antonios Antonopoulos, Assistant Professor NTUA
	Antonios Kladas, Professor NTUA
	Stavros Papathanasiou, Professor NTUA

Approved by the seven-member examination committee on 20/10/2023

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Antonios Antonopoulos, Assistant Professor NTUA	Antonios Kladas, Professor NTUA	Stavros Papathanasiou, Professor NTUA
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Dimosthenis Peftitsis, Professor NTNU		Emmanouil Tatakis, Professor UoP
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Athens, October 2023

.....

Theofilos Papadopoulos
Electrical and Computer Engineer
Doctor of Engineering of NTUA

«The approval of this Doctoral Thesis by the School of Electrical and Computer Engineering of the National Technical University of Athens does not imply acceptance of the author's opinions», (N. 5343/1932, article 202, par. 2)

Η χρηματοδότηση της διατριβής πραγματοποιήθηκε από τον Ειδικό Λογαριασμό Κονδυλίων Έρευνας (ΕΛΚΕ) του ΕΜΠ για τα έτη 2019-2022 και από το Ίδρυμα Κρατικών Υποτροφιών (ΙΚΥ), στο πλαίσιο της χρηματοδότηση των «Ώριμων Διδακτορικών», για τα έτη 2022-2023.

εκ μέρους του ΙΚΥ:
Η υλοποίηση της διδακτορικής διατριβής συγχρηματοδοτήθηκε από την Ελλάδα και την Ευρωπαϊκή Ένωση (Ευρωπαϊκό Κοινωνικό Ταμείο) μέσω του Επιχειρησιακού Προγράμματος «Ανάπτυξη Ανθρώπινου Δυναμικού, Εκπαίδευση και Δια Βίου Μάθηση», 2014-2020, στο πλαίσιο της Πράξης «Ενίσχυση του ανθρώπινου δυναμικού μέσω της υλοποίησης διδακτορικής έρευνας Υποδράση 2: Πρόγραμμα χορήγησης υποτροφιών ΙΚΥ σε υποψηφίους διδάκτορες των ΑΕΙ της Ελλάδας.

Επιχειρησιακό Πρόγραμμα
Ανάπτυξη Ανθρώπινου Δυναμικού,
Εκπαίδευση και Διά Βίου Μάθηση

Με τη συγχρηματοδότηση της Ελλάδας και της Ευρωπαϊκής Ένωσης

Πρόλογος

Η ερευνητική διαδικασία είναι μια κατεξοχήν συλλογική εργασία και η παρούσα διδακτορική διατριβή δεν αποτελεί εξαίρεση. Διεξήχθη στο Εργαστήριο Ηλεκτρικών Μηχανών και Ηλεκτρονικών Ισχύος, της Σχολής Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών του ΕΜΠ, από τον Οκτώβριο του 2018 έως τον Οκτώβριο του 2023. Καθώς εκτείνεται σε διάφορα αντικείμενα του κλάδου, από τους μετατροπείς συντονισμού και τα μαγνητικά στοιχεία έως τις τεχνικές βελτιστοποίησης και την στατιστική, χρειάστηκε η συμβολή αρκετών συναδέλφων, εντός και εκτός του εργαστηρίου.

Αρχικά, θα ήθελα να ευχαριστήσω τον επιβλέποντα καθηγητή κ. Αντώνιο Αντωνόπουλο για την εξαιρετική συνεργασία που είχαμε όλο αυτό το διάστημα. Η στήριξη που παρείχε, οι εποικοδομητικές παρατηρήσεις του και η ενδελεχής επιμέλεια των επιστημονικών άρθρων που δημοσιεύσαμε, αλλά και της παρούσας διατριβής, αποτελέσαν καταλύτη για την ανάπτυξη των ερευνητικών μου ικανοτήτων αλλά και για την όσο το δυνατόν ομαλότερη περάτωση της εργασίας.

Επίσης, θα ήθελα να ευχαριστήσω τον καθηγητή κ. Αντώνιο Κλαδά, διευθυντή του Εργαστηρίου, για τις συμβουλές του και τις δημιουργικές (επιστημονικές και μη) συζητήσεις που είχαμε. Καθώς και τον καθηγητή κ. Σταύρο Παπαθανασίου για την επίβλεψη τον πρώτο χρόνο ένταξής μου στο μεταπτυχιακό πρόγραμμα της Σχολής.

Δεν θα μπορούσα να παραλείψω τη συμβολή του καθηγητή κ. Εμμανουήλ Τατάκη, τόσο κατά την διάρκεια περάτωσης της διπλωματικής εργασίας στο Εργαστήριο Ηλεκτρομηχανικής Μετατροπής Ενέργειας, αλλά και για τις χρήσιμες παρατηρήσεις και συμβουλές του στην επιμέλεια της παρούσας διατριβής. Στο ίδιο πλαίσιο, θα ήθελα να ευχαριστήσω και τον καθηγητή κ. Δημοσθένη Πεφτίτση, για τις καίριες παρατηρήσεις του και την θετική ανατροφοδότηση που παρείχε. Θα ήθελα, επίσης, να εκφράσω τις ευχαριστίες μου στους καθηγητές κ. Ιωάννη Γκόνο και κ. Ιωάννη Προυσαλίδη για τον χρόνο που αφιέρωσαν ως μέλη της επταμελούς επιτροπής, αλλά και για τον εξοπλισμό που αξιοποιήσαμε από το Εργαστήριο Υψηλών Τάσεων.

Ειδική αναφορά πρέπει να γίνει στη συμβολή του κ. Παναγιώτη Ζάννη, μέλος ΕΤΕΠ του Εργαστήριου, ο οποίος βοήθησε ουσιαστικά με την δημιουργικότητά του και τις τεχνικές του γνώσεις στην ανάπτυξη των μαγνητικών στοιχείων, των μετατροπέων και στις καθημερινές ανάγκες του εργαστηρίου. Καθώς και στον διδάκτορα της σχολής κ. Παναγιώτη Ροβολή, μέλος ΕΔΙΠ του τομέα, για την άριστη συνεργασία που είχαμε.

Τέλος, θα ήθελα να ευχαριστήσω τους προπτυχιακούς φοιτητές και υποψήφιους διδάκτορες του εργαστηρίου για την εξαιρετική συνεργασία που είχαμε όλα αυτά τα χρόνια, ιδιαιτέρως δε τον κ. Κωνσταντίνο Μάνο και τον κ. Δημήτριο Κοντό. Είθε να συνεχιστεί η κουλτούρα ουσιαστικής συνεργασίας, δημιουργικότητας και καλής διάθεσης που υπάρχει στο εργαστήριο και που όλοι και όλες έχουμε επιτύχει.

Δεν θα μπορούσα να κλείσω τον πρόλογο χωρίς μια αναφορά στο οικονομικό πλαίσιο εντός του οποίου εκπονήθηκε η συγκεκριμένη διατριβή, αλλά και συνολικότερα οι διδακτορικές εργασίες στην Ελλάδα. Το κυρίαρχο πλαίσιο, αυτό των υποτροφιών, είναι ανεπαρκές για να ανταποκριθεί στις πραγματικές ανάγκες της έρευνας και των υποψηφίων διδακτόρων που την πραγματοποιούν. Το πλαίσιο δεν προβλέπει στοιχειώδεις ανάγκες, όπως αυτή της ασφάλισης, της αγοράς εξοπλισμού ή της συμμετοχής σε επιστημονικά συνέδρια. Σε ορισμένες περιπτώσεις, οι όροι της υποτροφίας είναι άκρως δεσμευτικοί, τόσο ως προς το χρονικό τους πλαίσιο, όσο και ως προς το περιεχόμενο των παραδοτέων. Αυτό έχει ως αποτέλεσμα της άσκηση εξαιρετικής πίεσης του υποψήφιους, η οποία είναι αντιπαραγωγική και σε πολλές περιπτώσεις μειώνει την δυνητική ερευνητική συμβολή. Απαιτείται ένα γενικό πλαίσιο σταθερής εργασίας, στο οποίο θα αποτυπώνονται οι ιδιαιτερότητες κάθε αντικειμένου, ώστε να μπορούν οι υποψήφιοι να εργαστούν απρόσκοπτα, χωρίς περιττά άγχη και να αναπτύξουν την δημιουργικότητά τους, η οποία αποτελεί απαραίτητο και δομικό στοιχείο κάθε ερευνητικής εργασίας.

Αφιερωμένο σε όλους και όλες
που με στήριξαν αυτά τα χρόνια,
Θεόφιλος Παπαδόπουλος
Αθήνα, Οκτώβριος 2023

Περίληψη

Σύντομη Περίληψη της Διατριβής

Η παρούσα διδακτορική διατριβή συμβάλλει στην ανάλυση και τον σχεδιασμό μετατροπέων συντονισμού υψηλής συχνότητας, με έμφαση στον σχεδιασμό των μαγνητικών στοιχείων. Συνεισφέρει με τις τροποποιήσεις υφιστάμενων εξισώσεων και την εισαγωγή νέων για την ακριβή εκτίμηση της επαγωγής παραλληλόγραμμων επίπεδων περιελίξεων, ενός και πολλών επιπέδων, επιτρέποντας τη γρήγορη σχεδίαση και την εφαρμογή αλγορίθμων βελτιστοποίησης. Επιπλέον, η παρούσα διατριβή παρέχει λύσεις κλειστής μορφής των διαφορικών εξισώσεων που περιγράφουν όλες τις περιοχές λειτουργίας των μετατροπέων συντονισμού LC και LLC, παρέχοντας λεπτομερή εικόνα της συμπεριφοράς τους και θέτοντας τα κριτήρια για την επιλογή παθητικών και ενεργών στοιχείων. Πραγματοποιείται σύγκριση μεταξύ των περιοχών και ορίζονται οι οριακές συνθήκες μεταξύ κάθε περιοχής λειτουργίας. Η δομή έχει ως εξής:

Αρχικά, συγκεντρώνονται και παρατίθενται καλές πρακτικές σχεδιασμού πλακετών τυπωμένου κυκλώματος (ΠΤΚ), που διαχειρίζονται υψίσυχνες τάσεις και ρεύματα, των οποίων η δυσκολία σχεδιασμού έγκειται στο ότι περιλαμβάνουν σήματα υψηλής ισχύος και συχνότητας, καθώς και αναλογικά και ψηφιακά σήματα ελέγχου και μετρήσεων. Οι πρακτικές αυτές εμφανίζονται διάσπαρτες στη βιβλιογραφία (σε συγγράμματα και άρθρα), αλλά και σε συνεντεύξεις και παρουσιάσεις έμπειρων σχεδιαστών πλακετών υψηλών συχνοτήτων και ηλεκτρονικών ισχύος.

Στη συνέχεια, προτείνονται τροποποιήσεις σε υπάρχουσες εξισώσεις για τον υπολογισμό της επαγωγής επίπεδων παραλληλόγραμμων τυλιγμάτων ενός επιπέδου, με το σφάλμα εκτίμηση να παραμένει μικρό, όπως και στις αρχικές εξισώσεις. Η χρήση παραλληλόγραμμων τυλιγμάτων δίνει έναν επιπλέον βαθμό ελευθερίας στον σχεδιαστή, ενώ η ακριβής γνώση της επαγωγής διαδραματίζει σημαντικό ρόλο στον υπολογισμό των χαρακτηριστικών τιμών του μετατροπέα συντονισμού. Προτείνεται μία νέα μονώνυμη εξίσωση για τον υπολογισμό της επαγωγής παραλληλόγραμμων τυλιγμάτων πολλών επιπέδων, η οποία διατηρεί την υψηλή ακρίβεια εκτίμησης των εξισώσεων για τα τυλίγματα του ενός επιπέδου. Πραγματοποιείται συγκριτική μελέτη για την ακρίβεια των διάφορων εξισώσεων σε τυλίγματα ενός και πολλαπλών επιπέδων, αναδεικνύοντας αυτήν που παρέχει το μικρότερο σφάλμα, για κάθε περίπτωση. Γίνεται σύντομη ανάλυση της επίδρασης της εισαγωγής πυρήνα (τύπου φερρίτη) στη συμπεριφορά και την επαγωγή ενός επίπεδου τυλίγματος.

Τέλος, παρουσιάζονται αναλυτικά μοντέλα στο πεδίο του χρόνου για τους μετατροπείς συντονισμού σειράς και LLC, για όλες τις περιοχές λειτουργίας (επαγωγική, συντονισμού,

χωρητική), όπως αυτές προκύπτουν από τις λύσεις των διαφορικών εξισώσεων που περιγράφουν το κύκλωμα. Ιδιαίτερη έμφαση δίνεται στις οριακές συνθήκες των περιοχών και ειδικά στον διαχωρισμό μεταξύ περιοχής συνεχούς και ασυνεχούς αγωγής. Από τις λύσεις προκύπτουν οι τιμές της τάσης και του ρεύματος για κάθε κόμβο του μετατροπέα συντονισμού, καθώς και οι απαραίτητες συνθήκες για την επίτευξη ομαλής μετάβασης των διακοπτών υπό μηδενική τάση ή ρεύμα. Πραγματοποιείται σύγκριση μεταξύ διακοπτικών στοιχείων τύπου MOSFET και IGBT και αναδεικνύεται η πιο αποδοτική περιοχή λειτουργίας για το κάθε στοιχείο. Με βάση τις τιμές των ηλεκτρικών μεγεθών, προτείνεται μια διαδικασία επιλογής παθητικών και ενεργών στοιχείων, η οποία συμπεριλαμβάνει τα παρασιτικά στοιχεία των ημιαγωγικών διακοπτών.

Εκτενής Περίληψη της Διατριβής

Η χρήση των ορυκτών καυσίμων σε μηχανές αρχικά εξωτερικής και ύστερα εσωτερικής καύσης σήμανε μια τεράστια αλλαγή παραδείγματος στους τομείς της παραγωγής και της οικονομίας (βιομηχανία, μεταφορές, κατασκευές, εμπόριο, κ.ο.κ.). Ειδικά οι εξελίξεις του τελευταίου μισού αιώνα οδήγησαν σε μια τεχνολογική άνθιση, η οποία έχει επαναπροσδιορίσει κάθε πτυχή της καθημερινότητας των ανθρώπων, από την εκπαίδευση και την εργασία, μέχρι την επικοινωνία και την πολιτική.

Ωστόσο, η ευρεία και σχεδόν ανεξέλεγκτη χρήση των ορυκτών καυσίμων φέρει τη βασική ευθύνη για την εκπομπή αερίων του θερμοκηπίου (μεταξύ άλλων διοξείδιο του άνθρακα, φθοροχλωράνθρακες, οξείδια του νατρίου κ.α.), τα οποία οδηγούν στο φαινόμενο που σήμερα ονομάζουμε "κλιματική αλλαγή". Η διάδοση των οικιακών ηλεκτρονικών και η ψηφιοποίηση του συνόλου των υπηρεσιών επιδεινώνει περαιτέρω την κατάσταση, μέσω της ανάγκης για εξόρυξη πρώτων υλών αναγκαίων για τις ηλεκτρονικές συσκευές (πλακέτες, ημιαγωγούς, αισθητήρες, μπαταρίες, κ.ο.κ.), καθώς και με την έλλειψη αποτελεσματικής ανακύκλωσης τους.

Η ανάγκη για απομάκρυνση από τη χρήση ορυκτών καυσίμων έχει αναδειχθεί ποικιλοτρόπως, και έχει πλέον αναγνωριστεί μέσω των στόχων που έχει θέσει η ΕΕ για μείωση της εκπομπής ρύπων κατά 55% μέχρι το 2029 και τον πλήρη μηδενισμό τους μέχρι το 2050. Η επίτευξη αυτού του αρκετά αισιόδοξου στόχου περνάει μέσα από τον εξηλεκτρισμό των τομέων που ακόμα χρησιμοποιούν ορυκτά καύσιμα, κυρίως οι μεταφορές, η παραγωγή ηλεκτρικής ενέργειας, καθώς και σε έναν βαθμό η θέρμανση των κτηρίων.

Οι ηλεκτρονικοί μετατροπείς ισχύος αποτελούν στοιχειώδες δομικό κομμάτι της προσπάθειας εξηλεκτρισμού. Η διασύνδεση ανανεώσιμων πηγών ενέργειας με το δίκτυο απαιτεί κατάλληλη μετατροπή της τάσης και του ρεύματος, καθώς και έλεγχο της ποιότητας και της ποσότητας της παρεχόμενης ισχύος. Η φόρτιση των μπαταριών των ηλεκτρικών οχημάτων, καθώς και των σταθερών μονάδων αποθήκευσης, απαιτεί συγκεκριμένη ακολουθία φόρτισης υπό σταθερό ρεύμα και έπειτα υπό σταθερή τάση, κ.ο.κ. Επομένως, είναι απαραίτητη η ανάπτυξη μετατροπέων υψηλής απόδοσης, ώστε να επιτυγχάνεται η μέγιστη εκμετάλλευση της παραγόμενης ενέργειας, αλλά ταυτόχρονα με μεγάλο χρόνο ζωής. Σε αυτήν την κατεύθυνση, η αύξηση της διακοπτικής συχνότητας (από τα δεκάδες kHz στα εκατοντάδες kHz) οδηγεί σε μικρότερο όγκο και σε υψηλότερη απόδοση. Απαιτείται παράλληλα κατάλληλος σχεδιασμός όσον αφορά τις Πλακέτες Τυπωμένου Κυκλώματος (ΠΤΚ) και την επιλογή των ενεργών και παθητικών στοιχείων.

Οι υψίσυχνοι μετατροπείς συντονισμού συμπεριλαμβάνουν και ένα δίκτυο πηνίων και πυκνωτών, το οποίο, υπό τις κατάλληλες προϋποθέσεις, επιτυγχάνει μηδενικές (ή μειωμένες) διακοπτικές απώλειες. Οι μετατροπείς συντονισμού αποτελούν την ενδεδειγμένη λύση για τροφοδοτικά, μέχρι την τάξη των δεκάδων kW. Ωστόσο, τα τελευταία χρόνια έχει προταθεί μια πληθώρα νέων εφαρμογών, όπως η φόρτιση ηλεκτρικών οχημάτων, η τροφοδότηση κέντρων δεδομένων, κινητήριων συστημάτων αεροπλάνων και πλοίων, καθώς και η χρήση τους σε

μετατροπείς στερεάς κατάστασης, οι οποίοι δύναται να είναι πολυτερματικοί και να ελέγχουν τη ροή της ισχύος.

Η παρούσα διδακτορική διατριβή συμβάλλει στην ανάλυση και τον σχεδιασμό μετατροπέων συντονισμού υψηλής συχνότητας, με έμφαση στον σχεδιασμό των μαγνητικών στοιχείων. Συνεισφέρει με τις τροποποιήσεις υφιστάμενων εξισώσεων και την εισαγωγή νέων για την ακριβή εκτίμηση της επαγωγής παραλληλόγραμμων επίπεδων περιελίξεων, ενός και πολλών επιπέδων, επιτρέποντας τη γρήγορη σχεδίαση και την εφαρμογή αλγορίθμων βελτιστοποίησης. Επιπλέον, η παρούσα διατριβή παρέχει λύσεις κλειστής μορφής των διαφορικών εξισώσεων που περιγράφουν όλες τις περιοχές λειτουργίας των μετατροπέων συντονισμού LC και LLC, παρέχοντας λεπτομερή εικόνα της συμπεριφοράς τους και θέτοντας τα κριτήρια για την επιλογή παθητικών και ενεργών στοιχείων. Πραγματοποιείται σύγκριση μεταξύ των περιοχών και ορίζονται οι οριακές συνθήκες μεταξύ κάθε περιοχής λειτουργίας.

Πρακτικές Σχεδιασμού Πλακετών Τυπωμένου Κυκλώματος

Ο σχεδιασμός πλακετών τυπωμένου κυκλώματος, στον τομέα των ηλεκτρονικών ισχύος, αποτελεί ένα πολύπλοκο έργο. Οι ΠΤΚ συνδυάζουν σήματα ισχύος συνεχούς και εναλλασσομένου ρεύματος και μάλιστα υψηλών συχνοτήτων, σήματα χαμηλής ισχύος για τον έλεγχο του μετατροπέα, καθώς και αναλογικά σήματα μετρήσεων. Ένας βασικός στόχος ενός καλού σχεδιασμού είναι ελαχιστοποίηση της αλληλεπίδρασης μεταξύ των τριών κατηγοριών, ώστε να μην αλλοιώνονται τα ευαίσθητα σήματα.

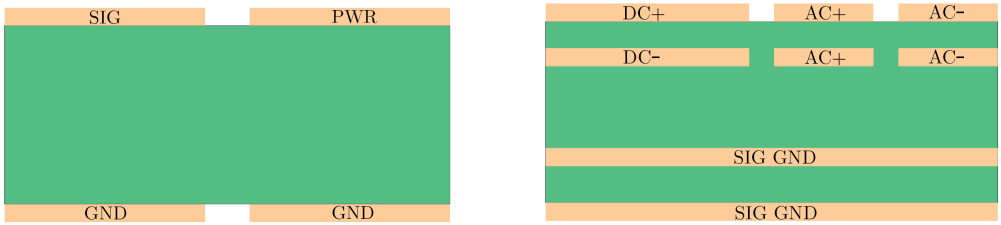
Ένας δεύτερος στόχος είναι η ελαχιστοποίηση της παρασιτικής επαγωγής, η οποία δύναται να προκαλέσει υπερτάσεις στα άκρα των διακοπτών όταν το ρεύμα έχει ταχείες μεταβολές, με αποτέλεσμα την καταπόνηση ή και την καταστροφή τους. Η παρασιτική χωρητικότητα μπορεί να είναι θεμιτή, στην περίπτωση των δρόμων συνεχούς τάσης, ή αθέμιτη, στην περίπτωση των δρόμων εναλλασσόμενης τάσης. Σε κάθε περίπτωση, η εκτίμηση των παρασιτικών στοιχείων είναι σημαντική και παρατίθενται οι εξισώσεις για τον υπολογισμό τους, για τις βασικές αρχιτεκτονικές θετικών και αρνητικών δρόμων.

Ειδικά όσον αφορά την παρασιτική χωρητικότητα, σε δρόμους με υψίσυχνο φασματικό περιεχόμενο, παρατηρείται ένα ισχυρό ρεύμα μετατόπισης. Το ρεύμα επιστροφής ακόμα και στην περίπτωση που έχει διαθέσιμη ολόκληρη την επιφάνεια, τείνει να συγκεντρώνεται κάτω από τον θετικό δρόμο. Αυτό αυξάνει την τόσο την πραγματική αντίσταση, όσο και την εμπέδηση του δρόμου, αλλά ταυτόχρονα περιορίζει και τη δυνατότητα του ρεύματος επιστροφής να αλλοιώσει άλλα πιο ασθενή σήματα.

Δύο παράλληλοι δρόμοι, οι οποίοι φέρουν διαφορετικά σήματα, μικρής και υψηλής ισχύος, ταυτόχρονα, οφείλουν να έχουν μια αρκούντως μεγάλη απόσταση μεταξύ τους, ώστε να μην αλληλεπιδρούν. Αυτή η απόσταση προκύπτει από τον εμπειρικό κανόνα του 3-5 w, ο οποίος σημαίνει πως πρέπει να απέχουν τρεις με πέντε φορές το πλάτος τους w. Εάν αυτό δεν είναι εφικτό, η τοποθέτηση ενός γειωμένου δρόμου στο ενδιάμεσο αποτελεί την αμέσως επόμενη καλύτερη λύση. Σε κάθε περίπτωση, πρέπει να αποφεύγεται η παρουσία αγώγιμων δρόμων οι

οποίοι δεν έχουν αναφορά, αλλά το δυναμικό τους αιωρείται (floating). Επίσης, η χάραξη των δρόμων στις δύο πλευρές της πλακέτας, με κάθετες διευθύνσεις μπορεί να μειώσει σημαντικά την αλληλεπίδρασή τους.

Με τον σχεδιασμό να απομονώνει σήματα κοινού είδους (αναλογικά, ψηφιακά, ισχύος) σε συγκεκριμένα μέρη της πλακέτας, είναι δυνατό να απεικονίσουμε κάθε είδος ως έναν δρόμο, σε ένα συγκεκριμένο επίπεδο. Η σειρά με την οποία τοποθετούνται αυτοί οι δρόμοι και τα αντίστοιχα επίπεδα, διαδραματίζει σημαντικό ρόλο στην ελαχιστοποίηση της αλληλεπίδρασής τους. Στο Σχήμα 1 παρουσιάζεται μία από τις βέλτιστες δυνατές επιλογές για πλακέτες δύο και τεσσάρων επιπέδων.



(a) 2-επίπεδα **(b)** 4-επίπεδα

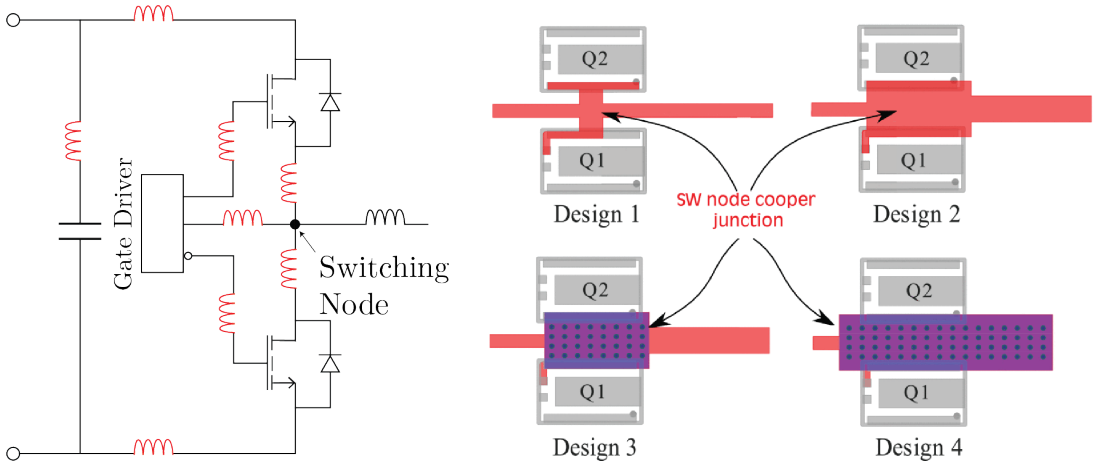
Figure 1 Τομή πλακέτας δύο και τεσσάρων επιπέδων. Προτεινόμενη σειρά επιπέδων.

Για την περαιτέρω μείωση της επίδρασης της παρασιτικής επαγωγής και των φαινομένων που αυτή προκαλεί, ενδείκνυται η τοποθέτηση πυκνωτών κοντά στα ενεργά στοιχεία (ολοκληρωμένα κυκλώματα, ζυγοί συνεχούς ρεύματος διακοπτών, κ.ο.κ.). Οι πυκνωτές έχουν διττό ρόλο: δημιουργούν έναν δρόμο για το ρεύμα, όταν αυτό διακόπτεται απότομα από κάποιον διακόπτη, καταστέλλοντας την υπέρταση και μπορούν επίσης να λειτουργήσουν ως τοπική αποθήκευση ενέργειας, ώστε όταν απαιτείται απότομη αύξηση του ρεύματος, αυτό αν μην έρχεται εξ' ολοκλήρου από την πηγή.

Ιδιαίτερη προσοχή χρειάζεται στον σχεδιασμό των διακοπτικών κόμβων (σημείο συνάντησης επαγωγού, διακόπτη και διόδου), οι οποίοι είναι υπεύθυνοι για την παραμόρφωση των κυματομορφών και την εκπομπή ηλεκτρομαγνητικού θορύβου. Στο Σχήμα 2 παρουσιάζεται το σχηματικό και η διάταξη ενός διακοπτικού κόμβου, με τέσσερις διαφορετικές διαμορφώσεις. Εξ' αυτών, η διάταξη 4 παρουσιάζει την καλύτερη συμπεριφορά από πλευράς θερμικής απαγωγής, ηλεκτρομαγνητικής συμβατότητας και ταλαντώσεων στον ζυγό.

Ένας τρόπος για την αύξηση της απόδοσης του μετατροπέα είναι η χρήση πολλαπλών στοιχείων τοποθετημένων παράλληλα. Αυτή η τακτική μειώνει τις απώλειες αγωγής και υπό τον κατάλληλο σχεδιασμό, αυξάνει την απαγωγή θερμότητας και μειώνει τις υπερτάσεις και τις διακοπτικές απώλειες. Βασική προϋπόθεση είναι ο συμμετρικός σχεδιασμός, έτσι ώστε κάθε ημιαγωγικό στοιχείο να έχει την ίδια (παρασιτική) επαγωγή σε κάθε δρόμο και το ρεύμα να διαιρείται όσο το δυνατόν πιο ομοιόμορφα μεταξύ των στοιχείων.

Επίπεδα Τυλίγματα



(a) Σχηματικό **(b)** Διαμόρφωση ΠΤΚ

Figure 2 Παρασιτική επαγωγή τοπολογίας ημι-γέφυρας.

Τα επίπεδα τυλίγματα αποτελούν έναν εναλλακτικό τρόπο σχεδιασμού μαγνητικών στοιχείων. Τα συμβατικά στοιχεία έχουν τυλίγματα τα οποία εκτείνονται στους τρεις άξονες, με κέντρο συνήθως το άκρο ενός πυρήνα (EI, UI, κ.ο.κ.). Τα επίπεδα τυλίγματα εκτείνονται στην xy-επιφάνεια, ενώ διατηρούν ένα μικρό ύψος της τάξης των μερικών χιλιοστών στην z-διάσταση. Μπορούν να χρησιμοποιηθούν σε περιπτώσεις και εφαρμογές στις οποίες το χαμηλό προφίλ είναι επιθυμητό, όπως οι καμπίνες δομημένης καλωδίωσης των κέντρων δεδομένων, οι ενσωματωμένοι στο ηλεκτρικό όχημα φορτιστές, κ.ο.κ.

Πέραν του χαμηλού προφίλ, τα επίπεδα τυλίγματα παρουσιάζουν καλύτερη απαγωγή της θερμότητας λόγω της τυπικά μεγαλύτερης επιφάνειάς τους. Μπορούν επίσης να παραχθούν μαζικά με χαμηλό κόστος, καθώς και με ακριβή και επαναλήψιμη τιμή επαγωγής. Επίσης, λόγω των 35-70 μm ύψους του χαλκού, δεν παρουσιάζουν επιδερμικό φαινόμενο για συχνότητες έως και 3.5 MHz.

Η επαγωγή των επίπεδων τυλιγμάτων εξαρτάται στενά από την γεωμετρική τους μορφή. Για τετράγωνα τυλίγματα ενός επιπέδου τρεις διαδεδομένοι τύποι είναι των Wheeler, Rosa και ο Monomial, και ορίζονται ως

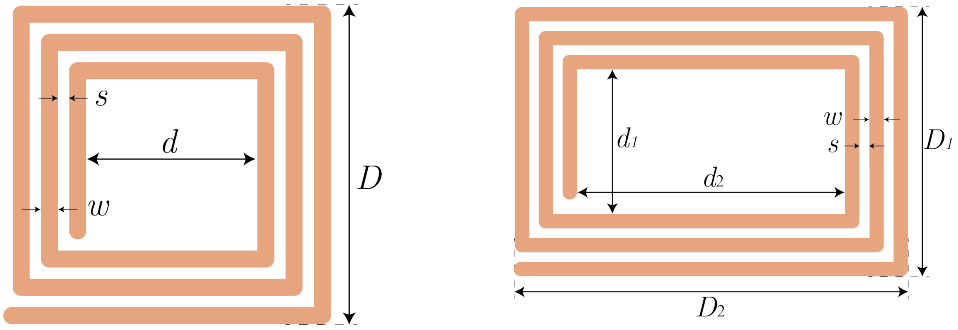
$$L_{\mathrm{WH}} = 2.34\mu_0 N^2 \frac{\frac{D+d}{2}}{1 + 2.75\frac{D-d}{D+d}}, \tag{1}$$

$$L_{\mathrm{RS}} = \frac{1.27}{2}\mu_0 N^2 \frac{D+d}{2}\left(\ln\left(\frac{2.07}{\frac{D-d}{D+d}}\right) + 0.18\frac{D-d}{D+d} + 0.13\left(\frac{D-d}{D+d}\right)^2\right), \tag{2}$$

$$L_{\mathrm{MN}} = 1.62 \cdot 10^{-3} D^{-1.21} w^{-0.147} \left(\frac{D+d}{2}\right)^{2.4} N^{1.78} s^{-0.03}, \tag{3}$$

όπου D η εξωτερική πλευρά, d η εσωτερική, w το πλάτος του δρόμου, s η απόσταση μεταξύ των δρόμων, και N το πλήθος των περιελίξεων. Τα μεγέθη αυτά παρουσιάζονται στο Σχήμα 3a και η εσωτερική πλευρά, συναρτήσει των άλλων μεγεθών δίνεται από

$$d = D - 2N(w + s) - 2s. \tag{4}$$



(a) Τετράγωνο **(b)** Παραλληλόγραμμο

Figure 3 Γεωμετρικά χαρακτηριστικά επίπεδου τυλίγματος.

Η ανάπτυξη παραλληλόγραμμων τυλιγμάτων προσδίδει στον σχεδιασμό άλλον έναν βαθμό ελευθερίας, καθώς οι δύο πλευρές μπορούν να εκτείνονται ανεξάρτητα η μία από την άλλη. Ωστόσο, ο υπολογισμός της επαγωγής τους είναι πολύπλοκος, καθώς δεν υπάρχουν αντίστοιχες εύκολες στη χρήση και την ερμηνεία εξισώσεις. Η παρούσα διατριβή προτείνει κατάλληλες τροποποιήσεις ώστε να γίνει δυνατή η εκτίμηση παραλληλόγραμμων τυλιγμάτων από τις εξισώσεις (1) - (3), ελαχιστοποιώντας το σφάλμα της εκτίμησης.

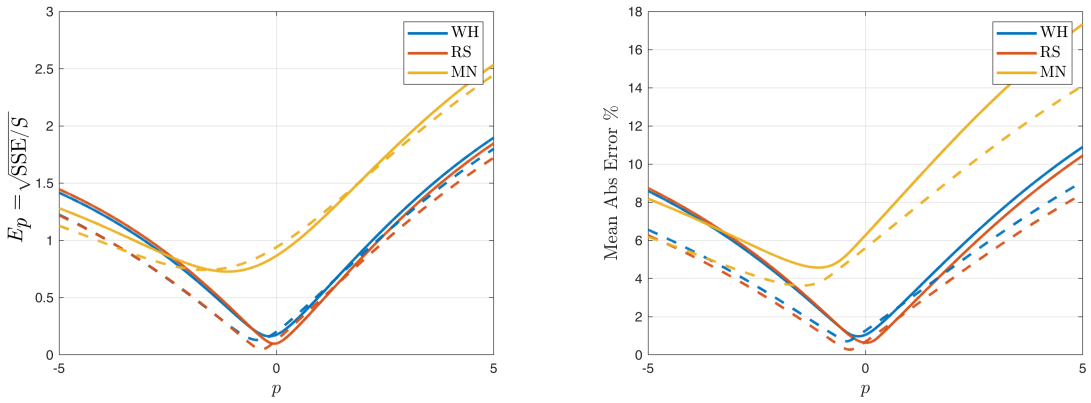
Με τη χρήση του γενικευμένου μέσου όρου, δύναται η εξωτερική πλευρά D των εξισώσεων (1) - (3) να αντικατασταθεί από μια νόρμα p των πλευρών D_1 και D_2 ($||D||_p = \left(D_1^p + D_2^p\right)^{\frac{1}{p}}$) του παραλληλόγραμμου τυλίγματος, όπως παρουσιάζεται στο Σχήμα 3b. Η επιλογή της νόρμας αποτελεί ένα πρόβλημα βελτιστοποίησης, κριτήριο του οποίου μπορεί να είναι η RMS τιμή του σφάλματος για ένα σύνολο τυλιγμάτων

$$E_p = \sqrt{\frac{\mathrm{SSE}(p)}{S}} \tag{5}$$

ή το μέσο απόλυτο σφάλμα

$$\mathrm{MAE}_p\% = \frac{1}{S}\sum_{i=1}^{S}\frac{|L_{sim,i} - L_{\{\mathrm{WH,RS,MN}\},i}|}{L_{sim,i}} \cdot 100 \tag{6}$$

όπου $\mathrm{SSE}(p) = \sum_{i=1}^{S}\left(L_{\mathrm{sim},i} - L_{\{\mathrm{WH,RS,MN}\},i}(p)\right)^2$, S το συνολικό πλήθος των τυλιγμάτων, $L_{\mathrm{sim},i}$ το αποτέλεσμα της προσομοίωσης για το i δείγμα (τύλιγμα) και $L_{\{\mathrm{WH,RS,MN}\},i}$ το αποτέλεσμα των εξισώσεων Wheeler, Rosa και Monomial, αντίστοιχα, για το i δείγμα.



(a) (b)

Figure 4 RMS και μέσο απόλυτο σφάλμα συναρτήσει του p για το τυχαίο υποσύνολο (διακεκομμένη γραμμή) και για το πλήρες σύνολο (συνεχής γραμμή), για κάθε εξίσωση. Το βέλτιστο p_{opt} εξαρτάται από το εκάστοτε υποσύνολο, αλλά όλα παρουσιάζουν ολικό ελάχιστο στην περιοχή του 0 για τις εξισώσεις Wheeler και Rosa και του -1 για το Monomial.

Τα αποτελέσματα της βελτιστοποίησης για νόρμες από -5 έως 5 παρουσιάζονται στο Σχήμα 4. Προκύπτει πως οι δύο πρώτες εξισώσεις παρουσιάζουν βέλτιστο για την νόρμα $p = 0$ με μέσο απόλυτο σφάλμα μικρότερο του 1.1% , ενώ η τρίτη για την νόρμα $p = -1$ με μέσο απόλυτο σφάλμα μικρότερο του 4.6%. Συνεπώς οι τροποποιημένες εξισώσεις είναι

$$L_{\text{WH}} = 2.34\mu_0 N^2 \frac{\|\overline{D}\|_0}{1 + 2.75\|\rho\|_0}, \tag{7}$$

$$L_{\text{RS}} = \frac{1.27}{2}\mu_0 N^2 \|\overline{D}\|_0 \left(\ln\left(\frac{2.07}{\|\rho\|_0}\right) + 0.18\|\rho\|_0 + 0.13\|\rho\|_0^2\right), \tag{8}$$

$$L_{\text{MN}} = 1.5428\mu_0 N^{1.78} \|\overline{D}\|_{-1}^{2.4} \|D\|_{-1}^{-1.21} w^{-0.147} s^{-0.03}, \tag{9}$$

όπου $\|\overline{D}\|_y = \frac{\|D\|_y + \|d\|_y}{2}$ και $\|\rho\|_y = \frac{\|D\|_y - \|d\|_y}{\|D\|_y + \|d\|_y}$.

Τα αποτελέσματα επιβεβαιώνονται από εργαστηριακές μετρήσεις, με σφάλμα μικρότερο του 1.5% για την εξίσωση Wheeler, μικρότερο του 1.3% για την εξίσωση Rosa, και μικρότερο του 5.5.% για την εξίσωση Monomial.

Ιδιαίτερο ενδιαφέρον παρουσιάζει η συμπεριφορά του σφάλματος συναρτήσει του λόγου D_1/D_2, ο οποίος αντιπροσωπεύει τον βαθμό παραμόρφωσης από το τετράγωνο προς το παραλληλόγραμμο σχήμα. Στο Σχήμα 5 παρουσιάζονται τα αποτελέσματα του μέσου απόλυτου σφάλματος, με ομαδοποίηση τον λόγο D_1/D_2, για τις τρεις εξισώσεις και για τρεις διαφορετικές νόρμες $p = \{-1, 0, 1\}$. Όσον αφορά τα βέλτιστα p, για τις πρώτες δύο εξισώσεις ($p = 0$) το σφάλμα μειώνεται όσο ο λόγος τείνει προς την μονάδα (τετράγωνο σχήμα), ενώ η τρίτη ($p = -1$) δεν παρουσιάζει μονότονη συμπεριφορά.

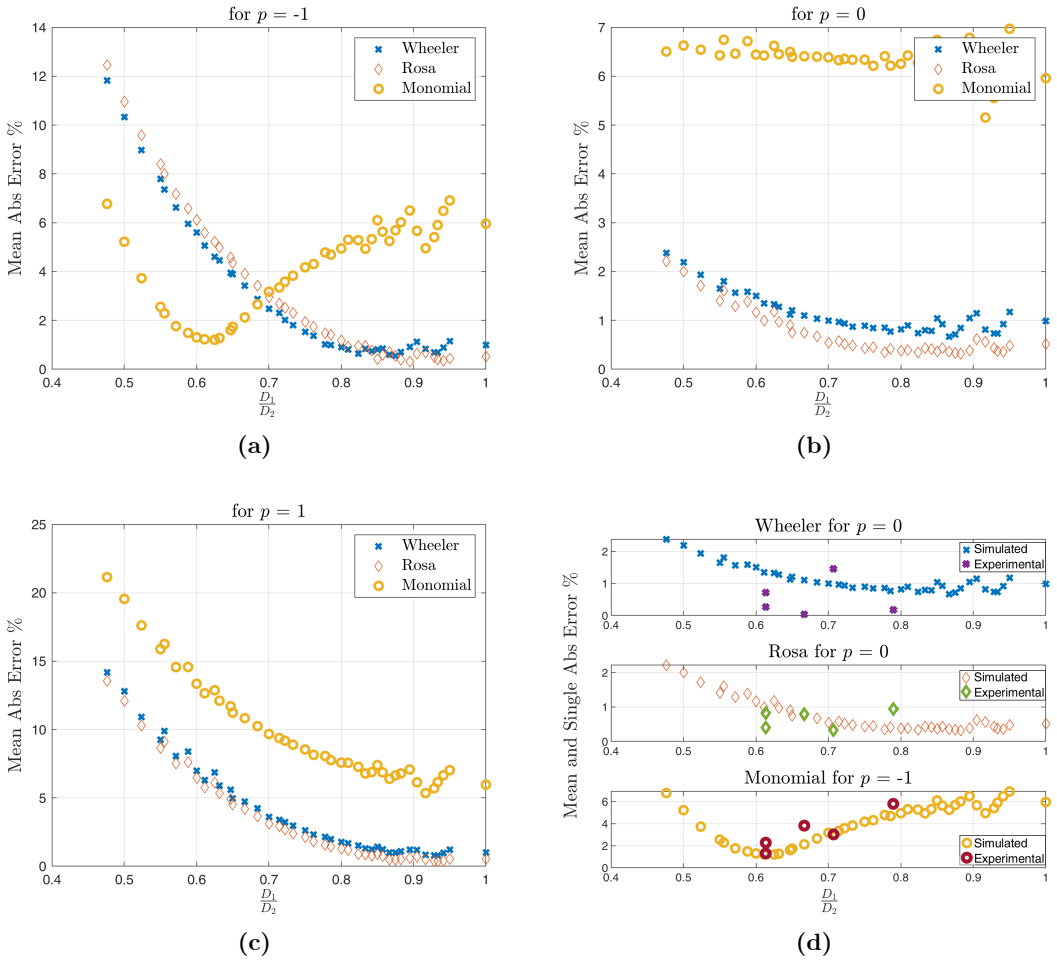
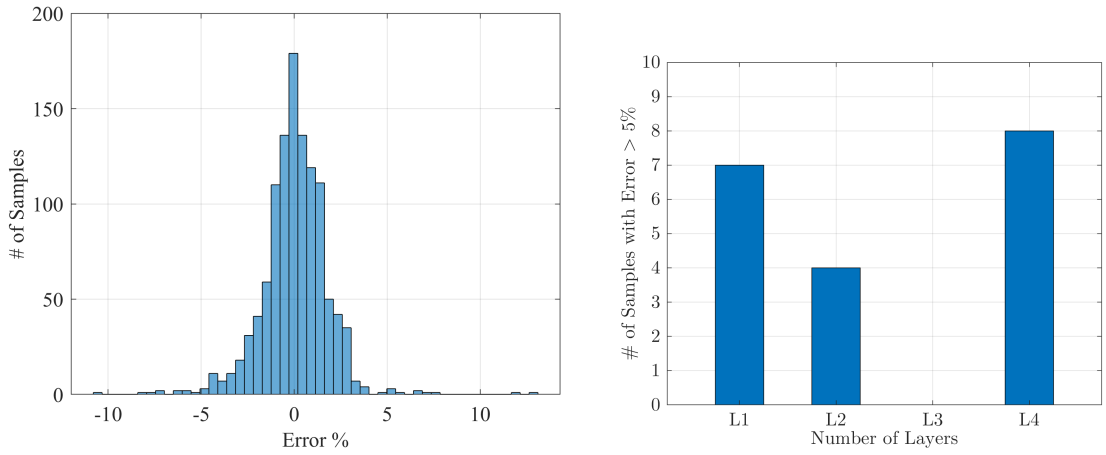


Figure 5 Μέσο απόλυτο σφάλμα % συναρτήσει του D_1/D_2, το οποίο αντιπροσωπεύει την παραμόρφωση του τετραγώνου προς το παραλληλόγραμμο σχήμα. Στο (d) παρουσιάζεται το μέσο απόλυτο σφάλμα % για τα αντίστοιχα στρογγυλοποιημένα p_{opt} κάθε εξίσωσης, με το αντίστοιχο απόλυτο σφάλμα των πειραματικών αποτελεσμάτων.

Με χρήση της εξίσωσης του Wheeler μπορεί να γίνει εκτίμηση της επαγωγής κάθε σπείρας ενός τυλίγματος, δίνοντας καλύτερη εικόνα για την κατανομή της τάσης σε αυτές, και επιτρέποντας καλύτερο σχεδιασμό από πλευράς ηλεκτρικής μόνωσης. Αρχικά υπολογίζεται η αυτεπαγωγή μιας σπείρας i και στη συνέχεια η επαγωγή της i με κάθε άλλη σπείρα j, συνδεδεμένες σε σειρά και με τις γεωμετρικές παραμέτρους που αυτές σχηματίζουν. Στη συνέχεια υπολογίζεται η αμοιβαία επαγωγή των σπειρών i και j αφαιρώντας την αυτεπαγωγή της i, και τέλος γίνεται δυνατός ο υπολογισμός της συνολικής επαγωγής της i σπείρας. Οι εξωτερικές σπείρες εμφανίζουν συστηματικά μεγαλύτερη επαγωγή και αναλόγως με το συνολικό τους πλήθος, οι σπείρες 2, 3 και 4 εμφανίζουν την μεγαλύτερη πτώση τάσης.

Για την επίτευξη μεγαλύτερη επαγωγής, διατηρώντας τις εξωτερικές διαστάσεις ίδιες, είναι δυνατή η σύνδεση πολλών επιπέδων σε σειρά, έτσι ώστε η μαγνητική ροή να έχει την ίδια κατεύθυνση για κάθε επίπεδό. Αυτό διαμορφώνει ένα πολυεπίπεδο τύλιγμα, το οποίο όμως



(a) Σφάλμα % σε 60 ομάδες. **(b)** Σφάλμα $> 5\%$ με βάση τα επίπεδα.

Figure 6 Ιστόγραμμα του σφάλματος % και το πλήθος των δειγμάτων με σφάλμα $> 5\%$.

συνεχίζει να έχει μικρό προφίλ στην κατακόρυφο, στην τάξη των μερικών χιλιοστών. Ωστόσο, ούτε σε αυτήν την περίπτωση, υπάρχουν εξισώσεις για τον εύκολο υπολογισμό της επαγωγής τους.

Μία εκτίμηση μπορεί να γίνει με την αντικατάσταση του πλήθους των σπειρών με το γινόμενο των επιπέδων επί τις σπείρες ανά επίπεδο, και την αντικατάσταση στις τρεις εξισώσεις. Αυτή η προσέγγιση δίνει έγκυρα αποτελέσματα για 2 επίπεδα και σε ορισμένες περιπτώσεις τυλιγμάτων τριών επιπέδων. Προκύπτει η ανάγκη για την ύπαρξη μιας νέας εξίσωσης, με την οποία καθίσταται δυνατό να εκτιμηθεί η επαγωγή τυλιγμάτων περισσότερων επιπέδων και με μεγαλύτερη ακρίβεια.

Χρησιμοποιώντας ένα σύνολο δεδομένων από περίπου 6,000 τυλιγμάτων διαφορετικών διαστάσεων, και με χρήση πολλαπλής γραμμικής παλινδρόμησης, προκύπτει η εξίσωση

$$L_{\mathrm{MN}} = 1.602\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} s^{-0.011} N_T^{1.794} N_L^{1.804} O^{-0.006(N_L-1)}, \qquad (10)$$

όπου N_T το πλήθος των σπειρών ανά επίπεδο, N_L το πλήθος των επιπέδων, και O η απόσταση μεταξύ τους.

Στο Σχήμα 6, παρουσιάζεται το ιστόγραμμα του σφάλματος και το πλήθος των τυλιγμάτων με σφάλμα μεγαλύτερο του 5%. Η μέση τιμή του σφάλματος είναι $\mu = 0\%$ και η διασπορά του $\sigma = 1.77\%$, ενώ το μέσο απόλυτο σφάλμα 1.24%. Η ακρίβεια της εξίσωσης επιβεβαιώνεται και με πειραματικές μετρήσεις, ακόμα και για τυλίγματα με διαστάσεις εκτός του αρχικού συνόλου δεδομένων, με σφάλμα μικρότερο του 6.1%.

Η εύρεση μιας εξίσωσης μπορεί να συμβάλει και στη βελτιστοποίηση του σχεδιασμού, όπου για δεδομένες εξωτερικές διαστάσεις μπορεί να βρεθεί η μέγιστη επαγωγή, ή για δεδομένη επαγωγή μπορούν να βρεθούν οι ελάχιστες εξωτερικές πλευρές. Αξίζει να σημειωθεί πως το

πρόβλημα βελτιστοποίησης προς επίλυση είναι μη κυρτό, οπότε απαιτούνται τεχνικές αντιμετώπισης της εμφάνισης τοπικών ακρότατων, όπως η επανάληψη του αλγορίθμου για διαφορετικές αρχικές συνθήκες.

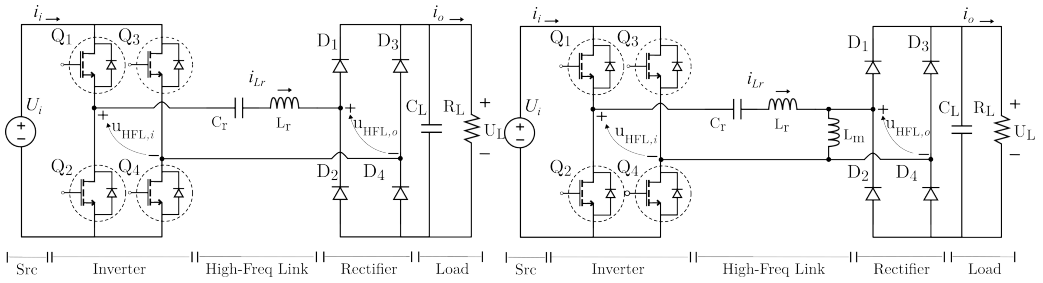
Στο πλαίσιο της διατριβής πραγματοποιείται σύγκριση των τροποποιημένων και των νέων εξισώσεων, όσον αφορά την ακρίβεια των εκτιμήσεων για τυλίγματα ενός και πολλαπλών επιπέδων. Για τα τυλίγματα ενός επιπέδου η τροποποιημένη εξίσωση του Rosa δίνει τα καλύτερα αποτελέσματα, με μέσο απόλυτο σφάλμα 0.65%, ενώ του Wheeler με 1.05%. Η νέα μονώνυμη εξίσωση δίνει τα τρίτα καλύτερα αποτελέσματα με μέσο απόλυτο σφάλμα 2.01%.

Όσον αφορά τα τυλίγματα πολλαπλών επιπέδων, και οι τρεις τροποποιημένες εξισώσεις (7) - (9), με $N = N_T N_L$, έχουν μέσο απόλυτο σφάλμα μεγαλύτερο του 7.5%, και μη μηδενική μέση τιμή. Με τη νέα μονώνυμη εξίσωση (10) επιτυγχάνεται μέσο απόλυτο σφάλμα μικρότερο του 1.5% με σχεδόν μηδενική μέση τιμή. Συνεπώς, για τυλίγματα ενός επιπέδου προτείνεται η χρήση των τροποποιημένων εξισώσεων των Rosa και Wheeler, ενώ για ανώ του ενός επιπέδου προτείνεται η χρήση της νέας μονώνυμης εξίσωσης.

Τέλος, παρουσιάζεται η επίδραση της εισαγωγής πυρήνα τύπου φερρίτη, συνήθως σχήματος UI και EI. Γίνεται σύντομη ανασκόπηση της εκτίμησης των απωλειών και της μαγνητικής ροής εντός του πυρήνα. Ειδικά για την περίπτωση του πυρήνα EI βρίσκεται το ισοδύναμο μαγνητικό κύκλωμα, η μαγνητική αντίσταση και η ροή για τις περιπτώσεις πυρήνα με και χωρίς διάκενο.

Μετατροπείς Συντονισμού

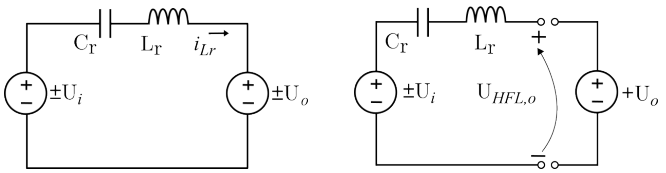
Με τη χρήση των υψίσυχνων μετατροπέων συντονισμού παρέχεται η δυνατότητα μείωσης, ακόμα και να εξάλειψης, των διακοπτικών απωλειών των ημιαγωγικών διακοπτών, γεγονός που επιτρέπει την αύξηση της απόδοσης του μετατροπέα για σταθερή διακοπτική συχνότητα, ή εναλλακτικά αύξηση της συχνότητας και μείωση του όγκου του μετατροπέα για σταθερές απώλειες. Οι μετατροπείς αυτοί χρησιμοποιούν ένα κύκλωμα συντονισμού, το οποίο αποτελείται από ένα δίκτυο τουλάχιστον ενός επαγωγού και ενός πυκνωτή και ονομάζεται δίκτυο ζεύξης υψηλής συχνότητας (High Frequency Link - HFL). Οι πιο διαδεδομένοι μετατροπείς συντονισμού είναι ο σειράς και ο LLC, όπως παρουσιάζονται στο Σχήμα 7, με συχνότητα συντονισμού $f_0 = 1/(2\pi\sqrt{L_r C_r})$.



(a) Συντονισμού-σειράς (ΣΣ) **(b)** LLC

Figure 7 Μετατροπείς συντονισμού.

Ο μετατροπέας συντονισμού-σειράς (ΣΣ) αποτελεί μία από τις πιο απλές και διαδεδομένες μορφές, ειδικά στην περίπτωση που δεν χρειάζεται ηλεκτρική απομόνωση μεταξύ εισόδου-εξόδου. Στην περίπτωση που υπάρχει μετασχηματιστής, εάν η αυτεπαγωγή μαγνήτισης L_m είναι τουλάχιστον δύο τάξεις μεγέθους μεγαλύτερη της σκέδασης L_r, η μαγνήτιση μπορεί να αμεληθεί και ο μετατροπέας μπορεί να αναλυθεί όπως ο συντονισμού-σειράς. Να σημειωθεί ότι όταν η μαγνήτιση μπορεί να αμεληθεί, το κέρδος τάσης U_o/U_i είναι ίσο ή μικρότερο του ένα, με $U_i = U_o$ στον συντονισμό.



(a) CCM **(b)** DCM

Figure 8 Απλοποιημένο μοντέλο μετατροπέα συντονισμού-σειράς.

Στο Σχήμα 8 παρουσιάζονται τα δύο απλοποιημένα μοντέλα του μετατροπέα ΣΣ, για την περίπτωση συνεχούς αγωγής ρεύματος (CCM) στο πηνίο συντονισμού L_r, και για την περίπτωση της ασυνεχούς αγωγής (DCM). Η λειτουργία του μετατροπέα εξαρτάται από τη διακοπτική συχνότητα (f_s) των διακοπτών: για $f_s > f_0$ ο μετατροπέας λειτουργεί στην επαγωγική περιοχή, για $f_s = f_0$ στον συντονισμό, ενώ για $f_s < f_0$ στη χωρητική περιοχή. Μόνο στην τελευταία μπορεί το ρεύμα του πηνίου να μηδενιστεί για κάποιο (μη-στιγμιαίο) χρονικό διάστημα. Η λύση της διαφορικής εξίσωσης

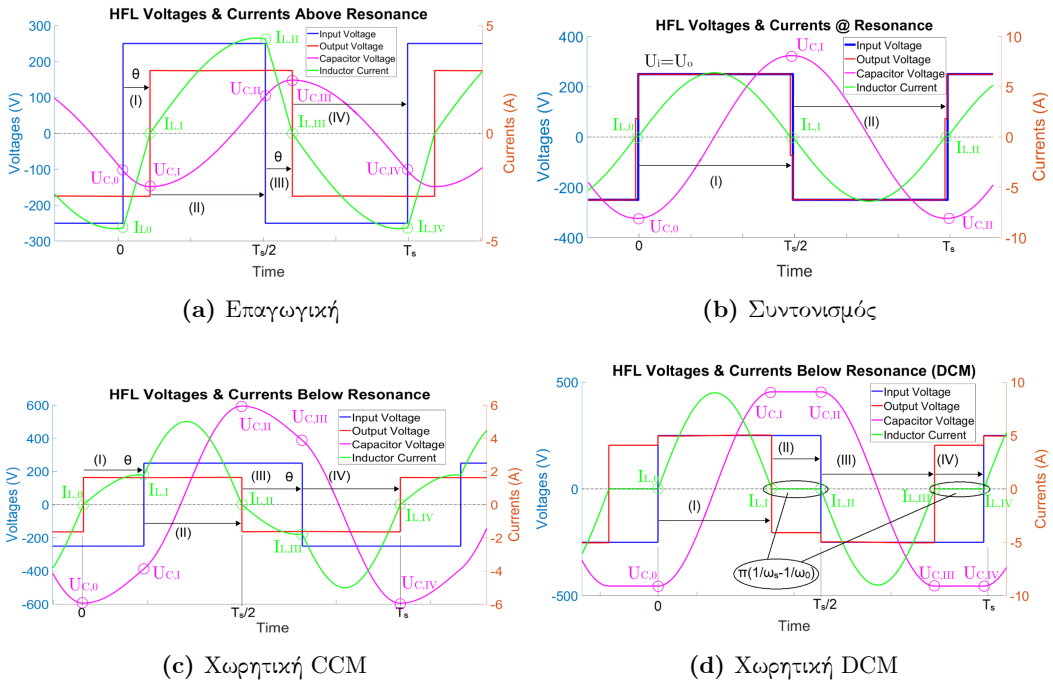
$$U_i - U_o = U_{L_r} + U_{C_r} = L_r \frac{\mathrm{d}}{\mathrm{d}t} i_{L_r} + \frac{1}{C} \int i_{L_r} \mathrm{d}t. \tag{11}$$

οδηγεί στον καθορισμό των αναλυτικών εξισώσεων που περιγράφουν την τάση και το ρεύμα για κάθε σημείο του μετατροπέα. Η εύρεση των αρχικών συνθηκών γίνεται μέσω της συνθήκης συνέχειας για το ρεύμα και για την τάση και μέσω του ισοζυγίου ισχύος.

Στο Σχήμα 9 παρουσιάζονται οι κυματομορφές τάσης και ρεύματος του HFL για κάθε περιοχή λειτουργίας. Στην επαγωγική λειτουργία επιτυγχάνεται μετάβαση των διακοπτών υπό μηδενική τάση κατά την έναυση και μετάβαση με απώλειες κατά τη σβέση. Στη συχνότητα συντονισμού και στη χωρητική ασυνεχή λειτουργία επιτυγχάνεται μετάβαση υπό μηδενικό ρεύμα τόσο κατά την σβέση όσο και κατά την έναυση. Στη χωρητική λειτουργία συνεχούς αγωγής, οι διακόπτες σβήνουν υπό μηδενική τάση ενώ η έναυσή τους παρουσιάζει απώλειες.

Το όριο λειτουργίας μεταξύ των περιοχών CCM και DCM, εξαρτάται από την χαρακτηριστική εμπέδηση του HFL Z_0, το φορτίο R_L, και τον λόγο συχνότητας συντονισμού και διακοπτικής, και δίνεται από

$$R_{L,BD} = Z_0 \frac{\pi}{4} \frac{\omega_0}{\omega_s} \Rightarrow \begin{cases} R_L > R_{L,BD} \Rightarrow \text{DCM} \\ R_L < R_{L,BD} \Rightarrow \text{CCM} \end{cases} \tag{12}$$



(a) Επαγωγική (b) Συντονισμός

(c) Χωρητική CCM (d) Χωρητική DCM

Figure 9 Κυματομορφές LC-σειράς για κάθε περιοχή λειτουργίας.

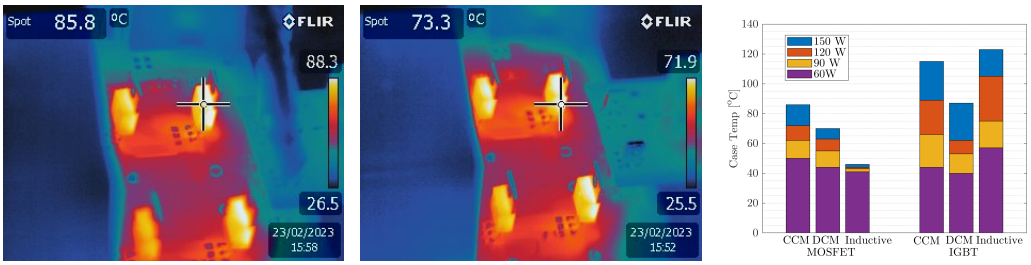
συναρτήσει του φορτίου, και από

$$f_{s,BD} = f_0 \frac{\pi}{4} \frac{Z_0}{R_L} \Rightarrow \begin{cases} f_s > f_{s,BD} \Rightarrow \text{DCM} \\ f_s < f_{s,BD} \Rightarrow \text{CCM} \end{cases} \tag{13}$$

συναρτήσει της συχνότητας.

Το αντικείμενο της διατριβής περιλαμβάνει, επίσης, την πειραματική επιβεβαίωση της λειτουργίας του μετατροπέα. Παρατηρείται πειραματικά πως η λειτουργία σε CCM είναι λιγότερο αποδοτική από τη λειτουργία σε DCM σε κάθε περίπτωση, όπως παρουσιάζεται στο Σχήμα 10. Όσον αφορά τα MOSFETs, η αποδοτικότερη λειτουργία τους παρατηρείται στην επαγωγική περιοχή και μάλιστα με πολύ μικρή αύξηση των απωλειών πάνω στα στοιχεία σε σχέση με την αύξηση της παρεχόμενης ισχύος. Αυτό οφείλεται στην έναυση υπό μηδενική τάση και την εξάλειψη των απωλειών του παρασιτικού πυκνωτή εξόδου. Για τα IGBTs, η βέλτιστη λειτουργία παρατηρείται στη DCM περιοχή, καθώς η σβέση υπό μηδενικό ρεύμα εξαλείφει τις απώλειες από το ρεύμα ουράς.

Παρόμοια ανάλυση πραγματοποιήθηκε για τον μετατροπέα LLC, η ανάλυση του οποίου περιλαμβάνει την επαγωγή μαγνήτισης του μετασχηματιστή. Ειδικά στην περίπτωση που η τιμή της είναι συγκρίσιμη με την αυτεπαγωγή σκέδασης, μπορεί να πετύχει κέρδος τάσης αρκετά μεγαλύτερο της μονάδας. Όπως και στην περίπτωση του ΣΣ, το κέρδος είναι ίσο με την μονάδα στη συχνότητα συντονισμού. Δυνάται, ωστόσο, να υπάρχει και μία επιπλέον συχνότητα μοναδιαίου κέρδους της τάσης, η τιμή της οποίας είναι αρκετά μικρότερη του συντονισμού,

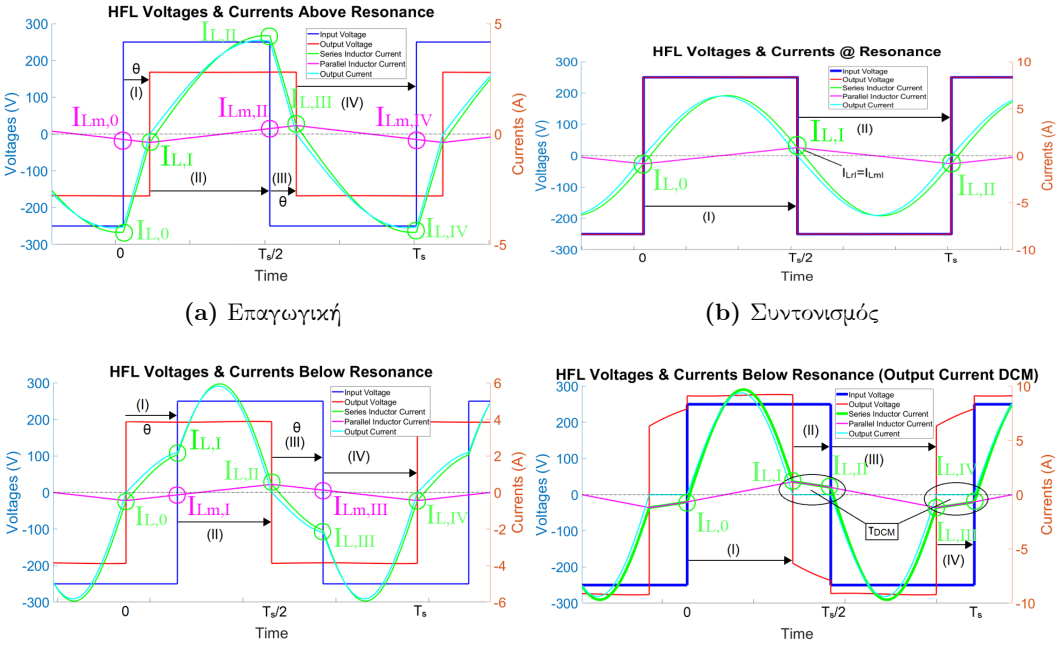


(a) CCM **(b)** DCM **(c)** MOS vs IGBT

Figure 10 Πειραματικά αποτελέσματα μετατροπέα ΣΣ.

εξαρτάται από την τιμή των παραμέτρων του κυκλώματος συντονισμού και του φορτίου και δεν αναλύεται στα πλαίσια της διατριβής.

Στο Σχήμα 11 παρουσιάζονται οι κυματομορφές τάσης και ρεύματος του HFL για κάθε περιοχή λειτουργίας του LLC. Να σημειωθεί πως, καθώς ο καθορισμός των αρχικών συνθηκών παρουσιάζει σημαντικές δυσκολίες για ορισμένες περιοχές, προτείνονται προσεγγίσεις για την ακριβή εκτίμησή τους. Στην επαγωγική λειτουργία, επιτυγχάνεται έναυση των διακοπτών υπό μηδενική τάση, αλλά η μετάβασή τους στην αποκοπή προκύπτει απότομα. Όμοια είναι και η συμπεριφορά τους στη συχνότητα συντονισμού, όπου λόγω του ρεύματος μαγνήτισης δεν επιτυγχάνεται μετάβαση υπό μηδενικό ρεύμα, όπως στον μετατροπέα ΣΣ.



(a) Επαγωγική **(b)** Συντονισμός

(c) CCM **(d)** DCM

Figure 11 Κυματομορφές LLC για κάθε περιοχή λειτουργίας.

Η συμπεριφορά των διακοπτών κατά την λειτουργία με διακοπτική συχνότητα μικρότερη αυτής του συντονισμού είναι αρκετά διαφορετική από αυτή της περίπτωσης του μετατροπέα ΣΣ.

Οι περιοχές CCM και DCM διακρίνονται από τη συνεχή ή ασυνεχή αγωγή της ανορθωτικής γέφυρας και όχι του κυκλώματος συντονισμού. Ορίζονται τρεις περιοχές λειτουργίας, η οποίες καθορίζονται από την παρεχόμενη ισχύ και προκύπτουν οι μεταβάσεις των διακοπτών, καθώς και οι συνοριακές περιοχές μεταξύ τους.

Στο πλαίσιο της διατριβής, γίνεται παρουσίαση των πιθανών τύπων πυκνωτών για το κύκλωμα συντονισμού και πραγματοποιείται μια συγκριτική μελέτη. Τονίζεται η δυσκολία της χρήσης εμπορικών επαγωγών, για τη συγκεκριμένη εφαρμογή, καθώς και τα πλεονεκτήματα και οι περιορισμοί των επίπεδων τυλιγμάτων. Τέλος, πραγματοποιείται μια συγκριτική διερεύνηση της παρασιτικής χωρητικότητας εξόδου των ημιαγωγικών στοιχείων, ως συνάρτηση της συσκευασίας τους και του τύπου τους.

Συμπεράσματα

Η διατριβή στοχεύει να συμβάλει στον κλάδο των μετατροπέων συντονισμού, όσον αφορά τον σχεδιασμό των ΠΤΚ και των μαγνητικών στοιχείων, εξετάζοντας παράλληλα τη λειτουργία και την κατασκευή των μετατροπέων ΣΣ και LLC. Οι πρακτικές καλού σχεδιασμού που συγκεντρώθηκαν από τη βιβλιογραφία και παρατίθενται δύναται να μειώσουν σημαντικά την αλληλεπίδραση των σημάτων εντός της πλακέτας, αλλά και της ηλεκτρομαγνητικής παρεμβολής, ενώ οδηγούν σε κυματομορφές με μικρότερο αρμονικό περιεχόμενο και διευκολύνουν τη μείωση των απωλειών των διακοπτικών στοιχείων. Όσον αφορά το σχεδιασμό των παραλληλόγραμμων επίπεδων επαγωγών, ενός και πολλών επιπέδων, παρατίθενται τροποποιημένες και νέες εξισώσεις, οι οποίες μπορούν να εκτιμήσουν με μεγάλη ακρίβεια την επαγωγή, με μέσο απόλυτο σφάλμα μικρότερο του 1.5% σε κάθε περίπτωση. Τέλος, αναπτύσσονται και επιβεβαιώνονται, σε επίπεδο προσομοίωσης και εργαστηριακών πειραμάτων, οι αναλυτικές λύσεις που δίνουν τις κυμαμορφές της τάσης και του ρεύματος για κάθε κόμβο του μετατροπέα ΣΣ, θέτοντας τις βάσεις για την εκτίμηση των απωλειών και της εύρεσης βέλτιστης λειτουργίας συναρτήσει του τύπου των διακοπτικών στοιχείων. Παρόμοια ανάλυση και επιβεβαίωση, σε επίπεδο προσομοίωσης, πραγματοποιείται για τον μετατροπέα LLC, όπου λαμβάνονται οι κατάλληλες προσεγγίσεις στις περιπτώσεις όπου η αναλυτική λύση δεν είναι εφικτή ώστε η εκτίμηση των αρχικών τιμών να ακριβής. Σε αμφότερες τις περιπτώσεις δίνεται ιδιαίτερη έμφαση στην εύρεση των συνοριακών περιοχών συνεχούς και ασυνεχούς αγωγής, για διακοπτική συχνότητα μικρότερη από αυτή του συντονισμού.

Λέξεις Κλειδιά: Βελτιστοποίηση Σχεδιασμού ΠΤΚ (PCB), Εκτίμηση Επαγωγής, Εκτίμηση Απωλειών, Μετατροπέας Συντονισμού

Summary

This PhD thesis contributes to the analysis and design of high-frequency resonant converters, with emphasis on the design of the magnetic components. The contributions lie on the modifications of existing equations and the introduction of new ones to for accurately estimating the inductance of rectangle-shaped single-layer and multilayer planar windings, enabling fast design and optimization processes. Furthermore, this thesis provides closed-form solutions of the differential equations that describe all the operation regions of the LC and LLC resonant converters, providing insight to their behavior and setting the criteria for the selection of passive and active components. A comparison between the regions is carried out and the boundary conditions between each operating region are defined. The structure is as follows:

First, good design practices are presented for high-frequency power electronics printed circuit boards (PCBs), whose design difficulty lies in the fact that they include high-power signals, as well as analog and digital control and measurement signals. The difference on the power level and frequency spectrum can lead to crosstalk between signals inside the board, and to electromagnetic interference between the converter and other electronics devices. The design practices appear scattered in the literature (in books and scientific articles), but also in interviews and presentations of experienced designers of high-frequency boards and power electronics.

The topic of planar windings (PWs) is discussed. Their inductance is affected by the geometrical shape of the winding, and several equations for regular-polygons have been proposed in the literature. However, the use of rectangle-shaped windings provides an additional degree of freedom to the designer, while the exact knowledge of the inductance plays a serious role in calculating the characteristic values of the resonant converter. Modifications to three well-established equations, namely Wheeler, Rosa, and the Monomial, are developed to calculate the inductance of single-layer rectangle-shaped planar windings, without affecting the estimation accuracy. The mean absolute error is less than 1% for the first two equations and less than 5% for the third. In addition, an algorithm for estimating the inductance per turn is presented and validated, providing less than 7% error in the worst case.

A new monomial-like equation for calculating the inductance of multilayer rectangle-shaped inductors is proposed, which retains the high estimation accuracy of the equations for single-level windings. The mean error $\mu = 0\%$, the standard deviation $\sigma = 1.77\%$, and the mean absolute error is less than 1.5%. Moreover, a comparative study is carried out on the

accuracy of the various equations in single and multi-level windings, highlighting the most accurate equation for each case. For single-layer PWs, modified Rosa and Wheeler provide a mean absolute error of less than 1.1% and the new proposed Monomial equation less than 2.1%. In the case of multilayer PWs, all modified equations provide a mean absolute error greater than 7.5%, while the new proposed monomial equation has an error of less than 1.5%. In addition, a brief analysis is made of the effect the insertion of the ferrite core has on the inductance of a planar winding, calculating the magnetic flux of an EI core with and without an air-gap.

The common denominator of the aforementioned topics is the resonant converters. Analytical models are presented in the time domain for series-resonant and LLC converters, for all operating regions (inductive, resonant, capacitive), and the initial conditions are deduced. Particular emphasis is given to the boundary conditions of the regions, and especially on the operation between continuous and discontinuous current mode. The solutions yield the values of voltage and current for every node of the converter, as well as the conditions necessary to achieve soft-switching under zero-voltage or zero-current.

Furthermore, a comparison between MOSFET and IGBT devices is carried out for the series-resonant converter, highlighting the most efficient region for each device respectively. The conduction and switching losses models are presented, enabling the estimation of the converter's efficiency under any condition and operation. Based on the analytical solutions and waveforms, a passive and active component selection procedure is proposed, which includes the parasitic components of semiconductor switches.

Keywords: PCB Layout Optimization, Resonant Converter, LLC Converter, Planar Windings, Inductance Estimation, Semiconductor Losses Estimation

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Chapter 1

Introduction

1.1 Decarbonization and Electrical Power

Fossil fuels have enabled one of the biggest revolutions in human history, acting as a source of energy for external and internal combustion engines (ICE). The transition from human or animal-powered, to hydrocarbon-powered machines allowed a rapid development of all productive and economic sectors (industrial, transportation, construction, commercial, etc.). The developments of the last half century led to a technological bloom that has changed everyday life, from education and work, to communication and politics.

However, to a large degree, the irrational and almost unregulated extraction and use of fossil fuels, led to an also rapid shift in climate, what is now called "climate change". This change is exacerbated by the poor management of electronic raw materials and waste and the increased electricity needs for hardware to support the digital transition.

The reduction and eventually the elimination of greenhouse gases (carbon dioxide (CO_2), hydro/chlorofluorocarbons (H/CFCs), and nitrous oxides (NOx)), which are largely responsible for the climate change, seems to be a high priority for many counties, including all European Union (EU) states, north America states and China. Especially for the EU, the European Green Deal [1] aims to reduce greenhouse gas emissions by at least 55% by the end of the current decade, and totally eliminate them by 2050, a very optimistic plan.

The electrification of all sectors is presented as a partial solution to the climate change threat. The production of electrical energy in central power plants, with optimized cycles, can help to reduce the emissions in general, especially when the produced electrical energy replaces energy which traditionally comes from fossil fuels, like the transportation sector. Also, the electrical energy can be produced locally from renewable energy sources (RES), as a part of a decentralized network or in large photovoltaic (PV) and wind farms, where the emissions during operation are almost zero. The utilization of RES also comes with the added benefit of partial or total power autonomy in the level of a state, a region or a municipality.

However, the ecological and economical cost of a transition like this should be considered, as it would require large changes on the power grid, the construction of new electric motors, PVs, wind turbines, batteries, and power converters. Especially when it comes to traditional electric batteries, the mining of the necessary materials (like lithium and nickel) is a big concern [2]. The emitted CO_2 during lithium battery production for an electric vehicle (EV) can range from 2,400 to 16,000 kg [3], while the average new passenger vehicle emits 1,000 kg of CO_2 every 7,000 to 9,000 km (110g to 140g of CO_2 per km) [4]. Therefore, with the current technology, the life-cycle of an EV should be large enough in order to offset the CO_2 emitted for the construction of its battery, with the nearly-zero emissions during its operation.

Energy storage can enhance the abilities of an all-electrical power society, by saving and providing power when the demand is low and high, respectively. This simple method can flatten the consumption "duck curve" [5], and overall reduce the production cost of electricity. In Greece pumped storage systems for hydroelectric power plants are a relative inexpensive and easy method to store energy, which can be better exploited as PV power increases [6]. Current plans include 5 new storage plants of total 1.5 GW power capability [7], which is close to the optimal for a 60% RES penetration [8, 9]. Increasing the penetration up to 80%, and including pumped storage and lithium battery storage systems, the optimal has been found to be up to 3.5 GW, and up to 15-20 GWh [9].

Autonomous grids and microgrids can also greatly benefit from energy storage, especially in Greece, where more than 30 non-interconnected power systems exist [10]. As an example, the island of Tilos, which is not connected to the mainland grid, has deployed a hybrid energy production system. This includes an 800 kW wind-turbine and an 160 kW PV park, with a 2.4 MWh battery energy storage [11]. A similar method is used in the Azores island complex, where a 50% RES penetration is achieved, with a 15 MWh energy storage [12].

Alternatives to store energy, which are less material-intense, like production of hydrogen, which is then used in a fuel cell or an hydrogen-based ICE are examined [13, 14, 15]. When hydrogen is produced from the excess energy of RES, it is called "green" and has low to zero CO_2 emissions, during its production and consumption.

Hydrogen is a good candidate for facilitating the electrification of ships, airplanes and heavy vehicles, where the power density of batteries is not high enough. Hydrogen can also be transported via the existent natural gas grid, which in Greece is hydrogen-ready and can be utilized with some minor modifications [16, 17]. However, they are not considered mature technologies for mass production that can totally replace the conventional means, like diesel ICEs, and further research is required.

Geopolitical conflicts are also a factor that can accelerate or decelerate the electrification process. On the one hand, countries with access to cheap fossil-fuel, put pressure on the relaxation of the commitments at the transnational level. On the other hand, conflicts in the European region has forced EU to generate plans for a more rapid transition [18]. Moreover,

raw materials and minerals, which are necessary for any electrification process, are another point of armed or diplomatic conflicts, like the restrictions China forced in gallium and germanium export, in response to chip export restrictions from the EU [19, 20]. Attempts to mitigate the continuous exploitation of African countries is also a factor that will test the feasibility of rapid electrification [21].

In any case, electrification requires converters of high efficiency, low volume and weight, and capable of monitoring and controlling the power level and flow. At the same time, power converters should comply with the several EU standards of safety and electromagnetic interference. Traditional 50 Hz power transformers are optimized for more than a century, and provide high reliability, high efficiency figures, and relatively low cost. However, they are bulky and heavy equipment, incapable of monitoring and controlling the power flow.

The research on solid-state technology has enabled the development of high-power high-frequency (HP-HF) converters, capable of monitoring and transmitting power in a controllable way, while also offering galvanic isolation between their sides. As switching frequency increases, the values of the necessary capacitors and inductors decreases, along with their volume and mass, reducing the need for copper, aluminium and core materials. The same is true for the high-frequency medium- or high-voltage transformers (DCX), when isolation is required. This leads to an overall more compact and lighter power converter.

The benefits that are introduced by HP-HF converters does not only make them suitable candidates for replacing the traditional low-frequency equipment, but has motivated engineers and designers to re-imagine the power transmission and distribution grid. Typically, energy harvested from RES passes through a rectifying stage and enters the grid via an inverter (DC-to-AC converter). With the ability of HP-HF converters to step-up and down the voltage level, DC power grids become of particular interest, which is enhanced by the installation of battery energy storage (BES) systems. Furthermore, DC power-intense loads, such as data centers and DC charging stations, start to become an important part of the total power consumption.

1.2 Resonant Converter

The transition from low-frequency to high-frequency systems is restricted by three main factors: (i) efficiency, (ii) reliability, and (iii) economic cost. Resonant converters can potentially provide better performance and be more reliable compared to their hard-switching low- or high-frequency counterparts. They consists of at least one active (full or half) bridge and a resonant circuit, capable of operating near the resonant frequency and enabling the switching devices to reduce and even eliminate the switching losses. Thus, the efficiency of a DC/AC/DC, AC/AC [22], and DC/AC converter can increase from the range of 90-95% to 97% or more.

The switching elements of resonant converters are subjected to less thermal stress due to lower losses and less non-active current, which can increase their life expectancy. Furthermore, resonant converters produce waveforms closer to sinusoidal, which means less electromagnetic interference and greater compatibility between devices. As for the economic cost, converters are difficult to compete with passive equipment, but as the technology matures and economies of scale are developed, a counterbalance is expected.

However, it should be highlighted that if not properly designed (layout and component selection), HP-HF converters can be less efficient or even unreliable, compared to conventional hard-switching counterparts. Resonant phenomena can produce high-voltage oscillations across the semiconductor switches, increasing their stress and even lead to their destruction. As it is discussed in Chapter 4, the steady-state voltage and current can be larger compared to other non-resonant topologies, for certain regions of operation. Nevertheless, it should be noted that direct comparisons are not always meaningful, as different topologies have separate properties that may or may not be suitable for a specific application. For example, the LC-series converter has a voltage gain less or equal to one, and can auto-regulate the output voltage when the switching frequency is equal to the resonant or the converter operates in the discontinuous-current region. These features do not necessarily exist for non-resonant converters.

The most common topologies of the resonant LC, LLC and CLLC converters are presented in Fig. 1.1. These topologies can be used as a conventional power converter, feeding a load with energy, or as a DC transformer (DCX), which galvanically isolates its ports, steps up or down the voltage via a HF transformer, controls the power level and even its direction.

If only an L is utilized to form the high-frequency link (HFL) topology (L-HFL) is non-resonant, but under specific conditions it can turn-on the primary-bridge transistors pair with zero losses. During the dead-time and as the current cannot change instantly, the current passes through the anti-parallel diodes, clamping the voltage to approximately zero, and thus no losses are produced during turn-on. This is a simple example of lossless switching, and further types of zero-voltage and zero-current transitions are discussed in Appendix A.

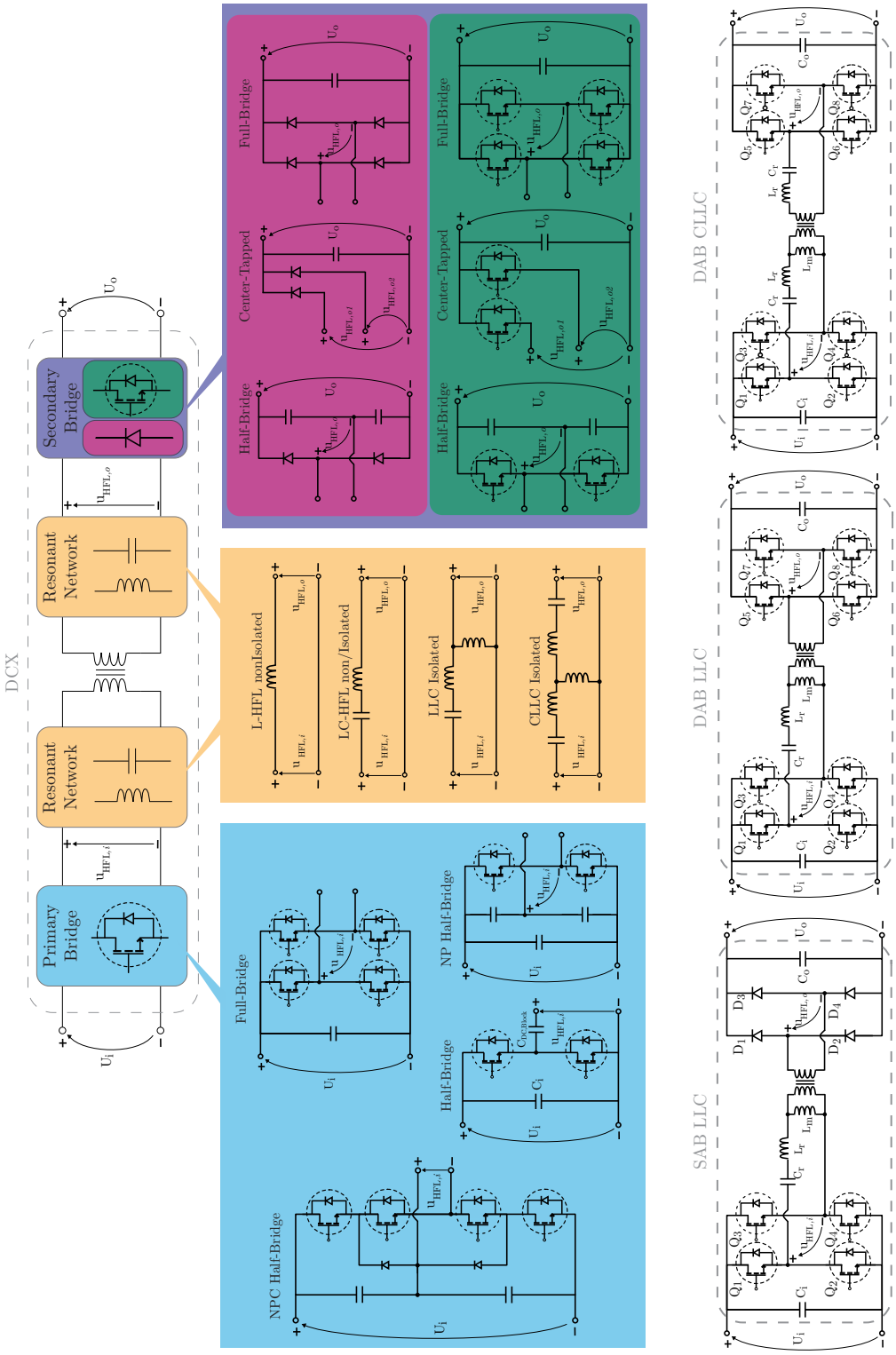


Figure 1.1 DCX converter topologies: the primary bridge consists of power transistors which control the power flow, the resonant network (or high-frequency link) consists of an inductor and capacitor network, and the secondary bridge which can contain diodes or transistors, depending on the direction of the power flow. The building blocks that are presented are only indicative, several more are available depending on the application.

The LC series resonant topology is the most basic resonant HFL, which consists of an inductor and a capacitor. This can represent two distinct physical components, or a capacitor and a transformer, which has a much larger magnetizing inductance (L_m) compared to its leakage (L_r), as it is discussed in Chapter 4. When L_m is greater or nearly equal to L_r, the HFL is modeled as an LLC circuit.

The primary bridge necessarily consists of active components, and can be a half-bridge, full-bridge, neutral-point, or multi-level topology. Other topologies, like the T-type LLC have been proposed [23], but an exhaustive presentation is beyond the scope of this study. The same is true for the secondary bridge, which can consist of diodes when unidirectional power flow is enough, or active transistors when bidirectional power flow is required. When both bridges are active, CLLC HFL may be preferable due to its symmetry.

The operation of a resonant converters is far from trivial, especially when the parasitic elements of the components and the traces are considered. As new topologies are developed and get more complex, trying to be more efficient and reliable, parallel and series branches are added to handle larger levels of voltage and current, a systematic and intuitive understanding of the basic building blocks is of paramount importance. In this effort, time- and frequency-domain analyses can be useful, to better understand the behavior of the voltages and currents, the ZVS/ZCS conditions, as well as the HFL response.

1.2.1 Applications

Ultimately, any power converter is as useful as the applications it can handle. Resonant converters are currently dominant in power supply (PS) applications, from hundreds of watts up to the kW range, like in computer and television PS. Studies over the last decade have shown that they are good candidates for applications that require higher power levels, like EV charging, and data center PS units. They are, also, considered as the core of any solid-state transformer, incorporating high-power medium- and low-voltage handling capabilities, power flow control, and high-efficiency. Other applications include the generation of high-voltage, utilizing an isolated LLC resonant converter with voltage multiplier rectifier at the output of the transformer. A simplified steady-state equivalent circuit is proposed, along with the power factor, electrical stress and possible voltage gain in [24].

For several applications, the utilization of planar magnetics is beneficial. Planar inductors and transformers are low profile components, and easy to construct and reproduce in large quantities. Additionally, they offer precise inductance values, repeatable in mass production, properties that are vital for resonant converters. The integration of planar magnetics in power converters is a very interesting topic, with hundreds of recent publications, aiming for designs that further decrease the cost and increase their efficiency. An indicative example is presented in [25, 26] for data-center and telecommunication applications.

1.2.1.1 EV Charging

Electrification of the transportation sector requires chargers for the EV batteries, which can respond to the two fundamental scenarios: slow charging during a long period of time (4 to 8 hours) and fast charging to enable long distance travel (15 to 45 minutes or even less). For the first scenario, an on-board charger (OBC) of 10 kW is enough, and there are already available LLC converters, capable for constant-current constant-voltage charging, like in [27]. However, there is still a large margin for power-level and efficiency improvements, regarding the bridges and their modulation, as it is presented in [28], where a variable-frequency phase-shift method is compared to other state-of-the-art modulations. A comprehensive review of two-stage resonant converters for EV charging is presented in [29], for various HFLs and modulation schemes.

Nevertheless, fast DC-DC chargers, which can supply up to 350 kW [30], can greatly benefit from resonant converters. The high-frequency transformer can reduce the massive grid-side transformer, and the higher efficiency can reduce the required heatsinks. While the community seems to be interested in this emerging application [31, 32], it is not a mature technology yet. This does not indicate any inability of resonant converter to handle hundreds of kW, as it is presented in [33], but there are many steps to be taken in order to produce reliable prototypes.

Another reason the topologies of Fig. 1.1 are preferable, is their ability to reverse the flow of the power when the secondary bridge consists of active components. Many activities can be found in the area of bidirectional power flow between EVs and the power grid. Numerous vehicles, from French, Japanese, Korean, and USA manufacturers, have been modified to enable vehicle-to-grid (V2G) or vehicle-to-anything (V2X) services, and have been field tested [34]. Although the details of a fair pricing and responsibility scheme for the battery wear caused be the additional charging-discharging cycles are under negotiation, V2X seems to be a promising service, capable of supporting the grid both in a local and central level.

1.2.1.2 Marine and Aviation

High-power high-frequency converters can stand as pivotal components to ship and harbor electrification, as well as the emergence of more electric aircrafts. Modern propulsion and auxiliary systems, shore-to-ship power (cold ironing) [35], and air-propellers can greatly benefit from these converters. In the context of ship electrification, resonant converters can seamlessly integrate with the power distribution networks [36] required for electric propulsion systems, enabling high-frequency operation to efficiently manage power flow. This enables enhanced maneuverability, reduced emissions, and improved fuel efficiency. Similarly, within the realm of more electric aircraft, resonant converters offer the potential to optimize the electrical power architecture by providing high-frequency power conversion, reducing weight, and improving the overall system efficiency [37, 38, 39]. As resonant converters continue to

evolve, their versatile application in ship electrification and more electric aircraft can usher to a paradigm of sustainable and efficient transportation systems.

A major challenge is thermal management of power converters in high-altitude or in space environment. Thermal dissipation via natural convection is greatly reduced due to the density of the air, and special consideration are required, as it is discussed in [40]. Another issue, especially critical for aircrafts, is the power density of the energy storage unit. Regardless of the power converters utilized, conventional lithium batteries create a bottleneck, which researchers try to overcome, considering hydrogen or solid-state batteries [41].

1.2.1.3 Data Centers

Another sector that can greatly benefit from the low-volume and high-efficiency and scalability of HP-HF converters is data centers [42, 43]. Through their ability to reduce losses, resonant converters address the critical energy consumption concerns of data centers, aligning with the industry drive to reduce carbon footprints and operational costs [44]. It should be noted that some estimations [45] predict that the emissions from data centers will increase to the levels of the airline industry.

The adaptability of resonant converters to diverse load conditions and precise control over output voltage and current make them an ideal choice for powering servers, networking equipment, and cooling systems, ensuring stability and minimizing downtime. Their compact, lightweight design aligns with the demand for high-density power solutions, optimizing space utilization and supporting data center scalability. As data centers expand, resonant converters emerge as a transformative solution that enhances energy performance, reliability, and environmental sustainability.

1.2.1.4 Solid-State Transformer as Power Router

The most promising and emerging device that can take advantage of resonant converters is the solid-state transformer (SST). This device introduces a new paradigm on power management and routing by being capable of multi-port input-output interface connections and combining buses with different characteristics, as it is illustrated in Fig. 1.2. SST can operate as a power routing [46] device, capable of interconnecting low- and medium-voltage grids and control the power flow depending on the requirements at any specific time. This can assists with the implementation of the V2X and battery storage systems, both industrial and residential [47]. Moreover, it can channel the regenerative braking energy from rail transport and operate as a intermediary between off-shore grid and ships. The building blocks of an SST are illustrated in Fig. 1.1. Note that the terms SST and DCX are used interchangeably in the context of the work.

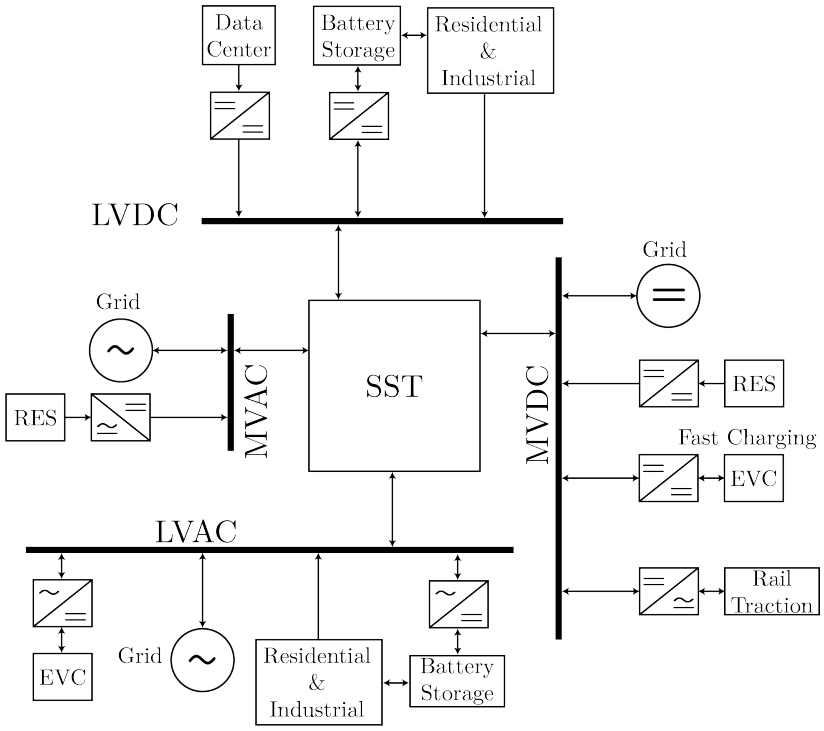


Figure 1.2 The solid-state transformer (SST) as the heart of a new concept of power routing. The SST can control the power flow from generators (power grid and RES) to the loads (residential, commercial, data centers, etc.), as well as control the power flow to and from EVs and batteries.

As in conventional inverters, placing multiple in series, as parts of a greater converter, can increase the voltage-handling capability. Moreover, placing multiple resonant branches in parallel can increase the current-handling capability, without resorting to oversized and expensive resonant components. These techniques can also enable for interconnections between medium-voltage and low-voltage (MV-LV) buses, utilizing input-series output-parallel (ISOP) architectures. Further discussion on the building blocks, modularity, ISOP-IPOS, and partial power handling for the DCX, along with specific applications, can be found in [48, 49].

Resonant converters can be used in a ISOP architecture to isolate the MV AC grid from the LV DC and step-down voltage levels, as in [50]. Modular multilevel converter (MMC) is another way to step down the medium-voltage to lower levers. Other studies [51] propose a hybrid modular multilevel converter, acting as a front-end between the MV grid and different DC loads, like fast-charging stations and data centers. The proposed converters claims 20% losses reduction compared to conventional full-bridge MMC and fault-ride through capability. However, as the converter is unidirectional, the system is unable to take advantage of V2X.

1.3 Scope and Contributions of the Dissertation

This dissertation aims to contribute to the vast field of resonant converter technology, more specifically DC-AC-DC topologies, offering suitable PCB layout strategies, planar magnetic components design and time-domain converter analysis. The specific contributions in each area are presented along with the structure of the document.

Substantial effort is dedicated on concentrating and presenting a useful collection of design rules that define the landscape of practices for high-power high-frequency converters operating in the range of hundreds of kHz to tens of MHz [52, 53, 54, 55, 56]. These practices encompass prudent trace routing, meticulous layout planning, and proper component placement. Moreover, the issues of paralleling power devices is briefly discussed. The culmination of these efforts leads to enhanced reliability, reducing voltage and current overshoots of power converters operating in the dynamic high-frequency domain. Furthermore, literature has shown that the efficiency is improved, especially in hard-switched converters, decreasing in some cases the switching losses up to 26% [57].

A novel facet of the dissertation lies in the vigilant analysis of planar magnetic components — a cornerstone of modern high-frequency power converters. The study carefully examines the geometric parameters of planar windings, namely the outer- and inner-side lengths, the number of turns, the trace width, and the spacing between them, providing an intuitive explanation of their effect on the inductance.

The estimation of the inductance for regular-shaped single-layer windings has been explored in [58, 59] and is presented collectively in [60]. For the rectangle-shaped windings the proposed equations are complex, hard to utilize, and are referred to windings of small dimensions and very-high-frequency [61]. Others [62] considers larger windings for power applications but make arbitrary simplifications without considering any other promising alternative. This work proposes methods for estimating the overall inductance, as well as the inductance per turn, for single-layer windings, by modifying existent well-established equations presented in [59]. These equations provide accurate results with less than 2% mean absolute error, for a dataset of more than 2,600 samples. Since other studies are either not considering power windings or do not have a large enough set, comparisons between the mean absolute error (or any other estimation metric) is impossible. However, the three proposed modified equations provide the same error as the initial regular-shaped low-power equations, as they are presented in [59].

The inductance estimation for multi-layer high-power windings is also considered in this thesis, and two additional geometrical parameters are employed, the number of layers and the distance between them. After comparing different equations and structures, a novel equation is proposed, with less than 1.5% mean absolute error, for a dataset of more than 5,500 samples. Moreover, an optimization methodology is introduced, enabling the selection of geometrical dimensions, that maximize the inductance for a given set of dimensions.

Understanding the effect of geometrical parameters on the electrical characteristics of planar magnetic components allows for the development of proper designs for high-performance power converter systems.

This dissertation further extends to present a comprehensive time-domain analysis for LC series-resonant and LLC converters. Previous studies have presented time-domain analyses for specific operating conditions of the neutral-point half bridge [63, 64, 65] and full-bridge primary bridges [66, 67, 68] or with simplified models [69]. This study deduces closed-form expressions for the initial values of current and voltage waveforms, from the full-order differential equations, and across all operating regions, encompassing inductive, resonant, and capacitive states. Moreover, the dissertation unveils the boundary conditions that separate the transitions between these regions, providing a holistic understanding of the converter behavior. The elucidation of zero-voltage zero-current switching conditions is of particular significance [70], as it comprises a fundamental aspect in converter operation. This rigorous analysis, supported by experimental results, deepens the comprehension of converter dynamics and paves the way for the appropriate component selection in high-frequency power converters.

The state-of-the-art studies on the planar magnetics technology and on the resonant converters are presented in the corresponding points of the text, to assist with the reading flow. More specifically, the analytical, empirical, and arithmetical approaches towards the estimation of single-layer and multilayer windings, are presented in Section 3.2 and 3.3, respectively. The effects of the magnetic core and the equivalent circuits are presented in Section 3.5. Finally, the state-of-the-art on frequency- and time-domain models for LC and LLC resonant converters are presented in Section 4.2.

To summarize the contributions of this dissertation:

- The effects of every geometrical parameter of PWs on the inductance. The necessary modifications on the square-shaped single-layer PWs estimation equations, in order to be applicable to rectangle-shaped PWs (RPWs). The modified equations require the same computational effort and provide similar estimation errors with the original equations.
- The deduction of a new equation, capable of estimating the inductance of multilayer RPWs (MLRPWs). A monomial-like equation form is utilized and its coefficients are extracted using the multiple linear regression algorithm.
- The time-domain analysis of LC series-resonant (LC-SR) and the LLC converter, for all switching regions (switching frequency greater, equal of less than the resonant frequency). This analysis provides closed-form expressions for the voltage and current on every node of the converter. Special consideration is given to the $f_s < f_0$ operational region, where the converter can operate between DCM and CCM, depending on the switching frequency and the load. The boundary between the two operation modes is

extracted. Furthermore, the proper conditions that should be met in order to achieve zero-voltage or zero-current switching (ZVS or ZCS) are defined.

1.4 Related Publications

Journals:

1. T. Papadopoulos and A. Antonopoulos, "Inductance Estimation for High-Power Multilayer Rectangle Planar Windings", *under review*.
2. T. Papadopoulos and A. Antonopoulos, "Extension of Simple and Accurate Inductance Estimation for Rectangular Planar Windings," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, doi: 10.1109/JESTIE.2023.3276349.

Conferences:

1. T. Papadopoulos and A. Antonopoulos, "Time-Domain Analysis of Full-Bridge Series-Resonant Converter and Boundary Conditions for DCM Operation", *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, Aalborg, Denmark, 2023, pp. 1-10.
2. T. Papadopoulos and A. Antonopoulos, "Inductance Estimation for Square-Shaped Multilayer Planar Windings", *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, Hanover, Germany, 2022, pp. 1-10.
3. T. Papadopoulos and A. Antonopoulos, "Formula Evaluation and Voltage Distribution of Planar Transformers Using Rectangular Windings", *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. 1-10, doi: 10.23919/EPE21ECCEEurope50061.2021.9570558.

Chapter 2

PCB Design Rules

2.1 Introduction

In modern power electronics, the pursuit for higher efficiency, increased power density, and improved performance has led to the ascendancy of high-frequency converters. These converters, operating in the kHz to MHz frequency range, have become pivotal components in a plethora of applications, ranging from renewable energy systems and electric vehicles to power supplies and telecommunications infrastructure. As the operating frequencies increase, the significance of printed circuit board (PCB) planning and layout in achieving optimal converter performance is paramount.

The PCB, once considered a mere substrate for mounting components, has now evolved into a critical medium intricately intertwined with the efficiency, electromagnetic compatibility (EMC), thermal management, and overall reliability of the converter. Properly designing and implementing a PCB layout for high-frequency converters demands attention to detail, as even minor design choices can exert profound impact to the converter functionality. Various common and popular design methods have passed from the field of low-power high-frequency PCB designs to that of power converters, potentially creating controversies.

2.1.1 PCB Design Issues for Power Converters

A typical power converter consists of a few power semiconductor devices, several active components such as gate drivers and sensors, and numerous passive components. These elements are necessary for the proper operation and control of the converter. The connections between the components are implemented via copper (or in some cases aluminum) traces, etched on a PCB, and vias to pass signals between layers. Every conduction path and the total layout presents some unwanted properties, which can potentially lead to the reduction of the converter efficiency and reliability.

Power electronic converters design includes all types of signals, namely

- High-power traces and planes (high-voltage and current),
- Low-voltage PWM traces (gate driver input),
- Driving PWM traces (gate driver output),
- Isolated supplies for driving high-side transistors,
- Low-voltage low-frequency controls (gate drivers disable, relay controls, etc.),
- Low-voltage input analog signals (e.g. voltage/current from sensors),

meaning that the PCB design is challenging, since in the same board co-exist signals with a wide frequency and voltage range.

Furthermore, in high-frequency power PCB designs, grounding and return path design is a critical factor. The complexities introduced by high-frequency operation can lead to significant challenges in establishing effective grounding schemes and return planes. These challenges arise due to the existence of inductive loops, signal interference, and voltage fluctuations that can impact the converter performance.

Proper grounding and return path design is essential for minimizing voltage induction, control noise, and maintain signal integrity. In high-frequency converters, the currents flowing through different parts of the circuit can induce voltage fluctuations across the ground plane, resulting in unwanted noise, interference and potential ground bounce. Strategic placement of the components and the ground vias, as well as careful consideration of current paths can help mitigate these issues.

Moreover, high-frequency converters often involve square-shaped switching waveforms that can generate transient currents and voltages in other places of the board. These transients need clear pathways to return to their source, without causing interference with other components or sensitive signals. The reduction of electromagnetic (EM) emissions is particularly important for commercial and industrial devices, since they should not exceed specific levels of EMI to not interfere with other electronic converters and devices (like computers) in their vicinity.

Despite the importance of the layout, literature is still relatively poor on scientific studies and recommendations regarding the placement of the components, the engraving and etching of the traces, the necessary distance between planes and traces of the same and different signals, etc. The main source of information, other than books considering high-frequency mixed signal boards, which do not have to handle high-voltage or high-current like power converters do, are practicing engineers specializing in PCB design. Their opinions and findings are usually shared in seminars, whitepapers, interviews etc. This creates a difficulty in establishing a strong scientific consensus on the topic, and in some cases even produce contradictory results.

For this chapter, the analysis of the parasitic components, the suppression methods and the good design practices are extracted from ECPE lectures [52, 53], textbooks [54,

55], interviews and presentations, like [56], of experts in the field of PCB design. Peer reviewed IEEE articles, discussing some specific problems have been also used, and are cited in the respective text parts. While the topic of PCB design is one that artificial intelligence algorithms, like genetic algorithms [71], could assist greatly, there is much work to be done until they can be considered reliable, and will not be discussed any further.

2.1.2 Purpose and Structure

This chapter aims to delve into the multifaceted domain of PCB planning and layout for high-frequency converters, briefly explaining the development of parasitic elements and suggesting methods and practices to minimize them and reduce their effect, increasing the reliability of the converter. By presenting the issues, and judicious use of layout, parasitic effects can be mitigated, enhancing the converter reliability and reducing losses. Moreover, the chapter elucidates how thoughtful PCB layout can deter the propagation of electromagnetic interference, both internally within the board and externally to the surrounding environment. Techniques for minimizing the switching loop area, controlling signal paths, and strategically positioning critical components are unveiled to create a harmonic coexistence of circuits on the board.

This chapter is structured as follows. First, the equations for parasitic capacitance and inductance are deduced for a two-wire transmission line, along with two PCB trace lines and a trace with ground return plane. The issue of inductive and capacitive coupling is discussed and the effect of displacement current for high-frequency PCB and crosstalk are examined. A set of good design practices is presented, containing recommendations on component placement, trace and layout planning, and the proper layer order for multilayer PCBs. In addition, special attention is given to the design of the switching node, which every power converter has, and the effects of symmetrical PCB design, focusing on the challenges that arise when semiconductor devices are placed in parallel.

2.2 Parasitic Components on a PCB

Every copper wire or trace presents an inherent inductance which increases with length and decreases with its cross-sectional area. Furthermore, the inductance is also determined by the return path of the current. The closer the return path is to the positive trace, the enclosed area between the two gets smaller, and their mutual inductance gets larger, factors that can significantly decrease the inherent parasitic inductance.

The most simple example of parasitic inductance is presented in Fig. 2.1, where two parallel cylindrical lines are illustrated. The total inductance per unit length of the system is given in [72] as

$$L = \frac{\mu_0}{\pi}\left(\frac{1}{4} + \ln\left(\frac{D}{R} - 1\right)\right), \tag{2.1}$$

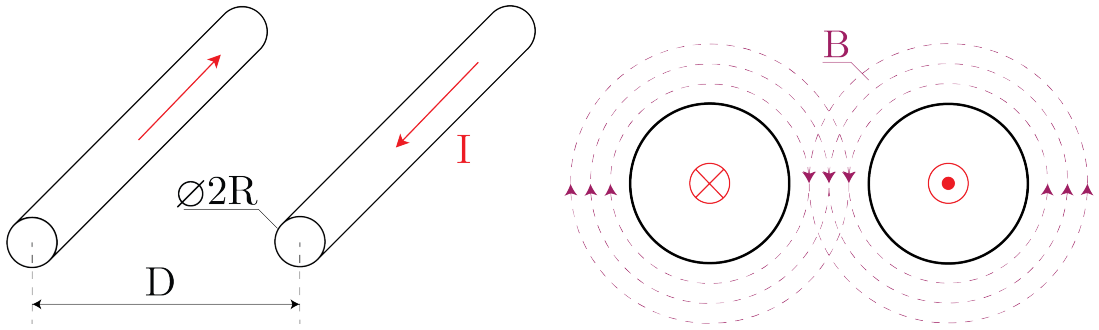
where $\mu_0 = 4\pi 10^{-7}$ is the magnetic permeability of free space, R the radius of each wire, and D the distance between their centers. The term 1/4 corresponds to the self-inductance of each line, caused by the magnetic flux inside the copper. If the internal self-inductance is ignored, and the radius is much smaller compered to the distance separating the two lines ($D \gg R$), (2.1) is simplified to

$$L \approx \frac{\mu_0}{\pi}\ln\left(\frac{D}{R}\right). \tag{2.2}$$

Another way to approximate the inductance of the two parallel lines is by calculating the capacitance between them, as in [72],

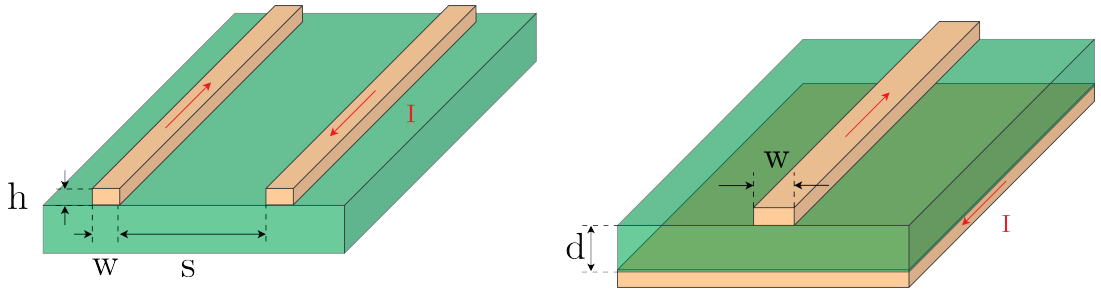
$$C = \frac{\pi\epsilon_0\epsilon_r}{\text{arcCosh}\left(\frac{D}{2R}\right)}, \tag{2.3}$$

where $\epsilon = \epsilon_0\epsilon_r$ is the absolute permittivity, and then by using the equation $\sqrt{LC} = \sqrt{\mu\epsilon}$, which yields,



(a) isometric view **(b)** cross-section

Figure 2.1 Two cylindrical parallel conduction lines.



(a) Pair of traces **(b)** Trace with ground plane return path

Figure 2.2 Most common signal transmission lines in PCBs.

$$L = \frac{\mu_0}{\pi} \operatorname{arcCosh}\left(\frac{D}{2R}\right) \tag{2.4}$$

$$= \frac{\mu_0}{\pi} \ln\left(\frac{D}{2R} + \sqrt{\frac{D^2}{4R^2} - 1}\right). \tag{2.5}$$

Again, if $D \gg R$, (2.4) can be simplified to (2.2).

For estimating the inductance of two parallel traces (of the same current loop), a slight modification of (2.1), is sufficient. The distance between the centers of the two parallel traces is $D = w + s$, where w is the trace width, and s the spacing between them, as illustrated in Fig. 2.2. The radius $R = \sqrt{\frac{wh}{\pi}}$, where h is the trace height, is typically 35 or 70 µm for PCBs. The modified equation is

$$L = \frac{\mu_0}{\pi}\left(\frac{1}{4} + \ln\left(\sqrt{\frac{\pi}{wh}}(w+s) - 1\right)\right). \tag{2.6}$$

which gives the inductance per unit length.

In the case of a ground plane return path, as illustrated in Fig. 2.2b, and given that the width of the trace w is much greater than the height of the substrate h, the parasitic capacitance is

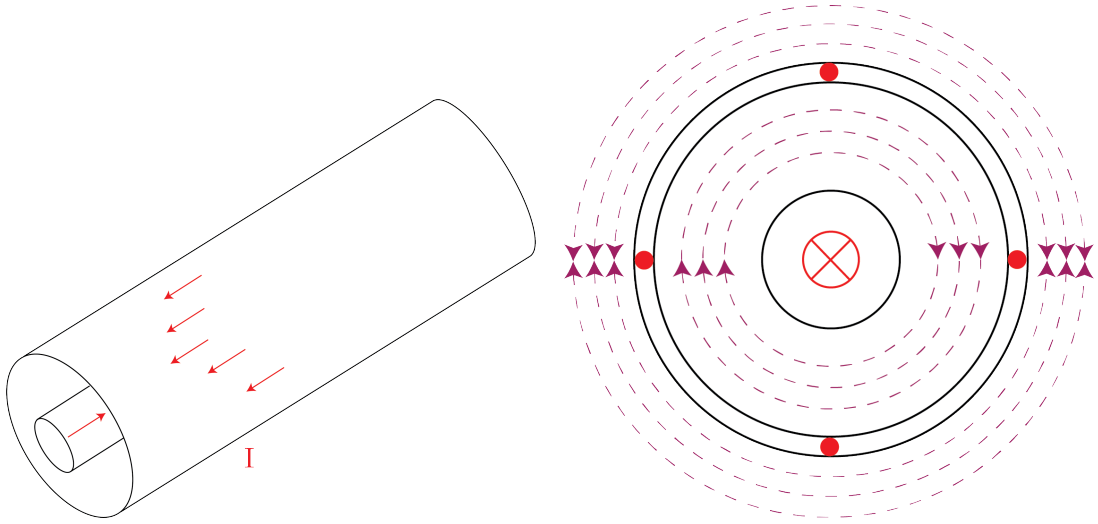
$$C = \epsilon_0 \epsilon_r \frac{w}{d}, \tag{2.7}$$

and the corresponding inductance

$$L = \mu_0 \mu_r \frac{d}{w}, \tag{2.8}$$

where μ_r is the relative permeability of the substrate (FR4).

Another way to transmit signals is with copper wires outside the PCB, which offers more flexibility, but can introduce more parasitics. The less noisy way is utilizing coaxial



(a) Isometric view **(b)** Cross-section

Figure 2.3 Co-axial cable.

cables, as the one illustrated in Fig. 2.3. The negative signal usually uses the cylindrical shell, surrounding the internal wire, offering noise reduction. Furthermore, the coaxial cable significantly reduces the EM radiation, as the magnetic fields of the positive and negative wires cancel each other out, as illustrated in Fig. 2.3b. The corresponding inductance per unit length is

$$L = \frac{\mu_0}{2\pi}\left(\ln\frac{D}{R}\right), \tag{2.9}$$

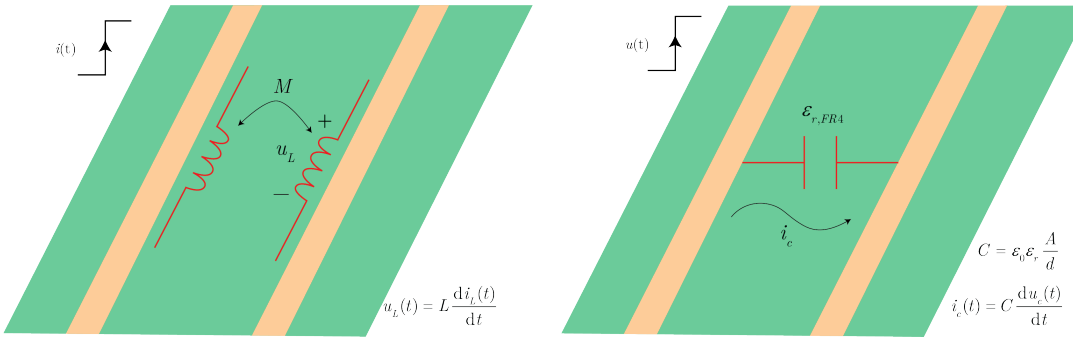
which is the half of the two-wire setup.

A detailed analysis of the impedances of various practical designs, like two parallel traces, a trace with a ground plane return path, etc. can be found in [73]. Matching the impedance of the line with that of the termination component can be useful, especially for high-frequency signals, in order to reduce transient phenomena like signal reflections.

Two traces carrying different signals (belonging to different current loops) can interact with each other due to the intrinsic parasitic inductance and capacitance, as illustrated in Fig. 2.4. Depending on the rate of change of voltage and current, the one or the other can be more significant. This is called crosstalk and leads to signal distortion, inducing smaller signals in the neighboring trace.

In the case of power converters, when power and control traces are close, the distortion can be significant enough to totally disfigure the control signal, potentially causing instability to the control loop. This type of crosstalk should be avoided at any cost, since it can cause malfunction of the whole converter, or even destruction.

Another issue that arises is the displacement current, caused from the parasitic capacitance in high-frequency signals, resulting in the non-uniformity of the current distribution



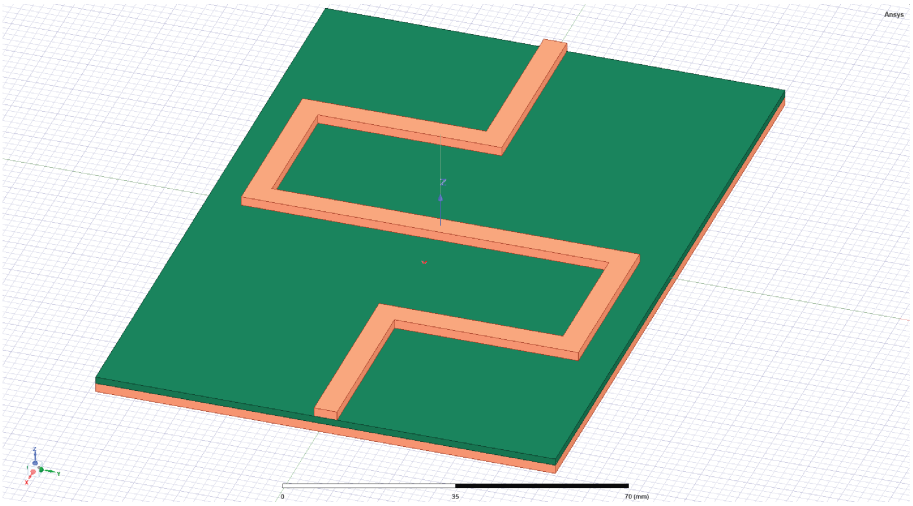
(a) Parasitic inductance **(b)** Parasitic capacitance

Figure 2.4 Parasitic elements on two parallel PCB traces, with two different signals (different current loops).

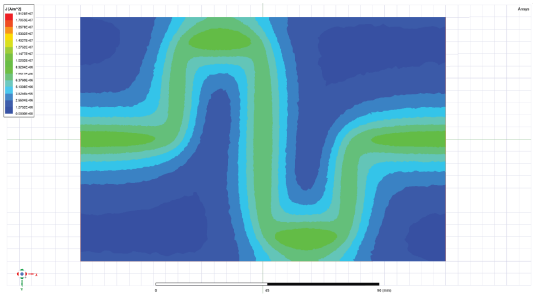
on the return plane path. Even when a wide ground plane is available, return current prefers to occupy the area underneath the positive signal trace, as it is illustrated for an indicative S-shaped trace, in Fig. 2.5d and 2.5e. In Fig. 2.5b and 2.5c, the same effect is presented but for a relative low-frequency signal of 20 kHz, in order to highlight the significance of this phenomenon as frequency increases.

This phenomenon increases the impedance of the return path and can intensify the crosstalk between two lines. Its mitigation is not trivial. The increase of copper height is not always possible, as manufacturers have specific capabilities, and the cost is dramatically increased when custom orders are placed. Removing the copper from the area that is right below the positive trace can reduce the phenomenon, but is a controversial method, as it is allegedly improves some aspects, like common-mode EMI [74], while making others worse, like impedance mismatch and trace routing [75]. When dealing with mixed signals, like in power converters, it is advised to separate the ground planes of high-power and low-power control signals. Furthermore, when possible, separating high-frequency digital signal plane from that of the analog signals can reduce the crosstalk.

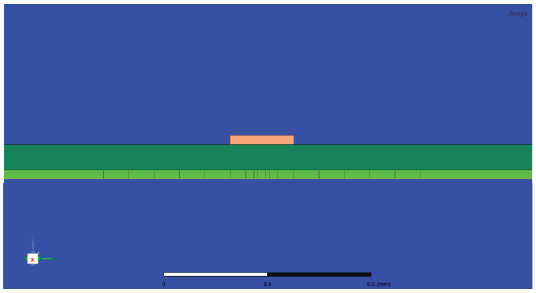
In conclusion, parasitic elements are present everywhere and can cause significant problems if they are not taken into account and no mitigation techniques are applied. The next section discusses the effect that those elements have in real PCBs, along with ways to prevent or reduce their effects.



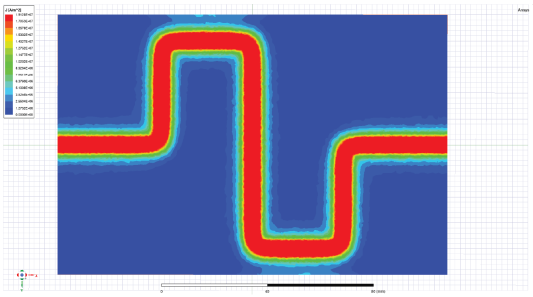
(a) isometric view



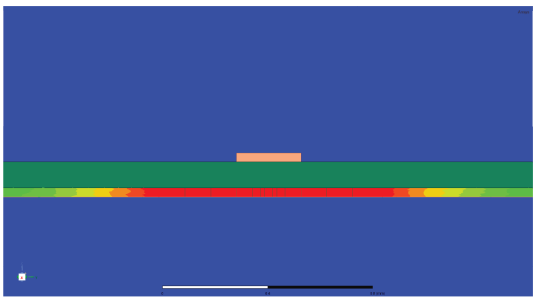
(b) z-axis view



(c) y-axis view



(d) z-axis view



(e) y-axis view

Figure 2.5 PCB with one S-shaped trace and a copper plane return path, and a sinusoidal current of 20 kHz for (b) and (c) and 200 kHz for (d) and (e). The return current does not occupy the whole area of the return plane, but prefers the path right underneath the S-shaped positive path.

2.3 Good Design Practices

The goal of a good design is to reduce unwanted parasitic elements, namely inductors and capacitors, as well as reduce the unwanted communication between paths, typically known as crosstalk. The analytical approach to such a problem is practically difficult, as it requires excellent knowledge of electromagnetic analysis and time-consuming processes. Additionally, the complexity of the problem increases exponentially with the inclusion of additional elements and paths. Certain software packages such as Maxwell3D, HFSS, and Q3D by ANSYS are more attractive solution, but require familiarity with the software and a powerful computing system to analyze real boards with tens of components and traces.

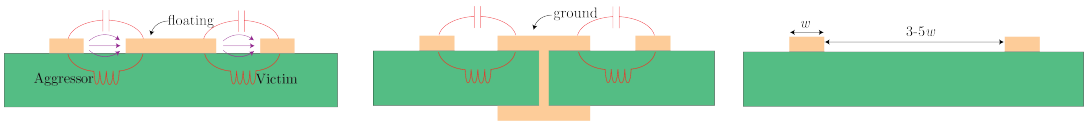
The previous section described the underlying causes that present undesirable effects on a power PCB. This section aims to establish a set of empirical rules (rules of thumb) which can be applied, without having to resort to complex EM analytical approaches. This can be useful, especially during the first phase of the design, in order to achieve good operation of the converter and to reduce the undesirable effects. The design of traces and overall PCB layout is discussed and suggestions are made on layer order for multilayer boards. Furthermore, the proper placement of bypass/decoupling capacitor is presented. Finally, the treatment of switching nodes and the paralleling of discrete semiconductor devices is examined.

2.3.1 Traces and Layout

As discussed in the previous section, crosstalk can appear between two or more signal traces. Signals with high harmonic content can interact with any other, due to electromagnetic phenomena. The severity of the phenomenon increases between high-frequency high-power traces and low-power control traces, and the possibility of instability is significant. In the context of this work, traces that tend to produce EM noise are referred to as aggressors, and traces that are most susceptible to this are referred as victims.

A common rule to reduce crosstalk is to keep a distance of at least $3w$ to $5w$ between traces, where w is the width of the trace. In Fig. 2.6, three cases are presented, where the distance between the aggressor and the victim is the same, but in the first two cases a copper island exists between them, and in the third all the copper has been removed. The first case, where the copper island is floating (it has no reference), can present the largest crosstalk. When current passes through the aggressor, electric charges also flow through the floating island, causing noise to the victim.

The existence of a grounded copper island is controversial. On the one hand ground is considered capable of sinking noise from high-frequency traces. On the other hand, the parasitic inductance of the ground in combination with large $\mathrm{d}i/\mathrm{d}t$ of the power side, can cause bouncing, which will induce noise to the victim trace. The debate is still open on whether a grounded island or the removal of any copper is the best choice for reducing crosstalk and EMI.



(a) (b) (c)

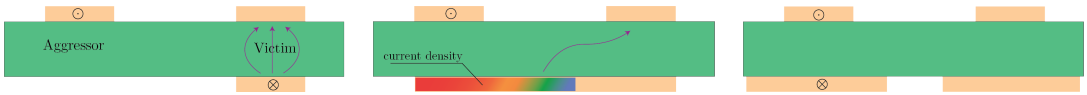
Figure 2.6 Parasitic capacitance and mutual inductance leading to crosstalk between two different signal traces, with (a) a floating copper island and (b) a grounded two-layer island between them, and (c) lack of copper island.

When the design does not allow for a spacing large enough, splitting the planes can restrict the return current to a smaller region. As illustrated in Fig. 2.7a, if the return path is under a potential-victim trace, the crosstalk is maximized. In Fig. 2.7b the plane surface increases and the current concentrates under the positive signal path, the crosstalk is limited. Separating the two grounds, contains the return current to a neighborhood far from the potential-victim trace, as presented in Fig. 2.7c. This return current containment can also reduce the loop area and ground bounce, as discussed in [76].

It should be noted that increasing the distance between the two layers results in reduction of the phenomenon of the displacement current. This may seem like a desired effect but is actually a bad practice, as it increases the fringe on the magnetic field and increases crosstalk. As it is discussed in the subsection 2.3.2, each trace and its corresponding ground plane should be kept as close as possible.

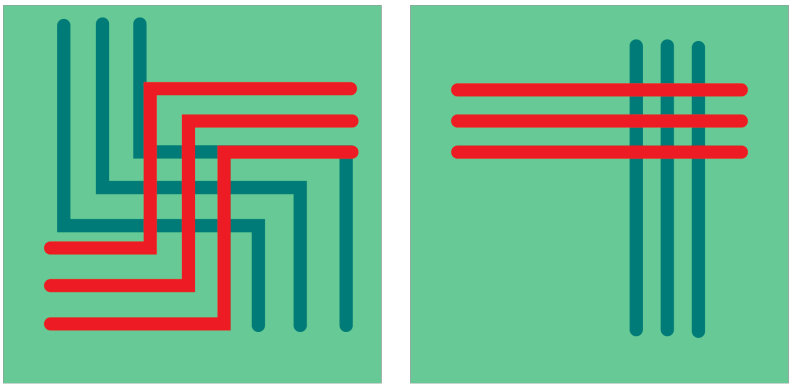
Another effective way of drastically reducing the crosstalk is designing the traces of the two consecutive layers perpendicular to each other, as illustrated in Fig. 2.8. This way the overlapping of the copper and therefore the parasitic capacitance is decreased. In addition, the magnetic fields generated by each trace are also perpendicular to each other minimizing their interaction.

Generally, overlaying low-frequency DC traces of the same conduction path is advised, as it decreases the parasitic inductance, due to the negative mutual flux, and increases the parasitic capacitance. This can assist with fast current transients, since the distributed parasitic capacitor can work as a low equivalent series capacitor energy storage. For high-frequency DC and AC traces the issue is more complex. When the positive and negative traces are close, the magnetic field is confined and the EMI is reduced. However, the parasitic



(a) (b) (c)

Figure 2.7 Crosstalk between two different signal traces, and methods to mitigate it when there is not enough distance between them.



(a) Improper pathing **(b)** Proper pathing

Figure 2.8 Possible layouts of traces in two different layers. Designing the traces with 90^o rotation between layers minimizes the crosstalk.

capacitance that is developed between the traces can cause undesirable effects, like filter or resonant circuit degradation.

Utilizing FEM simulation programs is a relative fast and inexpensive way to evaluate the EMI and try-out different layouts. To compare multiple laboratory prototypes, as in [77] and [78], is also an effective way to settle this subject for a specific application. The comparison can be made directly, based on the response of the converter, or indirectly, based on the parasitic inductance and capacitance. In [79] a set of techniques for measuring parasitic elements for SiC half-bridge configurations is presented. It is possible to modify these techniques for different types of converter and semiconductor devices. In any case, further research is needed, especially for power converter layouts.

2.3.2 Layer Order

To understand the necessity for specific layer order, it is important to remember that the energy of any circuit does not travel in the current, but in the electromagnetic field. When the levels, of a multilayer boards, have the proper sequence, the transmission line is set between a trace an the ground plane, the fields are contained within the two layers and the radiation to other loops is mitigated. It is crucial to ensure that grounding is one dielectric space away from the corresponding signal. The same is true for the power supply plane; it should be one dielectric space away from the corresponding ground.

The simplest case is illustrated in Fig. 2.9 for a two-layer board. The high-power, and low-power digital and analog traces can be on the the first layer, with the corresponding ground plane right underneath. As already discussed, surrounding the positive traces with the respective ground in the same layer is controversial. However, if enough space is available to create large-width ground traces parallel to the positive one, it is probably the best design choice.

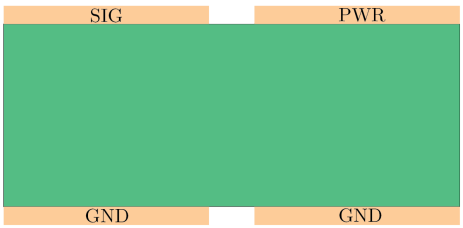


Figure 2.9 Recommended layer order for a 2-layer board.

(a)

L1	GND	PWR
L2	PWR	GND
L3	SIG	GND
L4	GND	SIG

(b)

Figure 2.10 Layer order recommendations for a 4-layer board.

Four-layer boards are widely available from large manufacturers and can be used to increase the power density of the converter. The cross-section and the optimal layer order is illustrated in Fig. 2.10. As can be seen, the layers are not equally distanced within the board, but are grouped together in groups of two, namely L1-L2 and L3-L4. Placing the ground planes on the external layers can reduce the EMI and provide close reference to high- and low-power signals. Placing the positive traces on the external layers and the ground planes on the internal is also an acceptable tactic. It can assist with the thermal dissipation of the traces, but it is more probable to increase the EMI.

As the components can only be placed in the external layers, it is possible that the design will require to mix of high- and low-power, digital and analog signals, to the first L1 or last L4 layers. This is permitted, but proper measures should be taken, namely providing the corresponding ground in the internal layers, and draw a corresponding parallel negative via close the any positive one. The last recommendation is usually overlooked, leading to fringing of the magnetic flux and potentially increasing crosstalk and EMI.

It should be noted that passive and active components can be designed as embedded parts in a PCB, reducing the parasitic elements. For example, in [80], a 3.3 kW power-factor correction buck converter is presented, with embedded SiC diodes are MOSFETs, as well as gate drives and passive elements. Nevertheless, this design makes any repairs impossible, and increases the cost significantly.

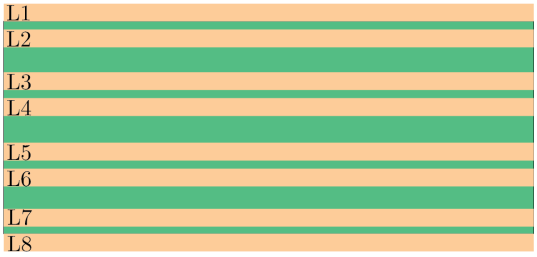
In [57] the effect of parasitic capacitance between the layers of a 4-layered full-bridge inverter board, is explored. It has been found that by reducing the overlaps between the negative DC bus, AC traces and control-ground plane, the parasitic-capacitance related losses

(a)

L1	GND	PWR	PWR
L2	PWR	GND	GND
L3	GND	SIG	SIG
L4	GND	GND	SIG
L5	SIG	SIG	GND
L6	GND	GND	PWR

(b)

Figure 2.11 Layer order recommendations for a 6-layer board.



(a)

L1	PWR	PWR	PWR
L2	GND	GND	GND
L3	SIG	SIG	SIG
L4	SIG	GND	GND
L5	GND	GND	GND
L6	SIG	PWR	SIG
L7	GND	GND	GND
L8	PWR	SIG	PWR

(b)

Figure 2.12 Layer order recommendations for a 8-layer board.

are decreased by 40% and the switching losses by 26%. These numbers are not necessarily reproducible in other setups, but are indicative of the effect a proper layout and the correct order have on the efficiency of the converter.

Six-layer boards have also become inexpensive over the last years. Power converters do not usually rely on such high-layer count, and utilize modular two- or four-layer boards, which are connected perpendicular to each other or stacked one upon the other. The biggest asset of six-layer boards is that they are capable to enclose all high-frequency signals within the board, by grounding the external layers L1 and L6, as illustrated in Fig. 2.11, and draw multiple vias between them, a technique that is called fencing.

Other orders are also appropriate, such as pairing each positive line with the respective ground reference. As stated in the case of two- and four-layer boards, it is possible to split each layer to carry multiple high- and low-frequency signals, as long as the corresponding ground reference layer is in the vicinity of the positive trace, together with the parallel positive-negative vias, where they are required.

Eight- and higher-order-layer boards are mostly utilized in high-frequency mixed signal low-power boards, like computer motherboards, and not in power electronics. Some indicative proper layer-orders are presented in Fig. 2.12, for the sake of completeness.

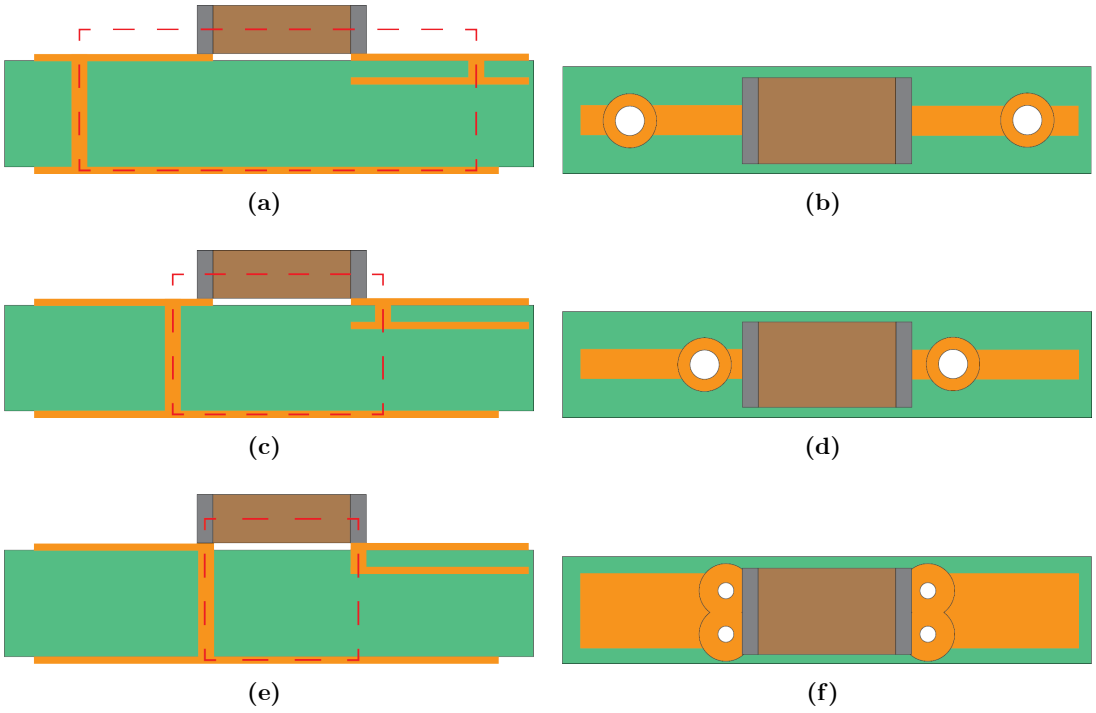
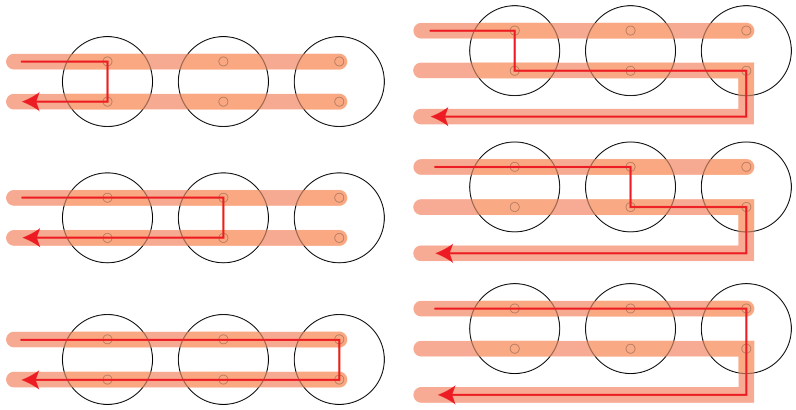


Figure 2.13 Cross-section and top-view of the position of a capacitor in a multilayer board, with (a) high, (c) medium, and (e) low parasitic inductance. The closest the via are to the terminals of the capacitor the lower the cross-sectional area and, hence, the inductance. Multiple vias increase the current-handling capability of the trace and the capacitor.

2.3.3 Capacitors

Capacitors are usually connected between the supply voltage and the ground of the integrated circuit (IC) and have a dual role. Since their impedance is inversely proportional to frequency, they are capable of providing a low impedance path for the typically high-frequency noise coming from the power supply, acting as a bypass line. Furthermore, they can provide energy in the form of bursts of current when they are needed by the IC, for example when a gate driver tries to turn on a MOSFET, acting like decoupling devices. Their abilities are, however, limited by the equivalent series inductance (ESL) and the parasitic inductance of the traces.

To compensate this, many designs place capacitors of low intrinsic ESL, or multiple capacitors in parallel in order to artificially reduce it. Furthermore, the traces that connect the capacitor play a significant role on the additional parasitic inductance. As it is illustrated in Fig. 2.13, manipulating the traces and the vias so that the cross-sectional area and the length are minimized can provide a better bypass effect. Another commonly used method is the placement of two different type of capacitors in parallel, one electrolytic and one ceramic. The first has greater ESR and ESL but can store more energy, which is suitable for lower-frequency higher-power demands of the IC. Contrary to that, the second can store



(a) Impedance mismatch **(b)** Impedance matching

Figure 2.14 Parallel connection of capacitors on a DC Bus.

less energy but due to the lower ESR and ESL can provide higher-frequency current, for the nano- to micro-second transients.

The effect that proper layout, layer order, and capacitor placement has to the performance of the converter is highlighted in [81], where the parasitic inductance of high-frequency GaN converter is reduced by 40%, along with the transient voltage overshoot by 35 %, and power losses by 10%.

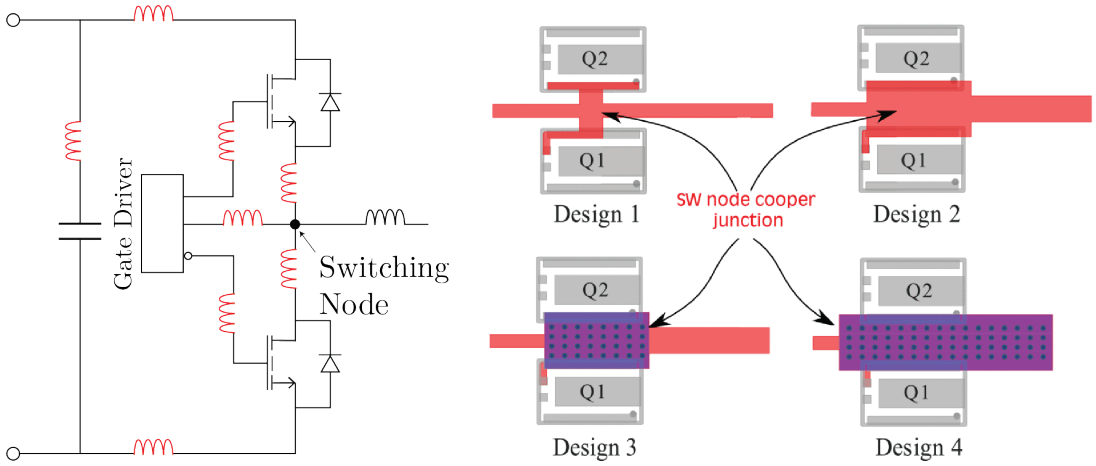
In most cases, a single 100 nF ceramic capacitor, typically an MLCC, is enough to ensure both the bypass and decoupling functions that are required by the IC to work properly. If two capacitors are placed in parallel, the electrolytic is usually 10 μF and the ceramic 100 nF.

However, special consideration is needed for capacitors on the DC bus, used to stabilize the direct voltage. When the capacitors are connected on the one side of the DC bus, as it is depicted in Fig. 2.14a, an impedance mismatch is created, since each capacitor has different trace length. Creating a third trace parallel to the first two, as in Fig. 2.14b, can reduce the mismatching.

2.3.4 Switching Nodes

Switching node is the point where one transistor, one diode, and one inductor meet, as illustrated for an indicative case in Fig. 2.15a. Every DC–DC switching configuration encompasses this node, which serves as a pivotal point where the current of the inductor can be commutated towards either the diode or the switch, depending on the switch state, and causes EMI.

As the current at this node alternates between the diode and the switch, it needs to alternately force the diode to change state too. The diode commutates from being reverse-biased when the switch is ON, to forward-biased when the switch is OFF. As a result, the



(a) Schematic **(b)** Layouts [84]

Figure 2.15 Parasitic inductance present in a typical half-bridge converter layout.

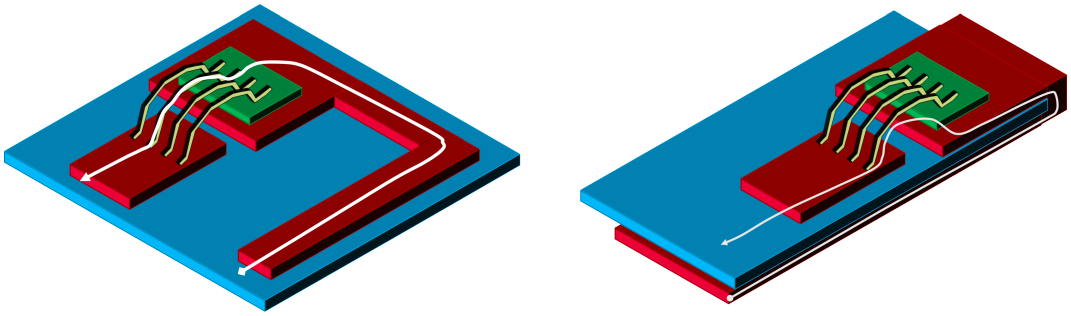
voltage at this node exhibits a characteristic oscillation. Attaching a probe at this location — where the ground clip of the probe is linked to the power supply ground (0 V) — will consistently reveal a voltage waveform characterized by sharp transitions (like a square-wave). This waveform closely resembles the inductor voltage waveform, albeit with a DC level-shift that varies according to the specific topology employed.

On a practical level during the PCB design phase, careful consideration must be given to the allocation of copper around the switching node, due to the high du/dt and di/dt it experiences. Excessive copper in this vicinity can inadvertently transform it into an efficient EM-field antenna, dispersing interference into the surrounding environment. Consequently, the radiated noise can be intercepted by other traces, subsequently propagating it directly to sensitive low-power electronics or to the load [82, 83].

However, there is a delicate balance between thermal management of the node and EMI, as it is discussed in [84]. As presented in Fig. 2.15b, four different layouts are experimentally tested, where: (1) a thin trace connects the source and the drain of the high- and low-side transistors, (2) the trace in enlarged, and (3) and (4) thermal relief vias are placed between the top and bottom layers. Designs 2 and 3 occupy the same surface area, but the trace of 4 is enlarged up to the point where the inductor is connected. The results reveal that design 4 has the best performance regarding the thermal dissipation, EMI and $\boldsymbol{U_{DS}}$ oscillations of the low-side MOSFET, with designs 3 and 2 following behind.

These results verify the general advice that components should be as close as possible to the switching node and the trace should be as wide enough to handle the nominal current, without changing width along the path.

Manipulating the parasitic elements, especially at a switching node, can be very useful. As discussed in subsection 2.3.3, the placement of each component and the arrival and departure traces play a significant role on the parasitic inductance. Designing the traces close



(a) High loop inductance **(b)** Low loop inductance

Figure 2.16 Layout of high-power traces for semiconductor switch [52].

to each other and taking advantage of the very small distance between L1-L2 and L3-L4 can drastically reduce the cross-section and the inductance. However, it may also increase the parasitic capacitance between the two signals, which is not an issue when placing a capacitor, but can be for other components.

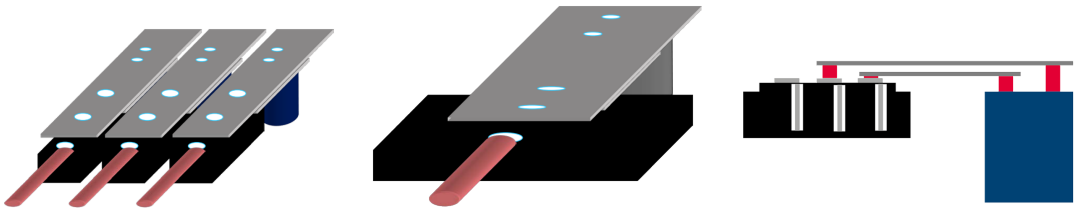
Two techniques that can influence the parasitics are presented in Fig. 2.16. In Fig. 2.16a an example of high-loop inductance with low parasitic capacitance is shown, for a semiconductor device and the bondwires. By designing a set of vias at the end of the device and the return path right underneath the positive path, the loop inductance decreases, as presented in 2.16b, but leads to greater loop capacitance.

2.3.5 Transistors in Parallel Operation

A well-established method for increasing the power-handling capability of a converter is increasing the current that the semiconductor devices can handle. This can be achieved by devices of higher nominal current, or by paralleling devices of lower nominal current than the required value. The paralleling process can by less expensive and even increase the overall efficiency, by reducing conduction losses. Yet, the placement and the routing of the devices affect the transients and even the steady-state current sharing between them, if the switching frequency is high enough.

As it is illustrated in Fig. 2.17, another advantage of paralleling discrete components or modules is the multiple vias through which the current passes. This prevents the creation of bottlenecks and reduces both the parasitic resistance and inductance. For this particular case, high-power modules with copper plates are used, instead of PCB embedded traces. The proper setup is presented in Fig. 2.17c, which is uncoincidentally identical to that of a PCB design.

Decisions that might seem minor during the design of a PCB can lead to notable asymmetries, as it is illustrated in Fig. 2.18a and 2.18b, where the layout and the equivalent circuit are presented. The same layout, with the same amount of copper can be designed in

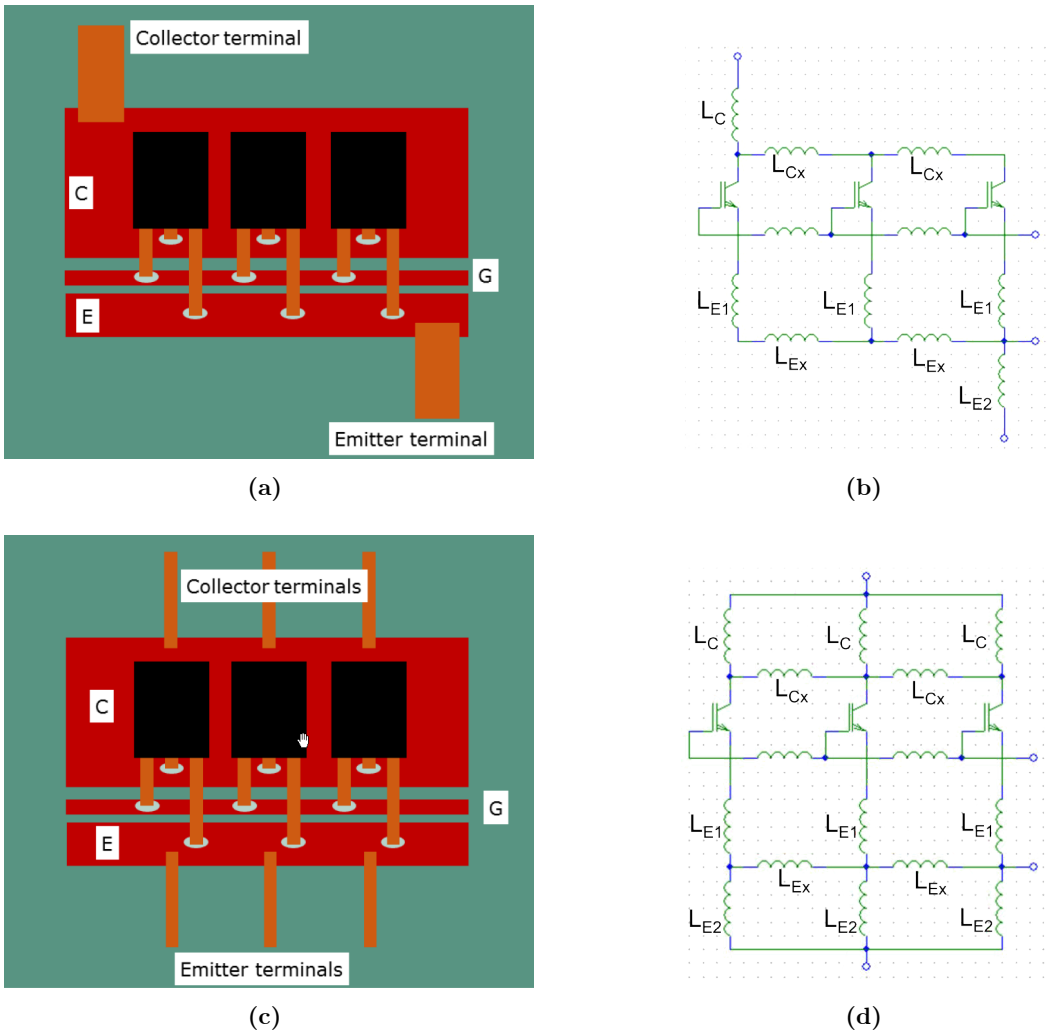


(a) Three parallel half-bridge modules

(b) One high-power module

(c) Proper placement of DC plates

Figure 2.17 Connecting three half-bridge modules in parallel offers greater overall trace width and more vias, compared to one high-power module. The vias can present [52].



(a) **(b)**

(c) **(d)**

Figure 2.18 Layout of three parallel semiconductor devices and the corresponding circuit diagrams. An asymmetrical layout is presented in (a) and (b), where the parasitic inductance from the positive to negative of the DC bus is different for each branch. The symmetrical version is presented in (c) and (d), where the total inductance is almost the same for each branch [52].

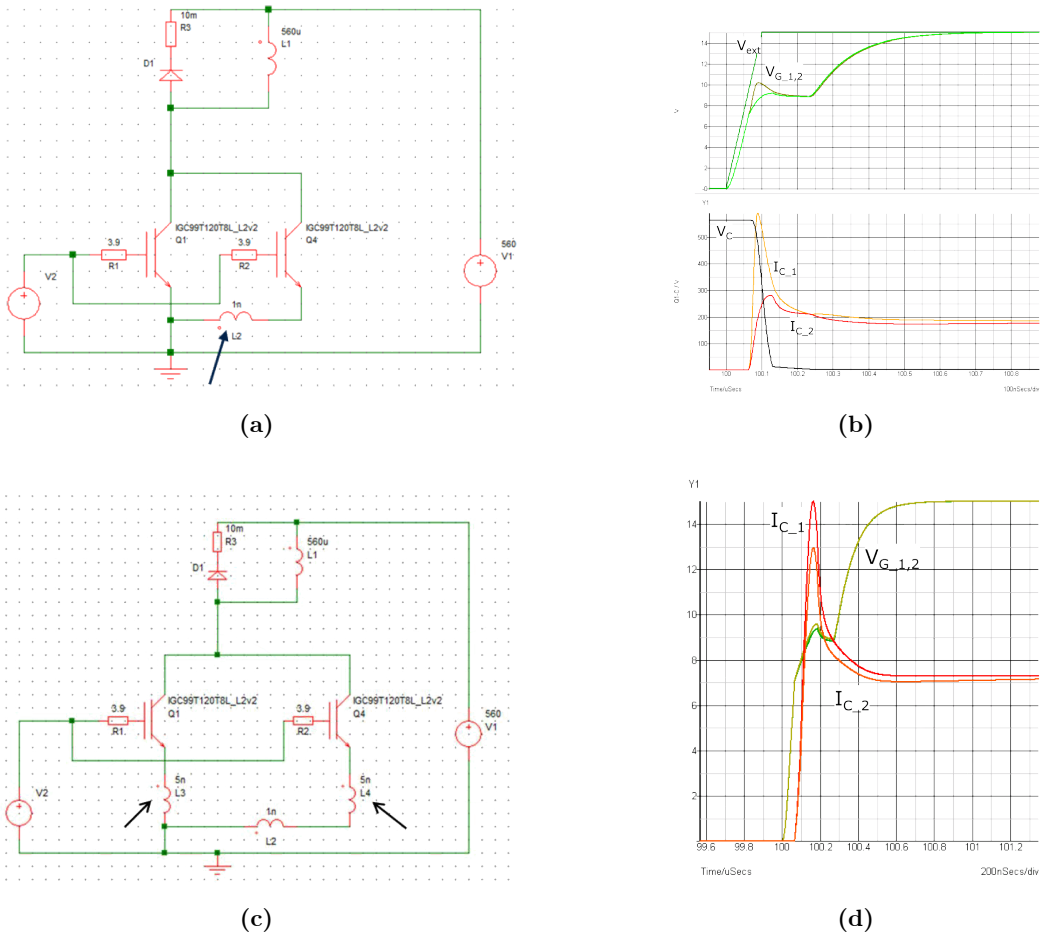


Figure 2.19 Current response of (a) and (b) an asymmetrical parallel topology of two devices, and (c) and (d) a symmetrical one. The current is shared more equally in the symmetrical design [52].

a symmetrical fashion, as presented in Fig. 2.18c and 2.18d. The significance of the symmetry of the components is also highlighted in [78, 85], for an LLC resonant converter, which is discussed in Chapter 4. Moving the switching component from the front layer to the back enables a more symmetric routing of the traces, and therefore a more efficient operation.

To further emphasize the importance of these issues when paralleling semiconductor devices, the current response of two parallel IGBTs is presented in Fig. 2.19, for a double pulse circuit topology. Even a minimal 1 nH parasitic inductance on the emitter of Q_4 can lead to a 2/3 – 1/3 current distribution for Q_1 and Q_4, respectively. Designing the traces in a more symmetrical manner, even if this results in an increase in emitter inductance (4 nH for this particular case), leads to a more even distribution of the current between the two IGBTs, as illustrated in Fig. 2.19d.

2.4 Conclusions

A good PCB design does not only aim to minimize the length of each trace, but also to minimize the cross sectional area that is formed by the trace and its ground reference. Larger cross-section means increased parasitic inductance, which can lead to an increase in noise induced internally from the board and by external factors. To reduce internal noise between different signals, there should be adequate distance between noisy and sensitive traces to reduce crosstalk. For example, high-frequency high-power and low-power digital traces should not be near each other, neither near analog-carrying traces, as the first can distort the signal of the second. Reducing EMI to and from external devices is relatively easier and requires shielding, like a Faraday cage.

Of special note is the meticulous attention devoted to the intricate design of the switching node—an omnipresent facet in every power converter. Moreover, the ramifications of symmetrical PCB designs are critically appraised, focusing particularly on the intricate challenge of effectively paralleling semiconductor devices—an aspect that assumes paramount significance in converter performance enhancement. In total, this chapter serves as a set of suggestions, unraveling the complexities of high-frequency converter PCB layout and offering a practical roadmap towards optimizing their performance, efficiency, and robustness.

There is still much work to be done on this topic. A set of generic rules on designing power converters must be produced, which further specializes in specific converter types, like buck/boost, inverter, resonant, multilevel etc. The accumulated knowledge that is provided by experts of the field, and in some degree in the literature, should be tested in a greater extend and published in peer-reviewed papers to start building the scientific consensus, on this multi-variable topic.

Chapter 3

Planar Windings

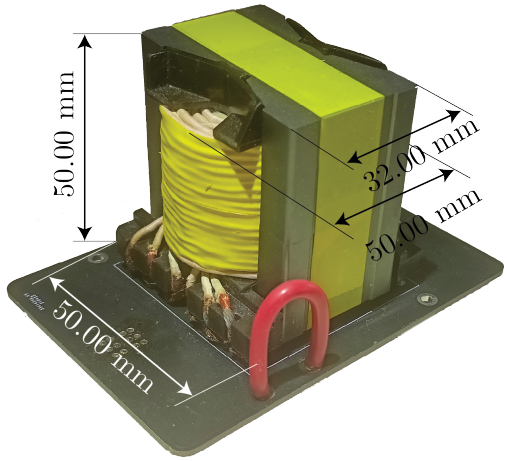
3.1 Introduction

Magnetic components constitute a cornerstone of the electrical circuits, converters and the power grid. Inductors operate by generating and storing the magnetic energy. Galvanic isolation, voltage level change and multi-terminal capability can be achieved via a transformer, which converts electrical energy to magnetic and then back to electrical. Utilizing the same principle, chokes can reduce the common and differential mode noise by increasing the apparent impedance for the undesirable frequencies.

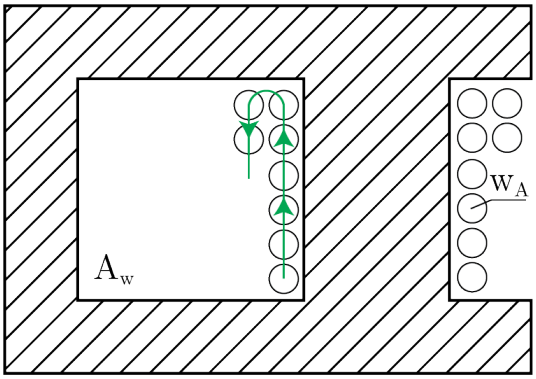
Magnetic components regularly represent a large portion of total volume and weight of a power converter and power systems, especially for low-frequency operation. Increasing the frequency leads to windings of smaller dimensions without affecting the corresponding impedance. Furthermore, high-frequency cored windings reduce the necessary peak magnetic flux (for the same induced voltage), hence require cores of smaller cross-section area. However, as frequency increases, so do the losses of the windings and the core.

For high-frequency current, its density decreases exponentially from the surface to the core of the conductor, a phenomenon known as skin effect. This results to the increase of the ohmic resistance, usually symbolized as R_{AC}, leading to increased losses and reduced efficiency. In this case, special attention is required to the shape of the conductors. The utilization of solid conductors thinner than the skin depth δ of the conductor material or Litz wires, can significantly reduce the R_{AC}.

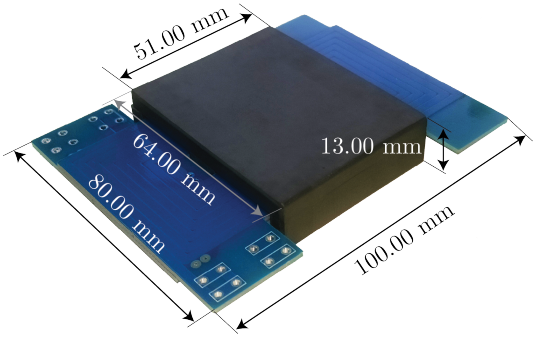
In the case a magnetic core is used, core losses increase with higher switching frequency. Magnetic materials of greater resistivity and narrower B-H loops are necessary to reduce the creation of eddy currents within the material and reduce the hysteresis losses. Such materials are NiZn and MnZn alloys, which are broadly available in many sizes and shapes by major and small manufacturers, and can also be produced on-demand for practically any shape.



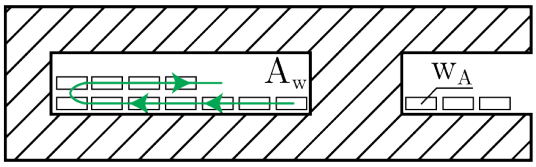
(a) Conventional winding



(b) Conventional winding cross-section



(c) Planar winding



(d) Planar winding cross-section

Figure 3.1 High-frequency conventional and planar windings with the respective cross-sections.

Another aspect is the physical design of the components, which has to consider the spatial limitations and the desired inductance value, as well as the thermal limitations. Those are usually dictated by the actual application the component is meant to be used.

3.1.1 Architecture of High-Frequency Magnetic Components

Magnetic components can be classified into two main categories with respect to the construction architecture: (i) the predominant "conventional" windings wrapped around an axis and (ii) planar windings, where each turn extends outwards, on the same plane. Both categories are illustrated in Fig. 3.1, along with the window cross-sections and the way new turns are introduced. Toroidal architectures are also available, but are usually utilized in chokes, for common and differential mode noise rejection, and will not be further discussed in this context.

Conventional designs extend by almost the same length in all directions, as it is illustrated in Fig. 3.1a. Typically, they use solid, stranded or Litz type wires depending on the nominal

power and frequency. Usually the windings are wrapped around a ferrite core and turns are added parallel to the z-axis, hence each turn (of the same column) encloses the same loop area. When the column is fully filled, a new column can be used for adding new turns, which have a slightly greater loop area, as presented in Fig. 3.1b. Depending on the available space on the z-axis and the total number of turns, the first and last column can enclose areas of considerably different sizes.

Planar designs expand mostly in the xy-plane, as presented in Fig. 3.1c. Turns are added in the same row (on the same plane), next to each other, meaning that every new turn encloses a different loop area. In the case of multilayer designs, when the row is fully covered, the new turns are added in a separate row, adjacent to the previous, as it is illustrated in Fig. 3.1d.

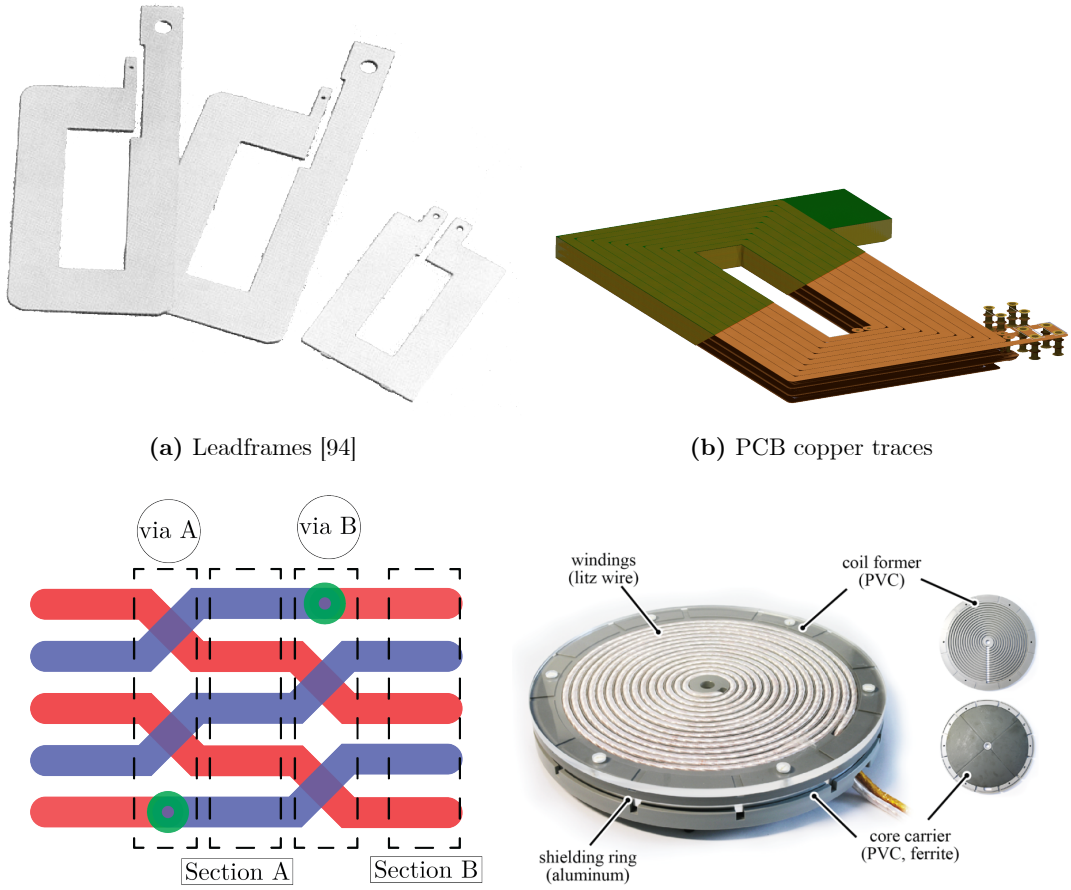
In the case of cored windings illustrated in Fig. 3.1, as the window A_w, becomes fully filled, the electrical behavior of the conventional and planar architectures becomes similar. The differentiation stands on the mechanical construction process, the occupied space and the thermal dissipation capabilities.

Planar Windings (PWs) can be categorized according to the shape, i.e., square, hexagonal, circular, rectangular, etc. Regular-polygon single-layer shapes present symmetries that facilitate the analysis and have been extensively discussed in literature [58, 59, 60, 86, 87]. Other shapes, namely rectangular, have been discussed mainly for Wireless Power Transfer (WPT) systems [62, 88, 89].

Another way of categorization depends on the manufacturing process: high-current planar windings can be constructed with copper bars properly bended (leadframes), and low-current windings can be directly printed on a standard insulating substrate (like FR-4) as any other PCB. Traces can be solid, or entangled in a way that is representing Litz type conductor [88, 90, 91, 92, 93]. Wireless Power Transfer (WTP) devices tend to use planar designs, placed upon a plastic of ferrite plate, for structural reasons. Illustrations of the those categories are presented in Fig. 3.2.

PWs are suitable for both inductor and transformer utilization, especially in the case of limited space on the z-axis. They can be integrated in the power PCB (even flex [95]) or discretely placed as a separate component, with the respective cases presented in Fig. 3.3. When leadframes are used as conductors, the height can be adjusted to reduce or totally suppress the skin effect phenomenon.

Direct PCB etching, where the copper height is typically 35 to 70 μm, can handle frequencies up to 3.5 and 1.6 MHz [96], respectively. When higher frequency current is present, it is possible to arrange traces properly and represent Litz-type wire or use Litz-wire as in conventional components. The shape of the corner for the copper traces (square, trapezoid, round) seems to affect the R_{AC}, but only slightly [97]. The main issue that arises with sharp corners is the increase of the electric field and, therefore, the higher chance of voltage break-



(a) Leadframes [94]

(b) PCB copper traces

(c) PCB adapted Litz type, based on [90]

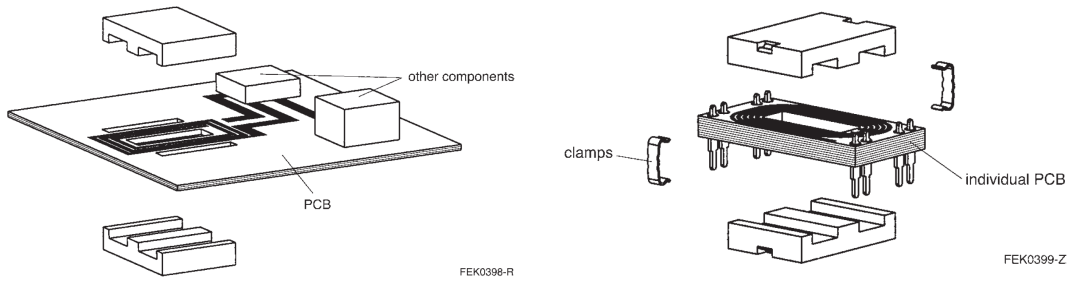
(d) WPT/IPT Litz-wire coil [88]

Figure 3.2 Conductor types for PWs.

down between the two adjacent turns. In this work only round corners are considered, which are the default selection for any Computer-Aided Design (CAD) program, i.e., KiCAD.

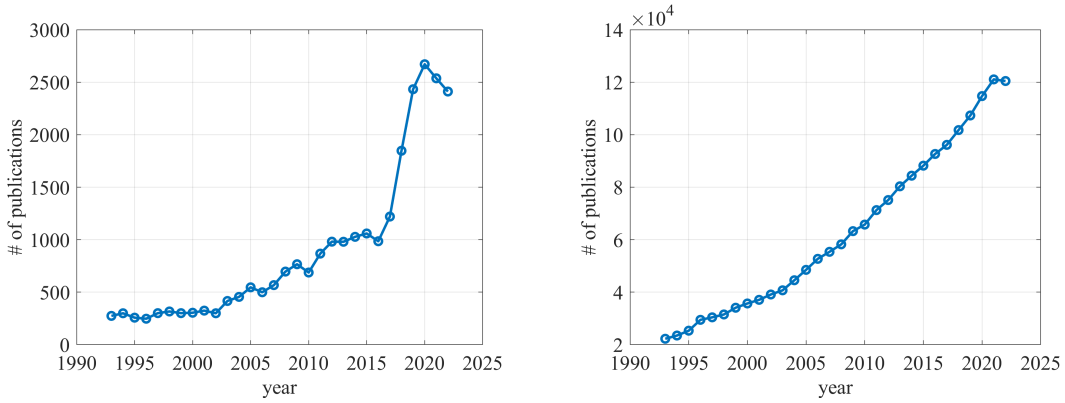
Furthermore, PWs present greater surface area increasing the heat dissipation [98], a very useful property for high-power magnetic components. The thermal behavior of PWs is extensively discussed in [99], where the copper traces, the FR4 insulation layers and the ferrite core are taken into account.

A discussion on the optimal design, based on the tradeoffs that are presented when regarding the skin effect, the winding and core losses, the leakage inductance and the stray capacitance, is presented in [100]. Interleaved architectures, where the primary and secondary windings are introduced alternately are proposed, as the optimal tradeoff between the different problem aspects.



(a) Embedded design **(b)** Discrete PCB

Figure 3.3 PTFs core assembly as a part of the converter PCB (embedded), or a discrete PCB with proper connectors [101].



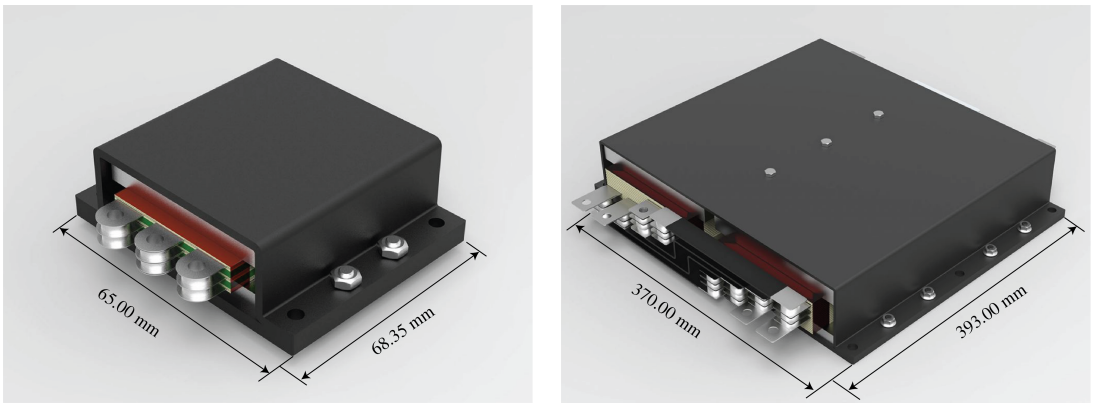
(a) IEEE journals **(b)** Total

Figure 3.4 Approximation of the number of scientific articles discussing planar magnetics from 1993 to 2022 [102].

3.1.2 Commercial and Industrial Applications of PWs

Real-world applications of planar magnetics lag behind when compared to conventional designs. However, in recent years they have gained market-share, a fact that can be backed up by the growth of established companies and the emergence of new ones. Also, they have gained an interest in scientific research articles, as it is illustrated in Fig. 3.4, separately for IEEE journals and in total, respectively.

Many applications can benefit from the use of planar windings, like spaces with limited z-axis, such as rack-mounted power supplies and EV power converters, wireless power transfer systems for charging mobile devices and vehicles. Other real-world applications, according to two major manufacturers, Payton [103] and Himag [104], are aviation [105, 106], traction and automotive, medical (in both heavy machines, like CT scanners and implanted medical devices, like artificial cardiac pacemaker for charging and communication purposes), telecommunications, data centers [107] and industrial applications. Furthermore, planar windings can be used as common and differential mode filters, as suggested in [108]. Two indicative



(a) PTF 1.0 kW, 1.0 kV, 250 kHz, 50:1 ratio [115] **(b)** PTF 350 kW, 800 V, 50kHz, 6:4:4 ratio [116]

Figure 3.5 Two indicative cases of commercially available PTFs from HiMAG Planar Magnetics.

off-the-shelf PTFs are presented in Fig. 3.5, one for a 1 kW, 1kV 50:1 ratio system and the other for a 350 kW, 800 V, 6:4:4 ratio system.

PTFs and planar inductors can be used in resonant converters, such as LC, LLC, and CLLC, with several related application notes published from major semiconductor manufacturers. For example, design applications for an 1.4 kW LLC [109], and a 6 kW DAB [110] have been published from Infineon and Texas Instruments, respectively. DC/DC converters can also benefit, like the synchronous buck-boost 500 W converter, which has been developed around an LTC3779 from Analog Devices [111], and the low-power high-voltage-gain multilevel flyback converter [112], utilizing a PTF from Coilcraft [113].

Other niche applications include coreless long-distance isolated power transfer for auxiliary supplies in medium-voltage converters, demonstrating 81% peak efficiency at 15 Watts [114].

High-power transformers, even with high-efficiency, are required to dissipate considerable amounts of wasted power. For example, the 350 kW Himag PTF, illustrated in Fig. 3.5b, presents approximately 1.4 kW of core and winding losses under nominal operation. The larger surface area of the PTF offers an important advantage for dissipating the heat, even without forced air flow. Payton claims a thermal resistance as low as 0.5 ^{o}C/W [117].

Although HiMAG claims accurate inductance values, most available PTFs are produced with an ±25% primary inductance tolerance. Payton reduces the tolerance to ±10% and ±20%, depending on the model. The most probable cause of these relatively high tolerances is the ferrite material used and not the planar windings themselves. Cores even from the same batch can present large tolerances to the relative permeability μ_r (or μ_e), which translates to a large inductance deviation. Cores with proper properties should be used, typically found in the datasheet of each manufacturer, in conformity with IEC 62358. Another possible point that can introduce inaccuracies, is the air-gap created between the two-part core. This effect can be minimized by carefully handling the core and consistent tightening the outer shell. In

any case, these inaccuracies are present in both conventional and planar designs and further research on these issues is mandatory.
To summarize, planar magnetics:

1. Offer low profile, preferable for certain applications.
2. Are the default solution for wireless or inductive power transfer and wireless charging, regardless of the power level.
3. Offer better thermal characteristics, due to larger surface area.
4. Can be produced without the need of specialized winding equipment.
5. Hold easily predictable electrical characteristics, repeatable for an arbitrary amount of windings, due to the well-defined geometry.
6. Offer high degree of integration on power PCBs, where the default copper height of 35-70 μm offers reduction of HF losses (and R_{AC}), leading to high-efficiency figures, for frequencies up to 3.5 MHz.

PWs are also accompanied by some restrictions in the design and usability. As the current increases, so does the necessary width for the conductor, leading to larger occupied area or less turns. Increasing the frequency beyond a certain point (that depends on the height of the trace) increases the resistance (R_{AC}). This can be partially compensated with proper planning of the layer stack, as presented in detail in [118, 119].

Furthermore, the construction of a three-phase inductor or transformer requires good planning, and in the case a core is utilized, a custom order must be made [120]. To avoid the extra cost that custom-made ferrites introduce, off-the-shelf parts can be used. In [118] and [121] this is shown for single-phase windings, but it is easy to adjust to the three-phase case.

Due to the close proximity of the conductors and especially in multilayer topologies, the parasitic (stray) capacitance is not negligible. Various methods of dealing with this issue have been developed, mainly by introducing thicker dielectric material with lower ϵ_r and by designing the two layer with a slight offset, so that there in no symmetry in the z-axis [119, 122, 123, 124, 125]. This technique can also increase the insulation level of the winding. An online experimental method of estimating the parasitic capacitance is proposed in [126].

Other studies [127] propose methods of exploiting the parasitic capacitance of the planar windings as an integrated series capacitor for resonant converters. By leaving the stacked layers of the transformer open-ended, the capacitance that is developed between them can act as a part of the resonant circuit for frequencies up to hundreds of kHz. The same technique is possible for planar transformers, meaning that it is possible to integrate the whole LLC resonant circuit and isolation in one device.

Despite the fact that many transformers and inductors are available in the market, some times it is quite difficult to find magnetic components that can handle the desired application

requirements. For example, as it will be discussed in a later chapter, it is difficult to find inductors for HF AC applications, even from global distributors like Mouser. For those cases, a custom design can be deployed, as long as there are methods to determine the inductance and the margins of good operation of the components.

An exploration of the effects of the geometrical parameters, and a fast, simple and accurate estimation of the inductance for rectangle-shaped, single- and multi-layer windings is crucial and has not been fully-explored in the literature. The main focus of the vast majority of the papers is regular-polygon shaped windings (spirals, squares, hexagonals etc.), and mostly single-layered. When rectangular and multilayer windings are discussed, there are arbitrary assumptions for the estimation of the inductance, without any simulation or experimental verification. Others attempt to approach the estimation problem with analytical solutions, resulting in piecewise, difficult to use equations, which require exact knowledge of several electrical and mechanical parameters of the winding.

There is a need for simple and accurate equations, that rely only on the geometrical parameters and have relatively high tolerance on the inaccuracies that are introduced during the manufacturing process. This can enable the better utilization of the available space, effectively address the potential disadvantages of planar windings and set the basis for optimization techniques.

3.1.3 Structure and Contributions

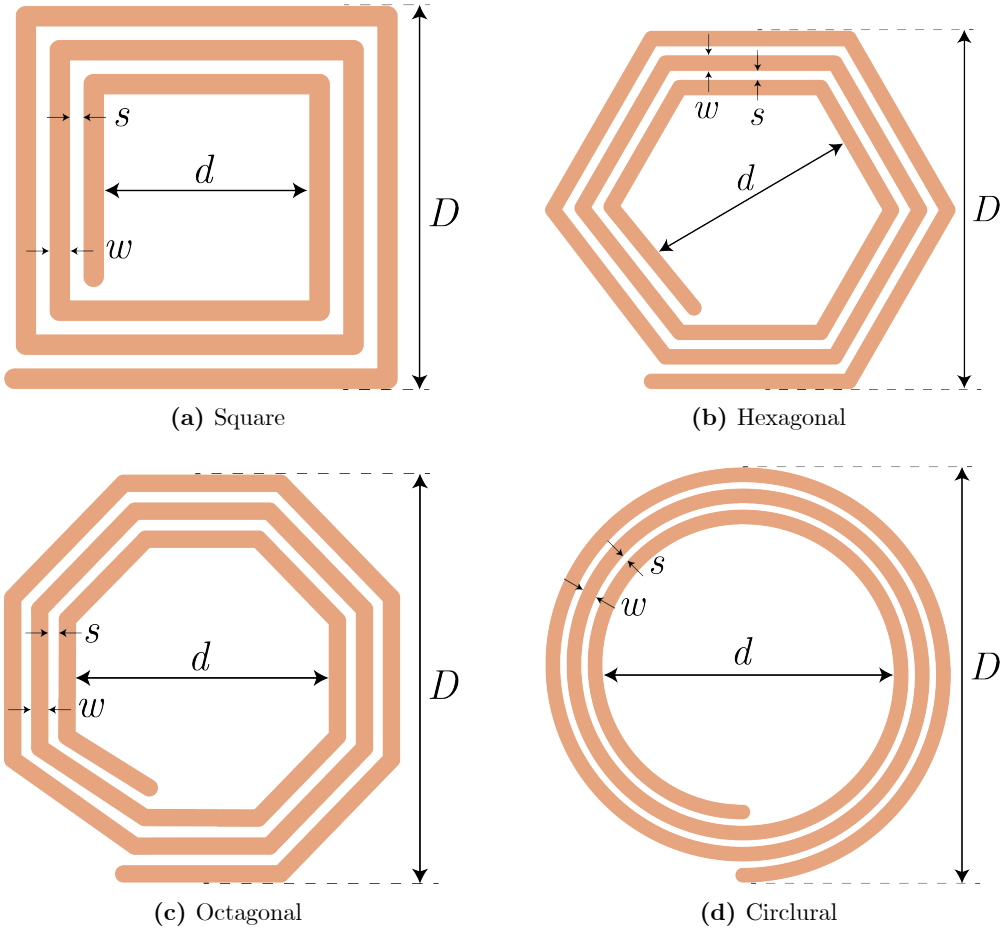
In this chapter, the design process and dimensioning of the rectangle-shaped single- and multi-layer planar windings is presented, adding one more degree of freedom to the design. Three established equations, namely Wheeler's, Rosa's and the Monomial, as they are collectively presented in [59] for square-shaped windings, are utilized and modified in order to be able to estimate the inductance of air-core single-layer rectangle-shaped windings. The inductance per turn is approximated, providing insight to the voltage distribution and the required distance between two consecutive turns. The accuracy of these estimations is evaluated also by experimental measurements.

Furthermore, additional modifications are examined to estimate the inductance of multilayer rectangular windings. A novel monomial-like equation is derived, via multiple linear regression (MLR) with approximately 6,000 samples, minimizing the error between the estimation equation and FEM simulations, and providing accurate results. This enables the use of optimization algorithms, aiming for maximizing the inductance or minimizing the geometrical dimensions of the winding. The accuracy of the new equation is also evaluated via laboratory measurements. A comparison is made between the modified and the new equations for windings up to 4 layers. The selection of a ferrite core is discussed along with the effects it has on the winding.

Publications:

- T. Papadopoulos and A. Antonopoulos, "Inductance Estimation for High-Power Multilayer Rectangle Planar Windings," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, under review.
- T. Papadopoulos and A. Antonopoulos, "Extension of Simple and Accurate Inductance Estimation for Rectangular Planar Windings," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, doi: 10.1109/JESTIE.2023.3276349.
- T. Papadopoulos and A. Antonopoulos, "Inductance Estimation for Square-Shaped Multilayer Planar Windings," *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, Hanover, Germany, 2022, pp. 1-10.
- T. Papadopoulos and A. Antonopoulos, "Formula Evaluation and Voltage Distribution of Planar Transformers Using Rectangular Windings," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. 1-10, doi: 10.23919/EPE21ECCEEurope50061.2021.9570558.

3.2 Single-Layer Planar Winding



(a) Square **(b)** Hexagonal

(c) Octagonal **(d)** Circlural

Figure 3.6 Typical layouts of planar windings and the geometrical characteristics.

Planar windings were first introduced as single layer coils of regular-polygon shapes (square, hexagonal, octagonal, circle), as illustrated in Fig 3.6. The applications were mainly RF-oriented, operating in the MHz region. With the recent developments in power electronics and the need for high-efficiency high-power-density converters, as well as the ongoing interest on WPT, more PW designs have been adopted for power applications, in the frequency range of 50 kHz to 5 MHz.

3.2.1 Geometrical Characteristics and Design of Regular-Polygon Shapes

For the regular polygon shapes, many equations have been proposed in literature, and are collectively presented in [60], namely Bryan, Wheeler, Greenhouse, Grover, Rosa, Cranin, and Terman. Most of the equations are derived to estimate the inductance of RF designs incorporating integrated circuits (ICs) and RFID and telemetry antennas.

Table 3.1 Coefficients for Wheeler, Rosa and the Monomial Equations [59]

Layout	Square	Hexagonal	Octagonal	Circular
K_1	2.340	2.330	2.250	-
K_2	2.750	2.820	3.550	-
c_1	1.270	1.090	1.070	1.000
c_2	2.070	2.230	2.290	2.460
c_3	0.180	0.000	0.000	0.000
c_4	0.130	0.170	0.190	0.200
α_0	1.620	1.280	1.330	-
α_1	-1.210	-1.240	-1.210	-
α_2	-0.147	-0.174	-0.163	-
α_3	2.400	2.470	2.430	-
α_4	1.780	1.770	1.750	-
α_5	-0.030	-0.049	-0.490	-

A comparative study between Crol, Ronkainen, Wheeler, Rosa, Jenei and the Monomial equations, suitable for estimating the inductance of RF square-shaped PWs, is presented in [128]. Rosa (referred in [59] as current sheet approximation) provides the most accurate results regarding RF ICs, while the Monomial presents margins for improvement.

In the context of this work, three equations are discussed, namely (i) the empirical Wheeler's equation, which was originally presented for single-layer helical coils [58], and was later modified to also estimate the inductance of other regular polygon layouts [59], (ii) Rosa's equation [86], which was derived by the current-sheet approximation, and (iii) the Monomial equation [59], which was derived by multiple linear regression from a dataset of approximately 19k samples. The equations are collectively presented in [59] and are:

$$L_{\mathrm{WH}} = K_1 \mu_0 N^2 \frac{\frac{D+d}{2}}{1 + K_2 \frac{D-d}{D+d}}, \tag{3.1}$$

$$L_{\mathrm{RS}} = \frac{c_1}{2} \mu_0 N^2 \frac{D+d}{2} \left(\ln\left(\frac{c_2}{\frac{D-d}{D+d}} \right) + c_3 \frac{D-d}{D+d} + c_4 \left(\frac{D-d}{D+d} \right)^2 \right), \tag{3.2}$$

$$L_{\mathrm{MN}} = \alpha_0 \cdot 10^{-3} D^{\alpha_1} w^{\alpha_2} \left(\frac{D+d}{2} \right)^{\alpha_3} N^{\alpha_4} s^{\alpha_5}. \tag{3.3}$$

where D and d are the outer- and inner- side lengths, N the number of turns, w the width of the conductor and s the spacing between two consecutive turns. The values of each coefficient K_i, c_i, and α_i are presented in Table 3.1, with respect to the winding layout.

For the square-shape case, Eqs. (3.1), (3.2), and (3.3), can be rewritten as,

$$L_{\mathrm{WH}} = 2.34\mu_0 N^2 \frac{\overline{D}}{1+2.75\rho}, \tag{3.4}$$

$$L_{\mathrm{RS}} = \frac{1.27}{2}\mu_0 N^2 \overline{D} \underbrace{\left(\ln(2.07/\rho) + 0.18\rho + 0.13\rho^2\right)}_{\Lambda(\rho)}, \text{and} \tag{3.5}$$

$$L_{\mathrm{MN}} = 1.5428\mu_0 N^{1.78} \overline{D}^{2.4} D^{-1.21} w^{-0.147} s^{-0.03}. \tag{3.6}$$

where $\overline{D} = \frac{D+d}{2}$ and $\rho = \frac{D-d}{D+d}$. It can be noted that in [59], the geometrical parameters of the Monomial are in mm and the resulting inductance in nH. Eq (3.6) as it appears here has been modified in order to be in SI units. The first term of 1.5428 has been rounded up from 1.542784.

Various observations can be made from (3.4), (3.5), and (3.6) regarding the behavior of the inductance. As expected, the inductance increases with the square of the number of turns N, except for the Monomial equation, where the coefficient is slightly lower. All equations include a relation to the average side length term $\overline{D} = (D + d)/2$: a proportional in the first two cases, and an exponential increase in the third case. This term can be considered a byproduct of the current sheet approximation: traces that run along one direction share a positive mutual inductance with the ones conducting current in the same direction (and are on the same side of the winding). Negative mutual inductance is developed among traces of the opposite sides (conducting current in the opposite direction). Determining the mutual inductance among conductors on the opposite sides of the winding requires the arithmetic mean distance between the two groups, hence, this term appears. Traces that are perpendicular to each other have zero mutual inductance [86, 87].

The filling factor ρ, which represents the amount of free space in the center of the winding, appears in (3.4) and (3.5). If D is kept constant, the ratio ρ decreases as d increases. For two windings with the same D and N, the one with the greater d is expected to have greater inductance, since its turns are concentrated closer to the outer side, have slightly greater length, and interact more efficiently with their adjacent turns, concluding in higher mutual inductance. Small filling factor can also accommodate for an EI or EE ferrite core, further increasing the inductance and drastically reducing the EMI, by restricting the magnetic field inside the core. According to (3.4), where ρ appears in the denominator, increasing d increases the inductance. A similar behavior can be observed in (3.5): As $\rho < 1$, the term $\Lambda(\rho) = \ln(2.07/\rho) + 0.18\rho + 0.13\rho^2$ increases with increasing d, as the $(\ln(2.07/\rho))$-term is stronger than $(0.18\rho + 0.13\rho^2)$-term.

In the Monomial approximation, D appears in both the numerator and the denominator. Since the exponent of the first is larger than the second, the total inductance tends to increase with D. On the contrary, the total inductance decreases as the width of the trace w and the

spacing between the turns s increase, but almost insignificantly. More specifically, the effect of s can be neglected, since it is raised to a power of almost zero.

In conclusion, the inductance increases with N, D, and d, which means that for any magnetic component where high inductance is desirable, these terms must receive their greatest possible values. It must be noted that these parameters are not fully-independent: D and N can be considered independent, although restricted by the physical-dimension limitations. The parameters w and s are dictated, however, by the nominal current and voltage of the winding, respectively. The IPC standards 2221, 2222 and 2152 describe the minimum trace width on a rigid PCB as a function of the nominal current and the temperature rise ΔT, as well as the minimum separation between two traces with a specific voltage difference ΔV. The necessary voltage difference between adjacent turns in PWs is discussed in the next subsection.

Considering the above, d is dependent on the aforementioned parameters, as in

$$d = D - 2N(w + s) - 2s. \tag{3.7}$$

In typical designs, w is larger than s by one order of magnitude, thus $2N(w+s) \gg 2s$, which means that for given values of N and D, d is strongly dependent on the sum $(w + s)$. A fast design process can be based on the geometrical parameters of the winding, matching the needs of each specific application.

3.2.2 Rectangular Shape

Contrary to regular polygons, rectangle-shaped planar windings (RPWs) can extend to the xy-plane by different lengths in each direction, offering one more degree of freedom and greater flexibility to the designer, as it is illustrated in Fig. 3.7. This allows for better use of space for both embedded and discrete planar magnetics. Furthermore, most off-the-shelf core shapes (I, UI and EI) are not symmetrical but extend more in one axis, making RPWs a better match.

The estimation of the inductance in RPWs cannot be done by the equations of subsection 3.2.1. Greenhouse proposes a method in [129], which estimates the mutual inductance of parallel traces and the total inductance of the winding, for relatively small dimensions (order of μm). In [61] an equation for estimating the inductance of considerably larger RPWs (order of mm) is proposed, for RFIC and RFID applications with frequencies in the order of MHz. However due to its complexity it is hard to utilize and requires strictly determined values for the geometrical parameters.

Inventing equations as simple as (3.4) - (3.6) for estimating the inductance of RPWs would be desirable. As [121] indicated, by using some form of mean value of the two outer-side lengths D_1 and D_2 can be used to replace the variable D. Also, in [62] the GeoMetric Mean Value (GMMV) of the outer-sides D_1 and D_2 is utilized and substituted in Rosa equation,

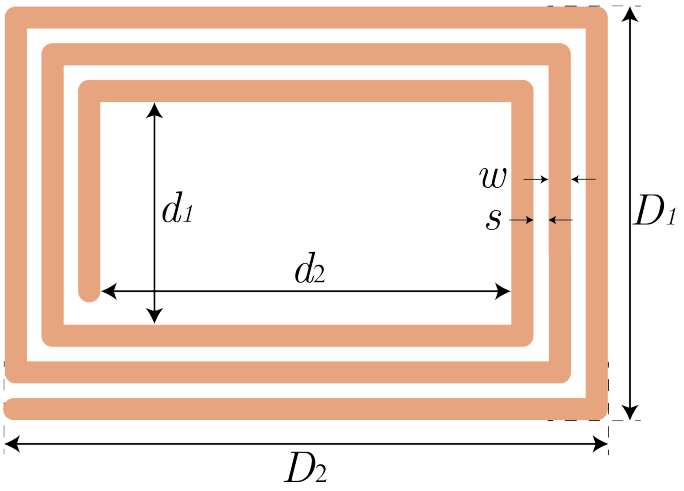


Figure 3.7 Geometrical parameters of rectangle-shaped planar windings.

in order to estimate the inductance of a single-layer RPW. However, no further explanation is given, other than the GMMV occupies the same surface area as D_1, D_2 do. Furthermore, no other solution is discussed and the estimation error is not considered.

A thorough search for the mean value which minimizes the estimation error can be conducted by employing the generalized mean value. By creating a large dataset of windings with different geometrical characteristics and knowing (or simulating) the respective inductance, it is possible to modify each equation to provide accurate results for RPW designs.

3.2.2.1 Generalized Mean Value (GMV)

The generalized Mean Value (GMV) of Power Mean (PM) is defined as

$$\mathrm{GMV}_p(\vec{x}) = \|\vec{x}\|_p = \left(\frac{1}{N} \sum_{i=1}^{N} x_i^p \right)^{\frac{1}{p}}, \tag{3.8}$$

where $\vec{x} = [x_1, x_2, \ldots, x_N]$ is a vector of dimensions $N \times 1$, and p is the p-norm of $\vec{x}$. For the case of $p = 0$, the GMV becomes the well-known geometric mean value (GMMV), as in

$$\mathrm{GMV}_0(\vec{x}) = \|\vec{x}\|_0 = \left(\prod_{i=1}^{N} x_i \right)^{\frac{1}{N}}. \tag{3.9}$$

Other well-known and widely used p-norm examples include:

- $p \to -\infty$: the minimum value,
- $p = -1$: the harmonic mean value,
- $p = 0$: the geometric mean value,
- $p = 1$: the arithmetic mean value,

- $p = 2$: the root-mean-square value,
- $p \to \infty$: the maximum value.

For a two-component vector $\vec{x}_{1\times2}$, as is the one composed by two independent outer-side lengths D_1 and D_2, (3.8) becomes

$$\mathrm{GMV}_p(D_1, D_2) = \|D\|_p = \left(\frac{1}{2}\left(D_1^p + D_2^p\right)\right)^{\frac{1}{p}}, \tag{3.10}$$

and (3.10) for $p = 0$

$$\mathrm{GMV}_0(D_1, D_2) = \|D\|_0 = \sqrt{D_1 D_2}. \tag{3.11}$$

3.2.2.2 Dimensions of the Windings and Simulation Setup

The physical dimensions of high-power planar windings vary from a few mm to a few hundred mm. In the context of this investigation the outer side dimensions vary from 100 mm to 210 mm, close to one side of the A4 paper size, a PCB size widely available and relatively cheap.

The width of the trace w is determined by the IPC-2221/2 and IPC-2152 standards, using as parameters the maximum current and the acceptable temperature increase ΔT in the copper. The placement of the traces on external or internal PCB layers must be considered, as the ones enclosed inside the FR-4 can dissipate less heat, hence for a given ΔT they can carry less current. The width varies from 3 mm to 5 mm, which for a copper height of 35 µm can handle between 5 A and 7 A, for a ΔT of 10^oC, according to SaturnPCB [96] which follows the IPC-2152 standard. By relaxing the restriction of $\Delta T = 10^o$C, higher current handling capability is possible.

Similarly to the above procedure, the spacing between two adjacent turns s is determined using the IPC standards. In this study, spacings from 0.1 mm to 2 mm are considered, which correspond to a voltage difference ΔV from 15 V to 400 V. These values are valid for external uncoated conductors (B2) and can be greatly increased for external coated conductors (B4). The dimensions of the simulated windings are presented in Table 3.2. It shall be kept in mind that the voltage is not following an equal distribution on each turn, but tends to concentrate more on the first few external turns, as it will be discussed in subsection 3.2.3.

It should be noted that the proposed width of a trace when considering the current capability and the temperature increase, works under the assumption that the trace has sufficient distance to any other trace. A design with small s can lead to considerably larger temperatures. In that case, a low-profile heat sink may be considered.

The number of turns N vary from 6 to 10 in order achieve two main goals: Firstly, to reach values for the coreless winding inductance in the the order of a few µH, which can be further increased to a few mH with the introduction of a core, and secondly, to achieve a

Table 3.2 Dimensions of Simulated RPWs

Variable	Values
D	[110:10:210] mm
w	3, 4, 5 mm
s	0.1, 0.5, 1, 2 mm
N	6, 8, 10 turns

relatively large d, which not only increases the inductance, but offers a central aperture to accommodate a proper core leg.

The orientation of the winding is irrelevant, hence for a pair $\{D_1, D_2\}$ only one combination is considered. Furthermore, some combinations of D, w, s, and N are impossible to implement as they conclude to a $d < 0$ and therefore are neglected. The combinations of the aforementioned parameter values constitute a large dataset, which, excluding the duplicate pairs and the impossible setups, contains 2633 samples.

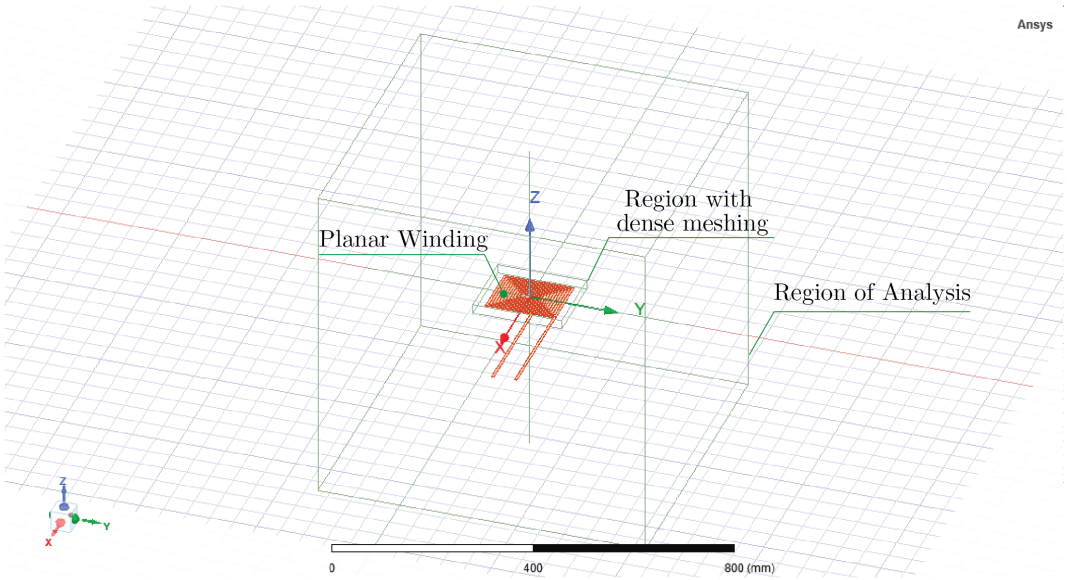
The region of analysis is defined by a cube with fixed sides of 700x700x700 mm^3, applying a solution region cut-off technique which contains the vast majority of the magnetic flux. The generated tetrahedras (Tets) are smaller near and between the copper traces, and become larger as they extend towards the boundaries of the analysis region, as it is illustrated in Fig. 3.8. On average, 40,000 Tets are generated, 36,000 on the empty space and 4,000 on the coil. The geometrical parameters D_1, D_2, N, w, and s are defined as parameters which can change easily, to facilitate a repetitive simulation process. The energy error and delta energy were set to 1%, as an acceptable compromise between accuracy of the model and its runtime. The excitation current was set to 1 A peak sinusoidal wave with a frequency of 100 kHz.

3.2.2.3 Optimization and Assessment Criteria

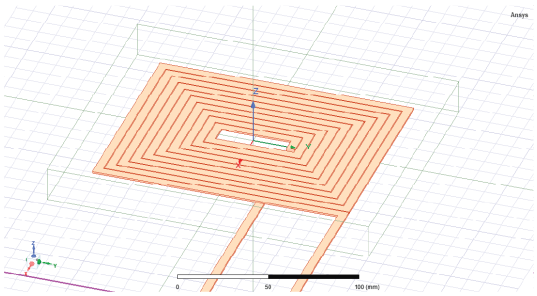
Provided a dataset of $L_{\text{sim}} = f(D, N, w, s)$, an optimization algorithm is required in order to find the optimal parameter p that will provide the best possible results. The function used for this optimization is

$$\text{SSE}(p) = \sum_{i=1}^{S} \left(L_{\text{sim},i} - L_{\{\text{WH,RS,MN}\},i}(p)\right)^2, \tag{3.12}$$

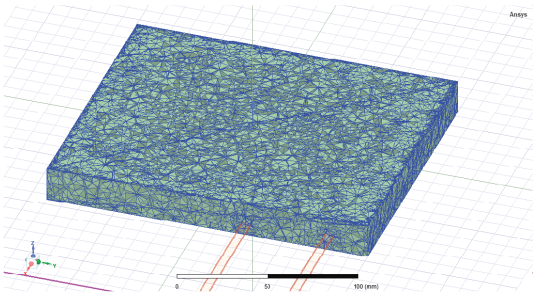
where S is the total population of the selected dataset and i is a single sample. The term $\left(L_{sim,i} - L_{\{\text{WH,RS,MN}\},i}(p)\right)^2$ is the Squared Error (SE) between the respective equation and the simulation results. The Sum of Squared Errors (SSE) represents the sum of these errors for the entire dataset. For different p-values, there is a different combination of D_1 and D_2 substituted in (3.4)-(3.6), creating different estimation results, indicating different levels of



(a) Ansys Maxwell3D window.



(b) An rectangle-shaped PW.



(c) Meshing around the winding

Figure 3.8 The simulation setup for the planar windings. The region is set to 700x700x700 mm and a subregion is defined for a more dense and accurate FEM analysis.

accuracy for each estimation. The parameter p is selected to vary in a range from $[p_{min}, p_{max}]$ with a fixed step increment. The steps of the algorithm are the following:

i. define dataset,
ii. $p = p_{\min}$,
iii. calculate $\|D\|_p$ and d from (3.7) ,
iv. calculate L_{WH}, L_{RS}, and L_{MN} from (3.4)-(3.6),
v. calculate $\mathrm{SE} = (L_{sim,i} - L_{\{\mathrm{WH,RS,MN}\},i}(p))^2$ for each sample i, and SSE for the entire dataset from (3.12),
vi. $p \leftarrow p +$ increment,
vii. if p in range $[p_{\min}, p_{\max}]$ return to (iii.), otherwise continue,
viii. find minimum SSE and corresponding p_{opt}.

The equivalent inner side length d in step (iii.), can either be found from (3.7), or from $\|d\|_p = \mathrm{GMV}_p(d_1, d_2)$. The second way does not offer any significant improvement in the results and will not be considered in the following.

The optimization algorithm performs an exhaustive search for the optimal p in the predetermined space $[p_{\min}, p_{\max}]$, which is set to $[-5, 5]$ with a step size of 0.001. For each p, the SSE is calculated as in (3.12) and the $\min|\text{SSE}(p)| = \text{SSE}(p_{\text{opt}})$ is found. In order to illustrate the results, either

$$E_p = \sqrt{\frac{\text{SSE}(p)}{S}} \tag{3.13}$$

or

$$\text{MAE}_p\% = \frac{1}{S}\sum_{i=1}^{S}\frac{|L_{sim,i} - L_{\{\text{WH,RS,MN}\},i}|}{L_{sim,i}} \cdot 100 \tag{3.14}$$

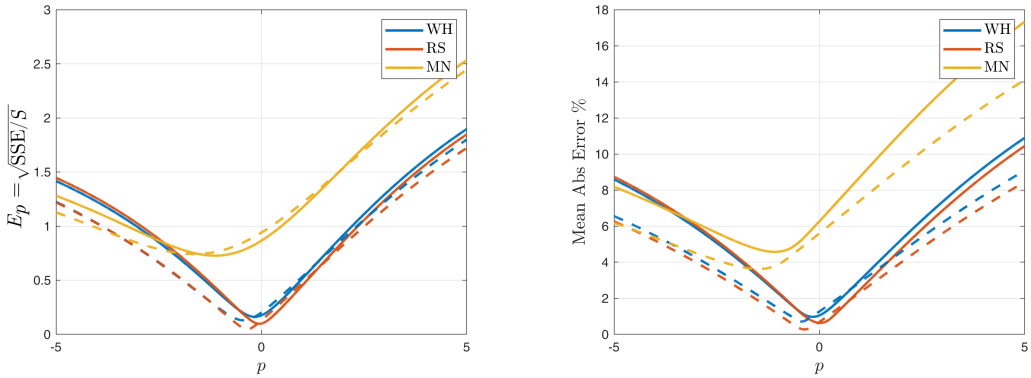
can be used. Eq. (3.13) essentially presents the RMS error between the simulation results and the equation approximation. While the SSE(p) value is H^2 and does not have any significant physical meaning, E_p presents the root of mean squared error for every sample in a given dataset, measured in µH. Equivalently, the results can be illustrated by (3.14), which is dimensionless, but presents the mean absolute error as a percentage, using the simulated inductance result as reference value. While p_{opt} will be selected based on the minimization of E_p, the results will be presented based on MAE_p, as a normalized value is more effective in visualization. The two metrics may results in slightly different p_{opt}, but the difference is negligible.

3.2.2.4 Selection of Optimal p-norm

To easily categorize each dataset, their names represent the parameters that remain the same throughout the optimization process. For example N8w4 represents a dataset, which has a constant number of $N = 8$ turns and traces with $w = 4$ mm width, while all other parameters vary according to the specifications given in Table 3.2.

All datasets present one global minimum (for the search region) with regard to p, as illustrated in Fig. 3.9, where the continuous lines represent the E_p and MAE of all simulated windings, and the dashed lines the respective values for a single subset (N10w5). The latter is illustrated only as an indicative case; all subsets behave similarly, with a global minimum around 0 for (3.4) and (3.5) and around -1 for (3.6).

The Monomial seems to have a slightly different behavior compared to the other two equations, as its MAE is significantly higher for positive p values, and presents the optimal p in a different area. This can be mainly attributed to the coefficient values shown in (3.6), which are derived using a linear regression algorithm for a specific dataset of planar inductors, targeting RF applications. It should be noted that it is possible to recalculate its coefficients, based on the given dataset of Table 3.2, in which case, the behavior is more similar to these of Wheeler and Rosa, which is discussed in Section 3.4.



(a) **(b)**

Figure 3.9 Metrics with respect to p for N10w5 (dashed line) and all samples (continuous line), for each equations. The optimal p_{opt} depends on the specific dataset but all lines present a global minimum, in the neighborhood of 0 for Wheeler and Rosa, and of -1 for the Monomial.

Table 3.3 summarizes ten dataset categories with the corresponding p_{opt} and the MAE%, for each equation separately. One observation that can be made for Wheeler's and Rosa's equations is that as N or w increases, p_{opt} decreases by a small amount, but generally is located in the neighborhood of 0 ± 0.45. For the entire dataset of simulated windings, p_{opt} is at -0.16 and -0.05, respectively. The MAE is less than 1.2 % and 0.7 % for the first and second equations, respectively, values that are within the simulation accuracy. The maximum error observed in the whole dataset for a single simulated winding is 7.2% for these two equations.

The Monomial, however, does not present a consistent trend regarding the p_{opt}, with respect to N and w. Furthermore, its estimation is less accurate compared to the other two equations. Its p_{opt} is also located elsewhere, i.e., in the neighborhood of -1.25 ± 0.25, and the MAE is in the range of 3.5% - 5%.

In order to simplify the calculations for the the inductance estimation, integer p values are preferred, namely $p = -1$ as the optimal p for the Monomial, $p = 0$ as the optimal p for Wheeler's and Rosa's equations, and $p = 1$ as the most intuitive value (arithmetic mean) which can be used in the context of RPWs. The results for these values of p are presented in Table 3.4. For Wheeler's and Rosa's equations the $\text{MAE}_{p=0}$ is very close to that of $\text{MAE}_{p=p_{\text{opt}}}$ of each individual case, as it is expected, and in any other case is less than 5 %. Similarly, the Monomial $\text{MAE}_{p=-1}$ is close to $\text{MAE}_{p=p_{\text{opt}}}$, but $p = 0$ still provides relatively accurate results. Eqs (3.4) - (3.6) can be modified as

Table 3.3 MAE% and p_{opt} for different datasets

Dataset[a]	WH		RS		MN	
	p_{opt}	MAE%	p_{opt}	MAE%	p_{opt}	MAE%
N6w3	0.446	1.18	0.209	0.36	-1.170	4.89
N6w4	0.160	0.54	0.214	0.34	-1.198	4.95
N6w5	0.018	0.38	0.172	0.61	-1.211	4.86
N8w3	0.004	0.81	0.080	0.42	-1.080	4.59
N8w4	-0.170	0.74	-0.011	0.43	-1.104	4.32
N8w5	-0.267	0.69	-0.129	0.53	-1.201	4.09
N10w3	-0.233	1.06	-0.085	0.60	-1.008	4.00
N10w4	-0.348	0.86	-0.212	0.40	-1.142	3.66
N10w5	-0.437	0.71	-0.346	0.28	-1.532	3.50
All Data	-0.162	0.97	-0.049	0.63	-1.130	4.58

[a] This column illustrates the parameters that remain constant and their respective values. For example N8w4 represents a dataset which has a constant $N = 8$ turns and $w = 4$ mm, while all other parameters vary.

Table 3.4 MAE% for $p = -1$, $p = 0$ and $p = 1$ for different datasets

	$p = -1$			$p = 0$			$p = 1$		
	WH	RS	MN	WH	RS	MN	WH	RS	MN
N6w3	3.22	2.42	5.16	1.43	0.62	6.49	1.82	1.86	8.63
N6w4	2.49	2.75	5.20	0.57	0.69	6.70	2.07	1.83	9.05
N6w5	2.40	3.12	5.09	0.38	0.86	6.80	2.53	2.09	9.37
N8w3	2.21	2.35	4.80	0.82	0.43	6.28	2.81	2.38	8.68
N8w4	2.15	2.47	4.50	0.90	0.44	6.29	3.54	2.73	9.02
N8w5	2.14	2.32	4.25	0.09	0.60	6.33	3.72	2.97	9.11
N10w3	2.10	2.14	4.17	1.43	0.68	5.88	4.01	3.17	8.61
N10w4	1.90	1.78	3.80	1.45	0.73	5.73	3.95	3.15	8.34
N10w5	1.44	1.12	3.87	1.27	0.68	5.60	2.91	2.34	7.43
All Data	2.27	2.33	4.58	1.05	0.63	6.27	3.03	2.50	8.75

Table 3.5 Simulation and Experimental Results

Sample	Dimensions							
	D1 [mm]	D2 [mm]	N	w [mm]	s [mm]	Sim [uH]	Lab [uH]	Er. %
#1	100	150	6	4	0.1	6.159	6.174	0.24
#2	100	163	8	4	0.5	8.369	8.402	0.39
#3	100	163	10	3	0.5	13.456	13.478	0.16
#4	210	266	6	5	1.0	14.553	14.396	-1.08
#5	210	297	10	5	0.5	32.122	32.015	-0.33

$$L_{\mathrm{WH}} = 2.34\mu_0 N^2 \frac{\|\overline{D}\|_0}{1 + 2.75\|\rho\|_0}, \tag{3.15}$$

$$L_{\mathrm{RS}} = \frac{1.27}{2}\mu_0 N^2 \|\overline{D}\|_0 \left(\ln\left(\frac{2.07}{\|\rho\|_0}\right) + 0.18\|\rho\|_0 + 0.13\|\rho\|_0^2 \right), \text{and} \tag{3.16}$$

$$L_{\mathrm{MN}} = 1.5428\mu_0 N^{1.78} \|\overline{D}\|_{-1}^{2.4} \|D\|_{-1}^{-1.21} w^{-0.147} s^{-0.03}, \tag{3.17}$$

where $\|\overline{D}\|_y = \frac{\|D\|_y + \|d\|_y}{2}$, $\|D\|_y$ is the y-norm of the outer sides D_1 and D_2, $\|d\|_y$ is the y-norm of the inner sides d_1 and d_2, which can be also calculated from (3.7) since the difference is negligible, and $\|\rho\|_y = (\|D\|_y - \|d\|_y)/(\|D\|_y + \|d\|_y)$. The modified equations (3.15)-(3.17) can be used directly, for windings within the specified dimensions or in the near vicinity.

It is interesting to investigate how accurate each approximation will be for the selected p values, when the outer lengths of the rectangle differ significantly. The deviation from the square shape can be expressed by the ratio D_1/D_2, and the MAE% for the selected p values is shown in Fig. 3.10, as a function of the D_1/D_2 ratio. For Wheeler's and Rosa's equations, the MAE% for $p = 0$ is significantly lower compared to that for $p = 1$ and $p = -1$, especially when the ratio is small. As it is expected and illustrated in Fig. 3.10, MAE% tends to decrease as the ratio increases, i.e., as the windings are getting closer to a square shape. The Monomial approximation does not show the same consistency in its behavior, however, it presents the lowest MAE% at $p = -1$, as expected from Fig. 3.9.

3.2.2.5 Experimental Results

Five indicative cases, presented in Table 3.5, are selected to be constructed and measured in the lab, in order to evaluate both the simulation results and the equations. The selected dimensions of three windings are within the scope of the simulations, as defined in Table 3.2, while two of them are intentionally outside the dataset used to evaluate the optimal p.

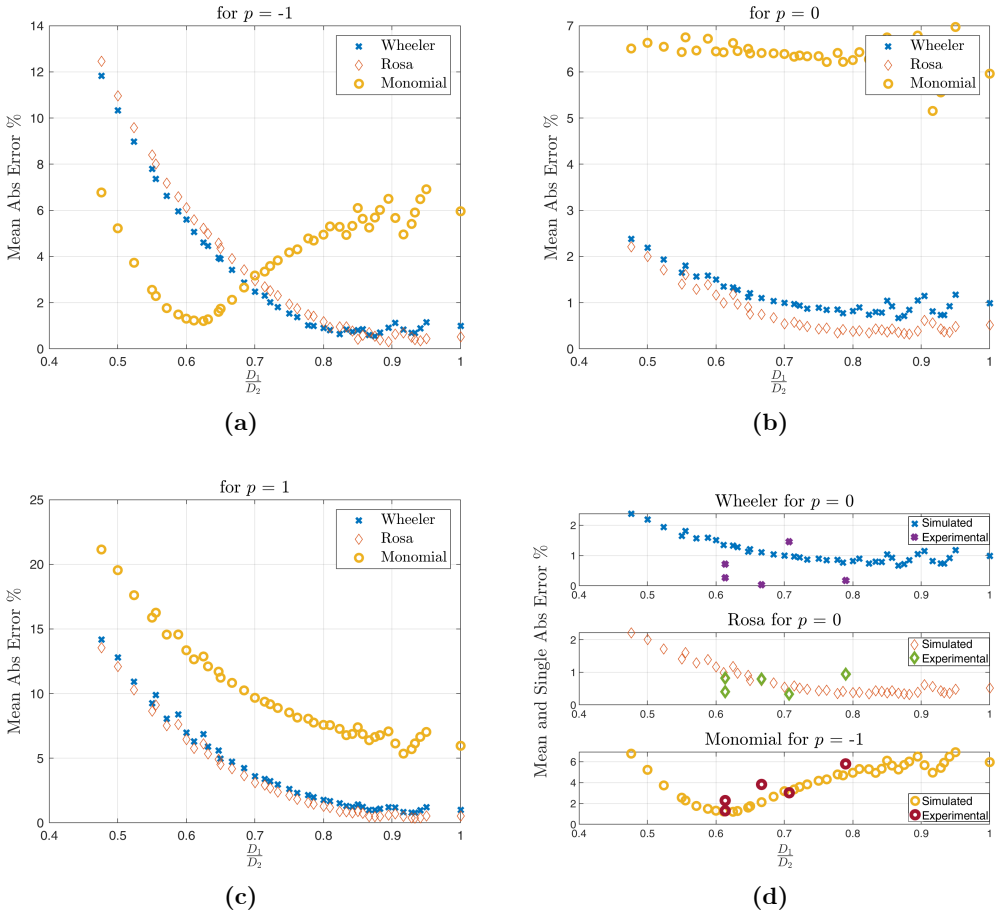
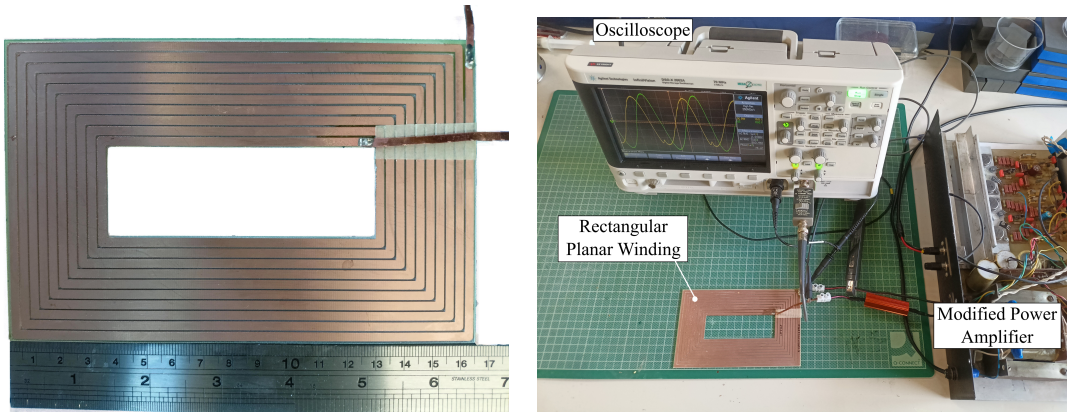


Figure 3.10 MAE % for as a function of the ratio D_1/D_2, which represents the deformation of the square shape. As D_1/D_2 increases, Wheeler's and Rosa's equation MAE decreases, while the Monomial does not present a consistent behavior. (d) presents the MAE% for the respective rounded p_{opt} of each equation, with the corresponding absolute error of the experimental vs. equation results.

A modified power amplifier is used, capable of producing 30 V peak voltage, with frequency up to 50 kHz and a current up to 1.5 A. The inductance is calculated by correlating the voltage excitation to the current response (amplitude and phase difference) at 50 kHz, and the experimental setup is presented in Fig. 3.11. The error between the simulation and the experimental results is less than 1.1%, and it is presented in Table 3.5, in order to evaluate the accuracy of the simulation results. The inductance is also verified with an HP 4284A precision LCR meter. It should be noted that since the self-resonant frequency of the winding is expected to be several orders of magnitude higher than the operating frequency, the inductance will not vary with respect to the latter (up to a reasonable operating frequency, e.g. 200 kHz).

The comparison between the equations and the experimental results is presented in Table 3.6, for the same windings, where the physical dimensions have been omitted. The error is less than 1.5% for Wheeler's and Rosa's equations and less than 5.5% for the Monomial,



(a) (b)

Figure 3.11 Experimental setup for measuring the inductance of RPWs using the amplitude and the phase difference of the voltage and the current.

Table 3.6 Equations and Experimental Results for the corresponding p_{opt} of each equation

Sample		Wheeler		Rosa		Mono	
	Lab [µH]	Ind. [µH]	Er. %	Ind. [µH]	Er. %	Ind. [µH]	Er. %
#1	6.174	6.145	-0.47	6.098	-1.25	6.464	4.49
#2	8.402	8.424	0.26	8.333	-0.83	8.223	-2.18
#3	13.478	13.575	0.71	13.424	-0.40	13.111	-2.80
#4	14.396	14.421	0.17	14.532	0.94	15.230	5.48
#5	32.015	32.479	1.43	32.155	0.44	32.984	2.94

even when considering windings with dimensions outside the initial dataset for which p is optimized. Furthermore, the same comparison is made, based on the ratio D_1/D_2, and as it can be seen in Fig. 3.10d, the absolute error between the measurements and corresponding equation follows the trend of MAE%. Note that the optimal p value is used for each equation, i.e., $p = 0$ for Wheeler and Rosa, and $p = -1$ for the Monomial, to produce the best possible results. The utilization of other p values is possible, but would increase the estimation error, especially in cases of small D_1/D_2, as shown in Fig. 3.10.

3.2.3 Voltage Distribution on each Turn

Due to the nature of PWs, each turn does not present the same inductance and hence experiences a different voltage drop. It is possible to use the equations (3.15)-(3.17) to estimate the inductance of each turn. Since the current that flows in every turn of the winding creates a magnetic field in the same direction, the inductance of each turn is given by

$$L_i = L_{1T,i} + \sum_{j=1, j\neq i}^{N} M_{ij}, \tag{3.18}$$

where L_i is the total inductance of the i turn, L_{1T} is the self-inductance of the i turn, and M_{ij} is the mutual inductance between the i turn and every other j turn.

The calculation of the self-inductance is straightforward, by utilizing any equation for the specific dimensions of the i turn with

$$\begin{aligned} D_{1T} &= D - 2(i-1)(w+s) \\ d_{1T} &= D_{1T} - 2w \end{aligned}, \tag{3.19}$$

for $i \in [1, N]$.

The calculation of mutual inductance requires additionally the knowledge of the inductance of turns i and j, connected in series, which can be approximated by

$$\begin{aligned} D_{2T} &= D - 2(i-1)(w+s) \\ d_{2T} &= D_{2T} - 2jw - 2(j-1)s \end{aligned}, \tag{3.20}$$

for $i \in [1, N-1]$, and $j \in [i+1, N]$.
Finally, the mutual inductance can be calculated from

$$M_{ij} = \frac{1}{2}(L_{2T,ij} - L_{1T,i} - L_{1T,j}), \tag{3.21}$$

and the total inductance of each turn L_i from (3.15). The steps of the algorithm are presented in Fig. 3.12. A comparison between the approximation algorithm and laboratory measurements is carried out to verify the accuracy of the process, and it is presented in Table 3.7.

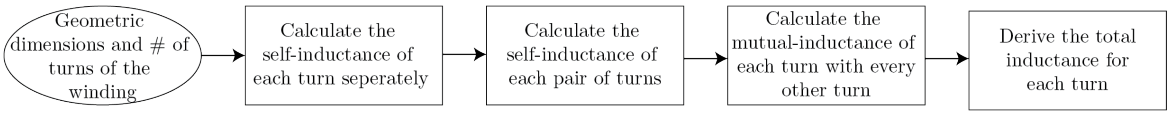


Figure 3.12 Flowchart of the proposed algorithm for calculating the inductance of each turn.

It can be noted that in both the estimated and measured results, the second turn presents greater inductance compared to the outermost (first), even though the surface area is smaller. The inductance of the third turn is also equal or greater of the outermost. This observation can be explained by considering the effect of the mutual inductance in combination with the surface area of each turn. The mutual inductance is significant between turns of long length, which are placed closed to each other. The exception is the first turn (outermost), which has no other turn surrounding it. From the fourth turn and inwards, the inductance rapidly declines.

Table 3.7 Laboratory and algorithm estimation results for 2 square- and 2 rectangle-shape coreless windings of 6 turns.

	Square						Rectangle					
	D = 185 mm			D = 210 mm			D1 = 266 mm D2 = 210 mm			D1 = 292 mm D2 = 210 mm		
	L [μH]			L [μH]			L [μH]			L [μH]		
Turn	Est.	Lab.	Er.%	Est.	Lab.	Er.%	Est.	Lab.	Er.%	Est.	Lab.	Er.%
1	1.26	1.31	-3.89	1.60	1.64	-2.50	2.43	2.44	-0.43	2.63	2.55	3.11
2	1.36	1.35	0.41	1.72	1.71	0.54	2.55	2.52	1.33	2.76	2.84	-2.82
3	1.31	1.35	-3.05	1.67	1.64	1.80	2.56	2.53	1.17	2.77	2.85	-2.62
4	1.13	1.07	5.31	1.50	1.40	6.67	2.46	2.41	2.03	2.67	2.70	-0.96
5	0.86	0.84	1.80	1.21	1.16	4.13	2.26	2.21	2.21	2.47	2.43	1.64
6	0.52	0.55	-5.77	0.82	0.84	-1.92	1.96	2.07	-5.61	2.16	2.11	2.14
Σ	6.44	6.48		8.52	8.39		14.22	14.18		15.47	15.48	

To explore in more depth this observation, in Fig. 3.13 the calculated and measured inductance per turn as a percentage of the total inductance is presented, based on the proposed algorithm. The geometrical characteristics of the winding are constant and equal to $D = 210$ mm, $w = 3$ mm, $s = 1$ mm. The number of turns N varies and consequently varies the inner-side length d. Changing the geometrical parameters would result in changes to the absolute values of the inductance distribution, but the fact that the inductance increases for the first few turns and then rapidly decreases, still stands true.

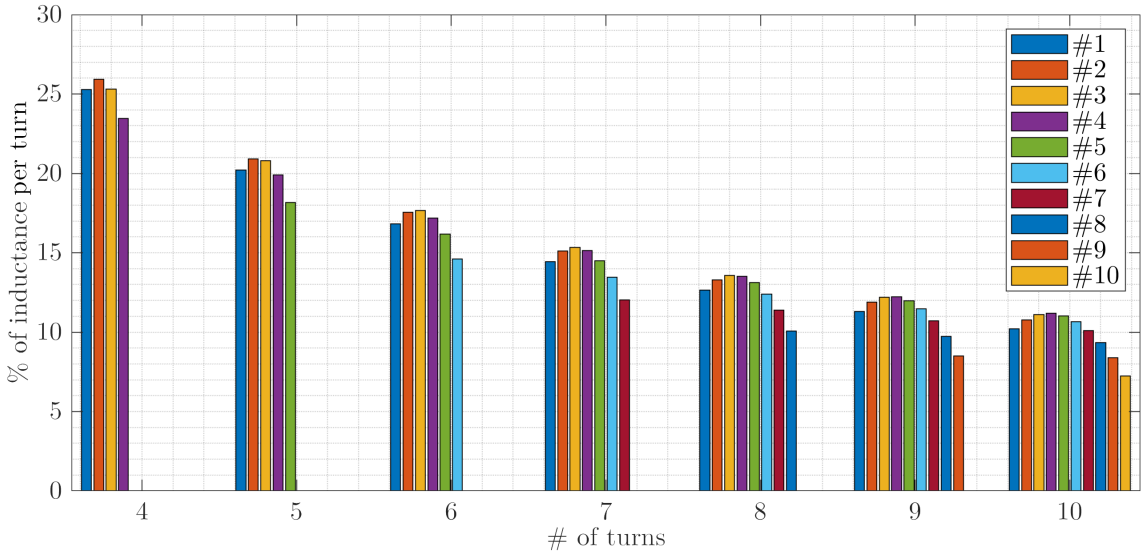


Figure 3.13 Inductance per turn as a percentage of the total inductance, for windings with different number of turns.

A repetitive process may be used when designing PWs, where in the first iteration the inductance for a specific set of geometrical parameters $\{\boldsymbol{D}_1, \boldsymbol{D}_2, \boldsymbol{N}, \boldsymbol{w}, \boldsymbol{s}\}$ is estimated, and the spacing between the first turns is validated as adequate or not. If the spacing cannot withstand the applied voltage, in the second iteration s increases, the other parameters $\boldsymbol{D}_1$, $\boldsymbol{D}_2$, or $\boldsymbol{N}$ are readjusted to comply with the desired characteristics of the windings and the new inductance is estimated. This process is repeated until the winding has the proper spacing and the desired inductance, as it is illustrated in Fig. 3.14. The width of the trace $\boldsymbol{w}$ is considered constant, as it depends on the maximum current passing through the winding. If it is not possible to achieve the desired inductance, while also comply with the geometrical restrictions of the application, multilayer planar windings should be considered.

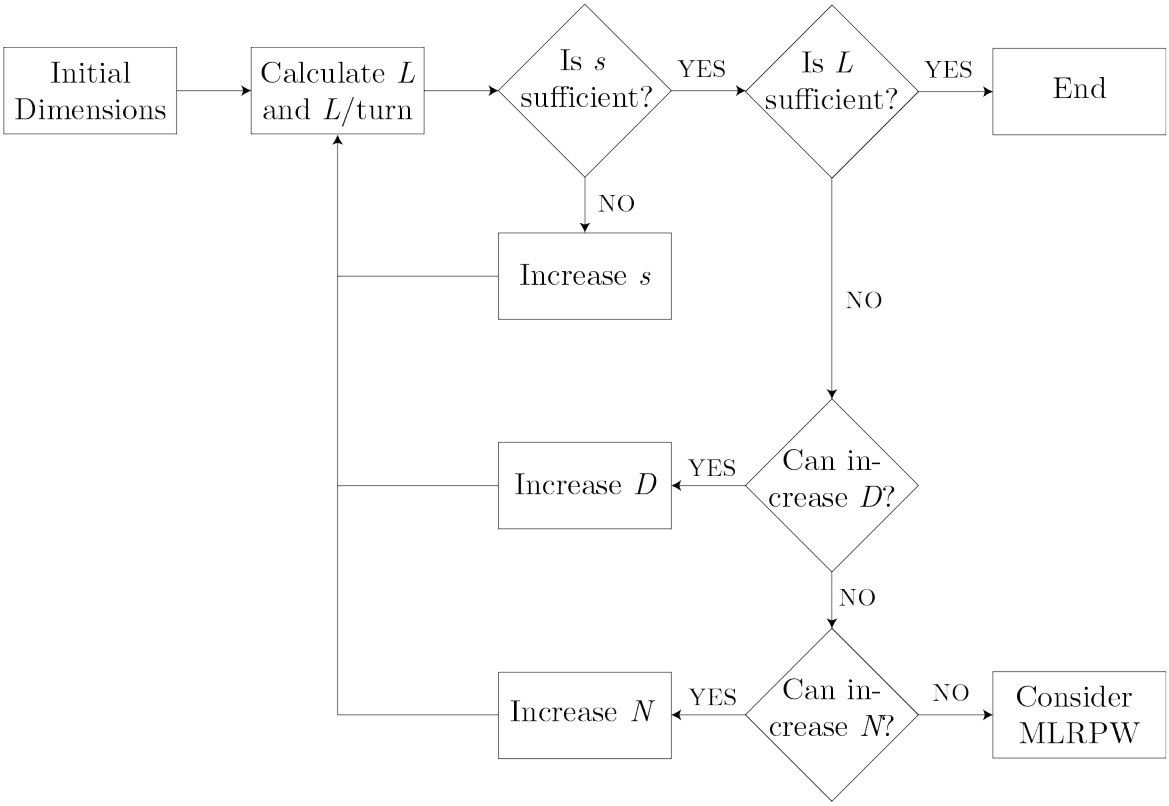


Figure 3.14 Design flowchart for an L1RPW.

In conclusion, for coreless designs, special considerations must be made for the spacing between each turn. Unlike conventional windings, in planar architectures, the voltage drop per turn is not simply given by the ratio of the applied voltage over the total number of turns. If the voltage distribution is not considered, it can lead to oversized windings or electrical breakdown between turns, most probably the outermost. It is important to ensure that the first turns are sufficiently far apart.

3.3 Multilayer Planar Winding

High-power PWs are generally designed with less turns, compared to conventional windings. However, via proper folding of similar single-layer windings, so that the magnetic flux of each layer is generated in the same direction, multilayer PWs (MLPWs) are possible. These designs can increase the inductance exponentially, while achieving a high coupling factor and maintaining the z-profile low. The utilization of multilayer rectangle-shaped PWs (MLRPWs) provides further benefits, by adding one more degree of freedom, which can be crucial for applications with limited space availability.

As in single-layer RPWs (L1RPWs), a simple and accurate method for estimating the inductance of MLRPWs is important. However, based on the current analytical equations of L1RPWs, a similar approach for MLRPWs, would result in a complex and inconvenient form difficult to use.

The utilization of Wheeler's and Rosa's equations, where the number of turn N is substituted by the product of number of layers (N_L) times the number of turns per layer (N_T), has shown promising results, but the estimation gets worse as the number of layers or the distance between them increases [130]. The Monomial equation, as it is presented in the previous section, provides worse results, but due to its form it is easily expandable to accommodate for the required additional variables.

3.3.1 Candidate Forms of Equations

The form of the new monomial-like equation should include all the geometrical parameters, which previous analyses have shown to have an impact on the resulting inductance of the winding. In this direction, a discussion on the single-layer winding monomial equation (3.6) or (3.17), would be useful to highlight the effect of each variable.

The variable that affects the inductance the most is the mean value of the perimeter of the winding $\overline{D} = \frac{D+d}{2}$, which is raised to 2.4. The importance of this parameter was already identified in the first estimation attempts [87]. It derives from the Current Sheet Approximation (CSA), where copper traces on the same side (being close to each other and carrying current in the same direction) create a strong positive mutual inductance. Accordingly, traces on opposite sides carry current in opposing directions, generating a negative mutual inductance. The strength of the negative mutual inductance decreases as the distance between the two sides increases, as for CSA the two sides of the winding can be regarded as two conductors with opposite currents. This reveals the important role of d when considering the total inductance of a winding.

The outer-side length D is present in the numerator (as a sum) raised to 2.4 and in the denominator raised to 1.21, hence the total inductance increases with D. The number of turns N also has a strong impact on inductance, as it is raised to 1.78. Therefore, the variables D, d and N play the most significant role in the determination of the total inductance.

The inductance decreases with the width of the copper w (raised to -0.147), since (with D and N constants) larger w results to smaller d. The impact of the spacing between traces s is almost negligible, at least for the dimensions this work considers. In practice, the spacing between the traces is not an important design issue for relatively low voltage, since a few μm of clearance, especially when coating is present, can isolate more than 100 V (IPC-2221B, B4 external conductors with polymer coating [96]).

In conclusion, as it is intuitively expected, larger external dimensions (larger D) increase the inductance. The inductance also increases by adding more turns (larger N) which, for a constant D, can be done either by decreasing w or d. In the first case the inductance will exponentially increase as long as d is kept approximately the same. However, reducing w may have adverse effects on the winding temperature, which will increase as well, since the same amount of current will run through a narrower trace. In case d is decreased it is uncertain if the inductance will increase, since $\overline{D}$ gets decreased (traces carrying currents in opposite directions get closer).

Based on the single-layer planar winding (L1PW) monomial equation and the analysis of its variables and coefficients, first of all, D and d need to be separated into D_1, D_2 and d_1, d_2, respectively, as presented in Fig. 3.7. In addition, two new parameters need to be introduced: the first is the number of layers N_L and the second is the vertical distance between two consecutive layers O, as illustrated in Fig. 3.15. Three candidate forms of a monomial-like equation are examined

$$L_{\mathrm{MN,c1}} = \alpha_0 \mu_0 D_1^{\alpha_1} D_2^{\alpha_2} d_1^{\alpha_3} d_2^{\alpha_4} w^{\alpha_5} s^{\alpha_6} N_T^{\alpha_7} N_L^{\alpha_8} O^{\alpha_9 (N_L - 1)}, \tag{3.22}$$

$$L_{\mathrm{MN,c2}} = \alpha_0 \mu_0 D_1^{\alpha_1} D_2^{\alpha_2} \overline{D}_1^{\alpha_3} \overline{D}_2^{\alpha_4} w^{\alpha_5} s^{\alpha_6} N_T^{\alpha_7} N_L^{\alpha_8} O^{\alpha_9}, \tag{3.23}$$

$$L_{\mathrm{MN,c3}} = \alpha_0 \mu_0 D_1^{\alpha_1} D_2^{\alpha_2} \overline{D}_1^{\alpha_3} \overline{D}_2^{\alpha_4} w^{\alpha_5} s^{\alpha_6} N_T^{\alpha_7} N_L^{\alpha_8} O^{\alpha_9 (N_L - 1)}, \tag{3.24}$$

where D_1, D_2, and d_1, d_2, are the outer- and inner-side lengths, respectively, $\overline{D_1} = \frac{D_1 + d_1}{2}$, $\overline{D_2} = \frac{D_2 + d_2}{2}$, w the width of the conductor, s the spacing between turns, N_T the number of turns on one layer, N_L the number of layers, and O the distance between two consecutive layers.

The three candidates are close to, but with two crucial differences. The first one considers the inner-side length d, while the second and third the mean perimeters $\overline{D}$. The other difference is that the exponent of O depends on the number of layers for the first and third equations, but it is independent of them for the second. This means that the effect of O becomes greater as the number of layer increases.

After running the multiple linear regression (MLR) algorithm for all three equations, with a dataset as defined in the next subsection, the results are close but not identical. The

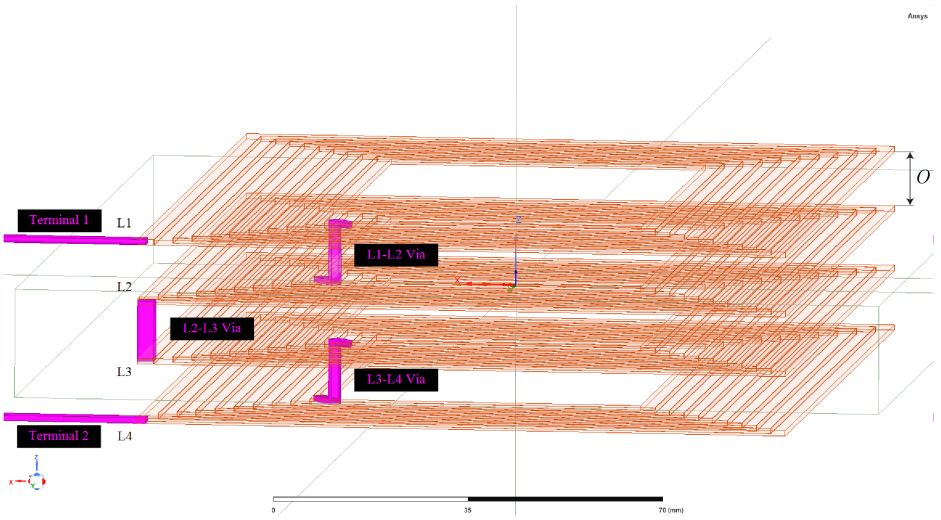


Figure 3.15 The simulation setup for the multilayer planar windings. The distance between two consecutive layers is O. The vias connecting the different layers has been modeled as well.

metrics utilized to evaluate the equation are the mean absolute error and the number of samples with error greater than 5%. The latter is crucial in order to guarantee that the proposed equation is not biased toward any specific subset (i.e., windings with 4 layers). Out of the three candidates, the MLR adaptation of (3.24) is presented in subsection 3.3.2, as it provided the best results.

3.3.1.1 Dimensions of Simulated Windings

As stated in the previous section, the orientation of the winding is irrelevant, so the inductance for a winding with dimensions $\{D_1^*, D_2^*\}$ is the same with $\{D_2^*, D_1^*\}$. This observation reduces the number of necessary simulations by a factor of 2. The outer-side lengths D_1 and D_2 of the simulated windings are presented in Table 3.8, and the full list of dimensions in Table 3.9. The dimensions set $\{D_1, D_2\} = \{70 : 110, 120 : 160\}$ has been omitted to reduce the total simulation time that is requires to generate the training dataset. As will be shown later, the proposed equation can accurately estimate the inductance of the windings with dimensions within the aforementioned omitted set.

The finite-element model developed in Maxwell3D (ANSYS) is presented in Fig. 3.15, for the four-layer case. Similarly to the single-layer models, the analysis region is 700x700x700 mm^3, and a denser parallelepiped encloses the winding, to provide more accurate results between the traces and the layers. The vias have been modeled as copper connections between the layers.

3.3.2 MLR Adaptation and Results

Applying $\log_{10}$ in both sides of (3.24) results in the following linear equation

Table 3.8 D_1 and D_2 dimensions, measured in [mm], for MLR training.

D_1 \ D_2	70	80	90	100	110	120	130	140	150	160
70	x	x	x	x	x					
80		x	x	x	x					
90			x	x	x					
100				x	x					
110					x					
120						x	x	x	x	x
130							x	x	x	x
140								x	x	x
150									x	x
160										x

Table 3.9 Simulated Datasets for MLR Training

	Dataset A	Dataset B
D_1	70:10:110 mm $D_1 \leq D_2$	120:10:160 mm $D_1 \leq D_2$
D_2	70:10:110 mm	120:10:160 mm
d_1	from (3.7), d_1 >17 mm	
d_2	from (3.7), d_2 >17 mm	
w	3, 4, 5 mm	
s	0.1, 0.3, 0.5 mm	
N_T	6, 8, 10 turns	
N_L	1, 2, 3, 4 layers	
O	0.5, 1.0, 1.5 mm not defined for $N_L = 1$	

$$\begin{aligned}\log_{10}(L_{\mathrm{MN}}) = c_0 &+ \alpha_1 \log_{10}(D_1) + \alpha_2 \log_{10}(D_2) + \alpha_3 \log_{10}(\overline{D}_1) + \alpha_4 \log_{10}(\overline{D}_2) \\ &+ \alpha_5 \log_{10}(w) + \alpha_6 \log_{10}(s) + \alpha_7 \log_{10}(N_T) + \alpha_8 \log_{10}(N_L) \\ &+ \alpha_9 (N_L - 1) \log_{10}(O)\end{aligned} \tag{3.25}$$

where $c_0 = \log_{10}(\alpha_0) + \log_{10}(\mu_0)$. Eq. (3.25) is a linear equation with the form $y = c_0 + c_1 x_1 + c_2 x_2 + \cdots + c_9 x_9$.

Generally, in MLR algorithms ($y = \sum_{i=0}^{N} (c_i x_i)$) the dataset is split into two subsets: one for the calculation of the coefficients c_i (training) and the other to assess the behavior of the equation to samples it has not been exposed to (evaluation). In this case, 80% of the samples (4680 samples) from the Datasets A and B (as given in Table 3.9) comprise the training subset, and the remaining 20% of the samples (1170 samples) comprise the

evaluation subset. Each sample is randomly assigned to either of the subsets, which is a common practice in MLR applications.

The resulting coefficients of the training process α_i are presented in Table 3.10, along with their corresponding variable (geometrical parameter). The asymmetry that is caused by the restriction $D_1 \leq D_2$ is pronounced by the fact that the exponents of D_1, D_2 and $\overline{D_1}, \overline{D_2}$ are not equal, and more specifically $|\alpha_1| > |\alpha_2|$ and $\alpha_3 > \alpha_4$. So, the equation

$$L_{\mathrm{MN}} = 1.602\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} s^{-0.011} N_T^{1.794} N_L^{1.804} O^{-0.006(N_L-1)}, \quad (3.26)$$

is valid when the restriction $D_1 \leq D_2$ is followed.

Table 3.10 Monomial Equation Coefficients

Variable	Coefficient	Value
constant	a_0	1.602
D_1	a_1	-0.592
D_2	a_2	-0.378
$\overline{D}_1$	a_3	1.175
$\overline{D}_2$	a_4	1.072
w	a_5	-0.183
s	a_6	-0.011
N_T	a_7	1.794
N_L	a_8	1.804
$O^{(N_L-1)}$	a_9	-0.006

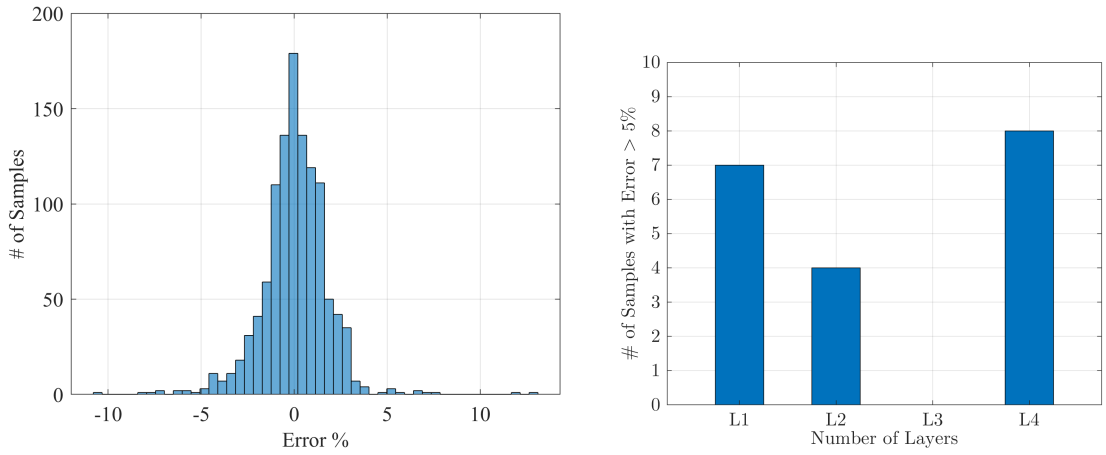
Several metrics can be used to determine the accuracy of the new equation. In Fig. 3.16a the histogram of the error

$$\mathrm{error}\% = \frac{L_{SIM} - L_{MN}}{L_{SIM}} \cdot 100 \quad (3.27)$$

is presented, where L_{SIM} and L_{MN} are the simulated and estimated inductance, respectively. The histogram is close to a normal distribution with mean value $\mu = 0\%$ and deviation of $\sigma = 1.77\%$. The total number of samples with error greater that 5% is presented in Fig. 3.16b, grouped according to the number of its layers. This is done in order to ensure that the equation is not biased against any subset of the original dataset. Another reliable metric is the resulting Mean Absolute Error (MAE), as given by

$$\mathrm{MAE} = \frac{1}{S} \sum_{i=0}^{S} \left(\frac{|L_{SIM} - L_{EQ}|}{L_{SIM}} \right) \cdot 100 = 1.24\% \quad (3.28)$$

where S is the number of evaluation samples.



(a) Grouped by the error % in 60 bins.

(b) Grouped by the number of layer.

Figure 3.16 Error % histogram and # of samples with > 5% error.

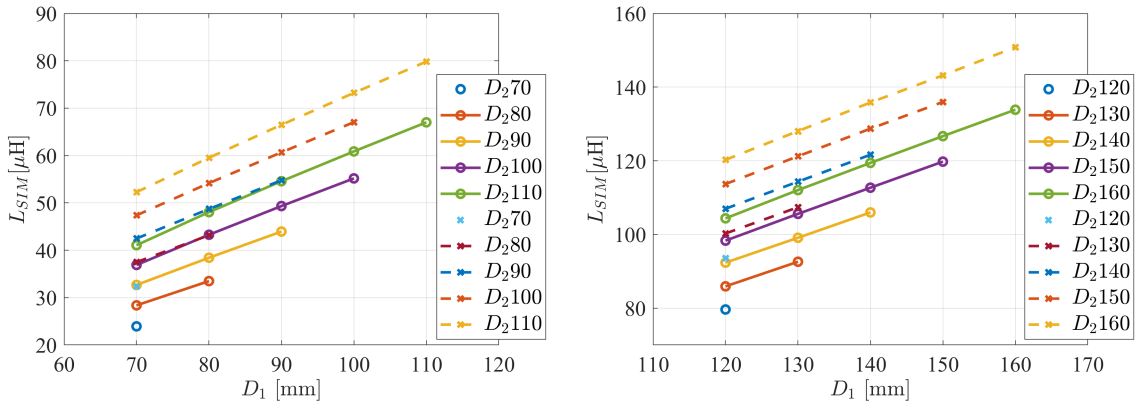
Usually, inductance equations contain an N^2 term, which means that for doubling the turns, the inductance is quadrupled. This is to be expected, since adding two inductors in series (adding N more turns to an inductor is practically connected two inductors of N turns in series) the total inductance is the self-inductance of each inductor, plus the mutual inductance between them. When the coupling factor is perfect (all the magnetic flux generated by one passes through the other and vice-versa), the mutual inductance is equal to the self inductance, hence $L_{series} = L + L + 2k\sqrt{L \cdot L} = 4L$.

In this case, MLR provides for both terms N_T (turns on each layer) and N_L (number of layer) a coefficient of 1.794 and 1.804 (practically equal to 1.8), respectively. This means that the equation compensates for the non-perfect coupling factor between turns and layers. The term $O^{-0.006(N_L-1)}$ only fine tunes this effect, based on the vertical distance between two consecutive layers, and receives values in the interval [1.0398, 1.1466], which means that can affect the estimation by approximately 11%. Another geometrical parameter with a small coefficient is w (width of the trace), which is raised to -0.183, and varies within [2.6369, 2.8953], affecting the estimation by approximately 10%. Finally, s (spacing between turns) is raised to -0.011 and varies with in [1.0872, 1.1066], affecting the estimation by less that 2%, which means that it can be neglected without affecting the estimation. Hence, the simplified form of the proposed equation is

$$L_{\text{MN}} = 1.7274\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} (N_T N_L)^{1.8} O^{-0.006(N_L-1)}, \tag{3.29}$$

with mean error $\mu = 0\%$, deviation $\sigma = 1.97\%$ and MAE $= 1.43\%$.

In Fig. 3.17 the estimated simulated inductance is presented, with respect to D_1 and D_2, for two different subsets of windings: the first (solid line) with $N_T N_L = 3 \cdot 8 = 24$ and



(a) (b)

Figure 3.17 The inductance of windings with $N_T N_L = 3 \cdot 8 = 24$ (solid line) and $N_T N_L = 4 \cdot 6 = 24$ (dashed line), with respect to D_1 and D_2.

the second (dashed line) with $N_T N_L = 4 \cdot 6 = 24$. The other geometric parameters are kept constant and equal to $w = 3$ mm, $s = 0.3$ mm, and $O = 1.5$ mm.

As it is shown, the inductance of $N_T N_L = 4 \cdot 6$ windings is larger from the corresponding $N_T N_L = 3 \cdot 8$, due to the fact that the windings with 8 turns have smaller d (for the same D). Furthermore, it seems that inductance increases linearly with D, which was difficult to derive directly from the equation. The parameters that play the most significant role in the total inductance are the outer- and inner- lengths, as well as the number of turns and layers. The width of the trace and the spacing slightly affect the inductance, but are responsible for the reduction of the inner-side lengths (under the assumption that the outer-side and the number of turns are constant).

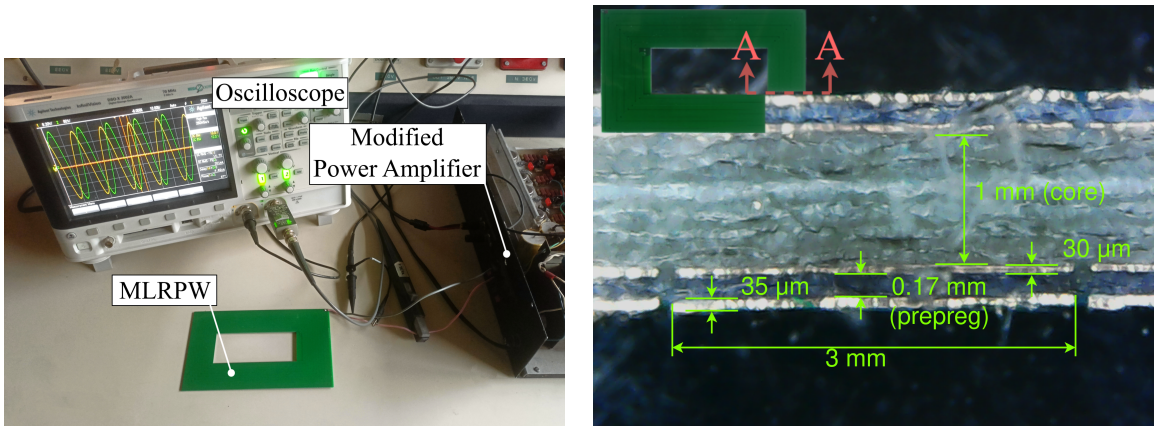
In the case of square-shape windings, where $D_1 = D_2 = D$ and $d_1 = d_2 = d$, Eq. (3.30) simplifies to

$$L_{\mathrm{MN}} = \alpha_0 \mu_0 D^{\beta_1} \overline{D}^{\beta_2} w^{\alpha_5} s^{\alpha_6} N_T^{\alpha_7} N_L^{\alpha_8} O^{\alpha_9 (N_L - 1)} \tag{3.30}$$

where $\beta_1 = \alpha_1 + \alpha_2 = -0.97$ and $\beta_2 = \alpha_3 + \alpha_4 = 2.247$. In this case, exponential values of (3.30) are reasonably close to those of (3.6).

3.3.2.1 Experimental Verification

To confirm the validity of the derived equation in practical windings, ten samples of different geometrical dimensions are examined. The experimental setup, as it is presented in Fig. 3.18, consists of a modified power amplifier, capable of producing 30 V peak, for current and frequency up to 1.5 A peak and 50 kHz, respectively. The parasitic capacitance is small enough to not affect the impedance in any measurable way for frequencies up to 200 kHz. The impedance of the winding is calculated by correlating the voltage excitation to



(a) Laboratory setup **(b)** AA cross-section

Figure 3.18 (a)The experimental setup for inductance measurement of MLRPWs at 50 kHz and current up to 1 A, and (b) the AA cross-section of an industrial L4RPW, where the layers are not equally spaced.

the amplitude and phase of the current response. To verify the measured inductance the HP 4284A precision LCR meter has also been utilized.

Nine of the windings were printed and folded properly in the lab. Custom printing is preferred to ensure that in multilayer design the distance O between each layer is the same. In commercially printed multilayer boards, copper layers are typically placed near the surface of the board, leaving larger vertical separation in the middle. The exact widths of copper layers, prepreg and core depend on the PCB manufacturer. In this case a 10th sample was ordered by a commercial manufacturer. Its values are measured and presented in Fig. 3.18b, and are in good agreement with the specifications given by the manufacturer.

The resulting inductances and the error with respect to (3.26) are presented in Table 3.11. It must be noted that even though most of the experimental windings do not belong to the training and evaluation datasets (at least one geometrical parameter is outside datasets A and B), there is only one where the equation estimates an inductance value with 6% error, compared to the experimentally measured one and all the others present significantly lower errors. Especially for the case of the commercial MLRPW, if O is replaced by the mean value of the prepreg and core, i.e., $(2 \cdot 0.17 + 1)/3 = 0.45$ mm, the equation provides very accurate estimation with only 3.15% error from the measured value.

3.3.3 Non-Linear Optimization with Non-Linear Constrains

The derived monomial-like equation in its general form

$$L_{\mathrm{MN}} = 1.602\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} s^{-0.011} N_T^{1.794} N_L^{1.804} O^{-0.006(N_L-1)}, \quad (3.31)$$

Table 3.11 Simulation and Experimental Results

	Dimensions [mm]									Inductance [μH]		
	D_1	D_2	d_1	d_2	w	s	O	N_T	N_L	L_{MN}	L_{LAB}	Error %
Square	100.0	100.0	44.0	44.0	4.0	2.0	1.60	5	2	9.69	9.38	3.31
	100.0	100.0	42.0	42.0	5.0	1.0	1.60	5	4	34.09	33.51	1.71
	100.0	100.0	42.0	42.0	5.0	1.0	1.60	5	2	9.09	8.91	1.95
	100.0	100.0	42.0	42.0	5.0	1.0	3.20	5	2	9.05	8.53	6.08
Rectangle	100.0	163.0	31.0	94.0	3.0	0.5	-	10	1	13.74	13.48	1.97
	210.0	294.0	101.0	185.0	5.0	0.5	1.50	10	2	125.70	120.80	4.05
	120.0	160.0	33.0	73.0	5.0	0.5	-	8	1	8.19	8.26	-0.77
	120.0	160.0	33.0	73.0	5.0	0.5	1.60	8	2	29.65	30.87	-3.95
	120.0	160.0	33.0	73.0	5.0	0.5	1.60	8	3	63.87	66.40	-3.81
	100.0	165.0	38.2	103.2	3.0	0.1	0.45	10	4	215.55	222.57	-3.15
	53.0	99.8	11.6	58.4	2.5	0.1	0.40	8	4	61.97	63.43	-2.35

can be utilized in an non-linear optimization algorithm in order to derive the best possible design with regard to one criterion, within a set of linear or non-linear constrains.

A specific example is examined to better illustrate the structure of the optimization problem and the benefit of using (3.31) to design an MLRPW. From the multiple linear regression data-fitted monomial equation the linear constrain

$$D_1 < D_2 \tag{3.32}$$

must hold. Furthermore, since the variables of the equation represent the geometrical parameters of the windings, which interact with each other, the non-linear restriction

$$d_1 = D_1 - 2N_T(w + s) + 2s \tag{3.33}$$

$$d_2 = D_2 - 2N_T(w + s) + 2s \tag{3.34}$$

should, also, be valid. The optimization process is taking place within the boundaries that are defined in Table 3.12.

Finally, the number of turns should be an integer number

$$N_T \in \{3, 4, \dots 9, 10\} \subset \mathbb{N}^* \tag{3.35}$$

It should be noted that in some designs fractional turns ($k + 0.5, k \in \mathbb{N}^*$) are preferable, mainly due to structural reasons and reduction of the ohmic resistance of the windings [131]. It is possible to relax this constrain by including more valid values for N_T, when such necessity arises.

Table 3.12 Lower and upper boundaries for the optimization process.

	lower boundary	upper boundary	units
D1	12.0	54.0	mm
D2	55.0	101	mm
d1	10.5	52.0	mm
d2	54.0	99.0	mm
w	2.5	5.0	mm
s	0.1	1.0	mm

The number of layers N_L is not considered in this optimization process, as it is independent of the other variables and as it increases, so does the total inductance. Similarly, the vertical distance between two consecutive layers O is not considered, since it depends on the production capabilities of the PCB manufacturer, and its increase leads to inductance reduction.

The non-linear programming solver `fmincon` is offered by Matlab and utilizes the interior-point algorithm, explained in detail in [132], properly modified by [133, 134, 135]. The algorithm finds the minimum of

$$\min_x \left(-L_{MN}(\vec{x})\right) \; : \; \begin{cases} c(\vec{x}) \leq 0 \\ c_{eq}(\vec{x}) = 0 \\ A \cdot \vec{x} \leq b \\ Aeq \cdot \vec{x} = b_{eq} \\ lb \leq \vec{x} \leq ub \end{cases} \tag{3.36}$$

where $c(x) \leq 0$ and $c_{eq}(x) = 0$ describe the non-linear constrain inequalities and equalities, respectively, $A \cdot \vec{x} \leq b$ and $Aeq \cdot \vec{x} = b_{eq}$ describe the linear constrain inequalities and equalities, respectively, and $lb \leq x \leq ub$ define the lower and upper boundaries for vector $\vec{x}$. Note that the algorithm tries to find the minimum L_{MN}, so the $-L_{MN}$ is utilized to find the maximum. The linear constrains of (3.32) can be easily implemented as `A(1,1) = 1; A(1,2) = -1;` and `b = 0;`.The vector $\vec{x}$ is defined as

$$\vec{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{bmatrix} = \begin{bmatrix} D_1 \\ D_2 \\ d_1 \\ d_2 \\ w \\ s \\ N_T \end{bmatrix} \tag{3.37}$$

and the lower and upper limits of each x_i are
`lb = [0.012 0.055 0.0105 0.054 0.0024 0.0001 03];` and
`ub = [0.054 0.101 0.0520 0.099 0.0060 0.0010 10];`, respectively.
The non-linear constrains of (3.33) and (3.34) are implemented as
`ceq(1) = x(1) - x(3) - 2*x(7)*(x(5)+x(6)) + 2*x(6);` and
`ceq(2) = x(2) - x(4) - 2*x(7)*(x(5)+x(6)) + 2*x(6);`.
Finally, the constrain (3.35) is implemented as

```
ceq(3) = (x(7)-v(1)) * (x(7)-v(2)) * (x(7)-v(3)) * (x(7)-v(4)) * (x(7)-v(5)) *
(x(7)-v(6)) * (x(7)-v(7)) * (x(7)-v(8));
```

where vector `v = [3 4 5 6 7 8 9 10];`. This forces the algorithm to consider only the values of `v` as valid for the N_T.

The problem is characterized as non-linear mixed integer optimization, which is non-convex in the general case, and may lead to several local maxima. One way to overcome this issue is running the optimization algorithm for different initial points `x0`, which can be randomized for each iteration.

For each iteration the optimization algorithm converges to a specific state vector $\vec{x}_i$ and returns a local maximum of $L_{MN,i}$. When the $L_{MN,i}$ is greater than the temporary $L_{MN,opt}$, and the constraints are not violated, the temporary $\vec{x_{opt}}$ is updated to the current $\vec{x_{opt}} = \vec{x_{iter}}$ and $L_{MN,opt} = L_{MN,i}$. It must be noted that this method does not mathematically guarantee that the global maximum is achieved. However, practically, running the algorithm for a large number of iterations, provides a very good solution.

The optimal results are presented in Table 3.13, and its dimensions are very close to those of the winding presented in the last row of Table 3.11.

Table 3.13 Optimization algorithm results.

		[mm]				turns	[μH]
D_1	D_2	d_1	d_2	w	s	N_T	L
54.0	101	12.6	59.6	2.5	0.1	8	63.82

It can be noted that the max(L) is achieved for max(D_1) and max(D_2), but not for max(d_1), max(d_2), or max(N_T). A winding of these dimensions has been designed and commercially printed, with a measured inductance of 63.43 μH, resulting in 0.7% error compared to the equation.

3.4 Comparison of L1 Modified and MLR Equations

To illustrate the potential of each equation, modified or data-fitted, a comparison between them is useful. In this section, the two datasets as they are presented in subsections 3.2.2 and 3.3.2 are combined and used to compare the MAE and the error distribution of each equation and highlight the context in which they provide the best results.

Two sets of comparisons are carried out. The first one is considering single-layer rectangle-shaped planar windings (L1RPW). Five equations are compared, the three modified equations of subsection 3.2.2, the novel monomial equation of subsection 3.3.2, and one additional monomial equation with recalculated coefficients. The second comparison considers multilayer rectangle-shaped windings. Four equations are compared, the three modified with the assumption that the total number of turns is equal to the product of the number of layers and the turns per layer, and the novel multilayer monomial equation.

3.4.1 Single-Layer

The equations under consideration are presented again in this section for the sake of completeness,

$$L_{\mathrm{WH}} = 2.34\mu_0 N^2 \frac{\|\overline{D}\|_0}{1 + 2.75\|\rho\|_0}, \tag{3.38}$$

$$L_{\mathrm{RS}} = \frac{1.27}{2}\mu_0 N^2 \|\overline{D}\|_0 \left(\ln\left(\frac{2.07}{\|\rho\|_0} \right) + 0.18\|\rho\|_0 + 0.13\|\rho\|_0^2 \right), \tag{3.39}$$

$$L_{\mathrm{MN}} = 1.5428\mu_0 N^{1.78} \|\overline{D}\|_{-1}^{2.4} \|D\|_{-1}^{-1.21} w^{-0.147} s^{-0.03}, \tag{3.40}$$

along with the a modified data-fitted monomial-like equation. Since the original equation is fitted for small (dimensions of μm) windings, its coefficients are recalculated via MLR algorithm to fit the square-shaped windings of dataset presented in Tables 3.2 and 3.9 (dimensions of mm), and then optimized for the RPW case. It is denoted with an $\boldsymbol{RL}1$ subscript, as in

$$L_{\mathrm{MN,RL1}} = 1.3677\mu_0 N^{1.774} \|\overline{D}\|_0^{2.255} \|D\|_0^{-1.064} w^{-0.165} s^{-0.021}. \tag{3.41}$$

The monomial-like equation derived in subsection 3.3.2 is adjusted for single-layer winding estimation, as in

$$L_{\mathrm{MN,MLR}} = 1.51\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} N_T^{1.794}. \tag{3.42}$$

In Fig. 3.19 the error histogram is presented for each equation separately, and in Table 3.14 the respective MAE%, mean value μ, and deviation σ. With the exception of (3.40) (modified Monomial), all error distributions are close to the normal, with small deviation σ, and have a MAE of less than 3%. Eq. (3.39) (modified Rosa) presents the best inductance estimation, with (3.38) (modified Wheeler), (3.42) (Monomial MLRPW), and (3.41) (Monomial RL1) following.

Table 3.14 MAE%, mean value, and deviation for L1RPWs

Equation		MAE	μ	σ
Mod. Wheeler	(3.38)	1.05 %	-0.38	1.33
Mod. Rosa	(3.39)	0.64 %	-0.02	1.00
Mod. Monomial	(3.40)	4.54 %	-3.68	3.52
Monomial RL1	(3.41)	2.59 %	2.23	2.94
Monomial MLR	(3.42)	2.01 %	-0.20	2.33

However, when considering the MAE% with respect to the ratio D_1/D_2, only (3.38) and (3.39) provide results with less than 3%, and (3.42) with less than 4.1 %, as it is presented in Fig. 3.20, which makes these equations practically similar.

3.4.2 Multi-Layer

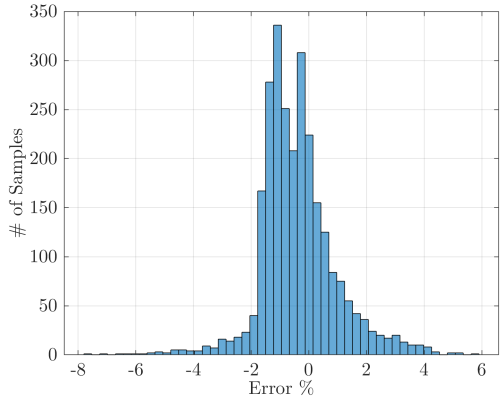
Based on the results presented in [130], and the fact that (3.26) has almost the same exponential values for N_T and N_L, a comparison between the equations of Sections 3.2 and 3.3 is possible, by substituting the number of turns N with the product of number of turns times the number of layers $N_T \cdot N_L$, as in

$$L_{\mathrm{WH}} = 2.34\mu_0 (N_T \cdot N_L)^2 \frac{\|\overline{D}\|_0}{1 + 2.75\|\rho\|_0}, \tag{3.43}$$

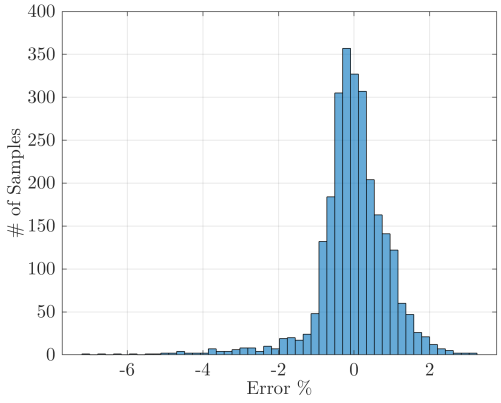
$$L_{\mathrm{RS}} = \frac{1.27}{2}\mu_0 (N_T \cdot N_L)^2 \|\overline{D}\|_0 \left(\ln\left(\frac{2.07}{\|\rho\|_0}\right) + 0.18\|\rho\|_0 + 0.13\|\rho\|_0^2 \right), \tag{3.44}$$

$$L_{\mathrm{MN}} = 1.5428\mu_0 (N_T \cdot N_L)^{1.78} \|\overline{D}\|_{-1}^{2.4} \|D\|_{-1}^{-1.21} w^{-0.147} s^{-0.03}, \tag{3.45}$$

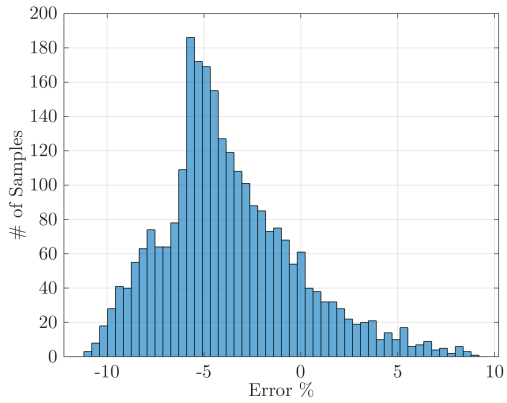
$$L_{\mathrm{MN}} = 1.602\mu_0 D_1^{-0.592} D_2^{-0.378} \overline{D}_1^{1.175} \overline{D}_2^{1.072} w^{-0.183} s^{-0.011} N_T^{1.794} N_L^{1.804} O^{-0.006(N_L-1)}. \tag{3.46}$$



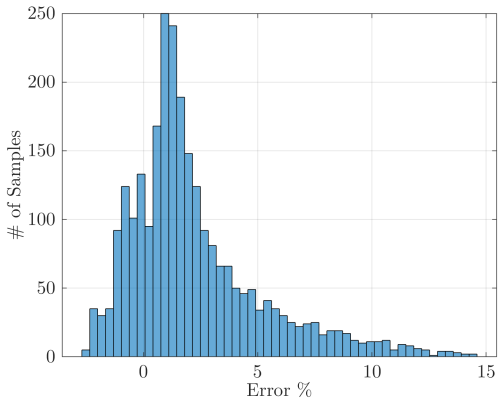
(a) Modified Wheeler



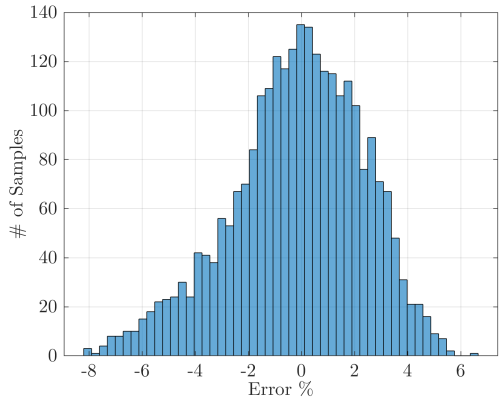
(b) Modified Rosa



(c) Modified Monomial



(d) Monomial RL1



(e) Monomial MLR

Figure 3.19 Error% histogram for each separate equation for L1RPWs.

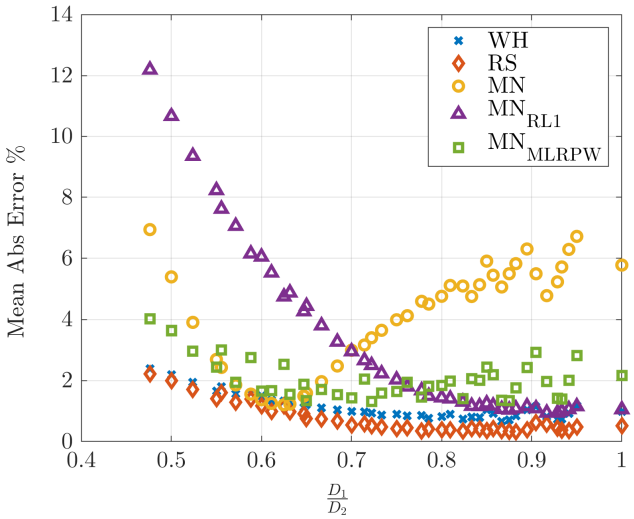
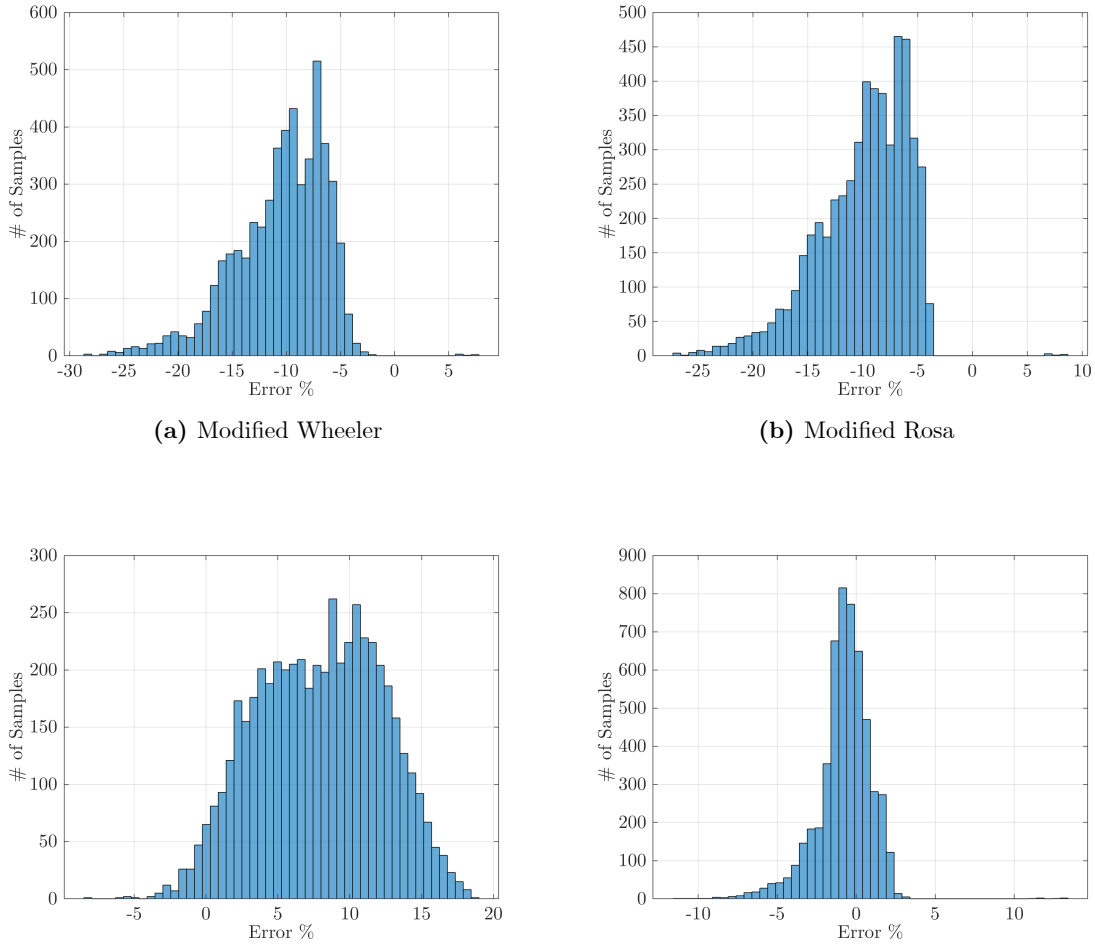


Figure 3.20 Comparison of MAE % for as a function of the ratio D_1/D_2, which represents the deformation of the square shape.

The error% histograms are presented in Fig. 3.21 for each equation respectively. As it was expected and presented in Table 3.15, (3.43) and (3.44) overestimate the total inductance, with a mean value of -10%, while (3.45) underestimates it, with a mean value of 8%. Only (3.46) provides accurate results, with a mean value of approximately 0% and small standard deviation.

Table 3.15 MAE% and mean value for MLRPWs

Equation		MAE	μ
Mod. Wheeler	(3.43)	10.55 %	-10.53
Mod. Rosa	(3.44)	9.95 %	-9.93
Mod. Monomial	(3.45)	7.96 %	7.89
Monomial MLR	(3.46)	1.35 %	-0.76



(a) Modified Wheeler

(b) Modified Rosa

(c) Modified Monomial

(d) Monomial MLR

Figure 3.21 Error% histogram for each separate equation for MLRPWs.

3.5 Selection and Effect of Ferrite Core

Planar inductors and transformers can operate without a core since they usually present high coupling factor and have structural support from the PCB. However, when a specific application requires large inductance values in a small volume, electromagnetic field containment, and even higher coupling factor, the use of a ferrite core is advised. Especially in the case of high current, traces must have large width leading to windings of few turns, ferrite cores are utilized to increase the inductance. In this section the introduction of a core is discussed, the basic relations that describe the cored inductor are presented, and an example of an EI ferrite core from Fair-Rite 7895400721 is considered.

3.5.1 Core Loss Estimation

Magnetic cores for high-frequency designs are usually soft ferrites, namely alloys of Mn-Zn (frequencies $<$ 2 MHz) and Ni-Zn ($>$ 1-2 MHz) [136, 137]. Manufacturers generally categorize them with respect to a specific application or usage (switch-mode power supplies, telecommunications, EM filters, etc.), the frequency range, the geometrical shape (EI, UI, PQ, toroid, etc.), and the material properties (permeability μ, saturation flux density B_{sat}, power loss P_V, etc.) [101, 138, 139, 140]. The categorization can act as a first filter of selection from a plethora of potential cores, based on a rough estimate of the desired inductance value, frequency range, and volume.

After reducing the range of options to a few candidates, a more detailed analysis on the losses of the core with respect to the magnetic flux and the frequency is useful. Generally, the losses (per unit volume) are given by the Steinmetz equation [141]:

$$P_{core} = P_{hyst.} = K_c(\Delta B)^m (f_s)^n, \tag{3.47}$$

where

- $P_{hyst.}$ the core losses per unit volume
- K_c a constant depending on the core
- ΔB the magnetic flux density swing
- f_s the switching frequency
- m a constant between 1.5 and 3
- n a constant between 1 and 2 [94, 142]

which is valid for sinusoidal excitation. For non-sinusoidal excitations the improved Steinmetz equation is developed [143]:

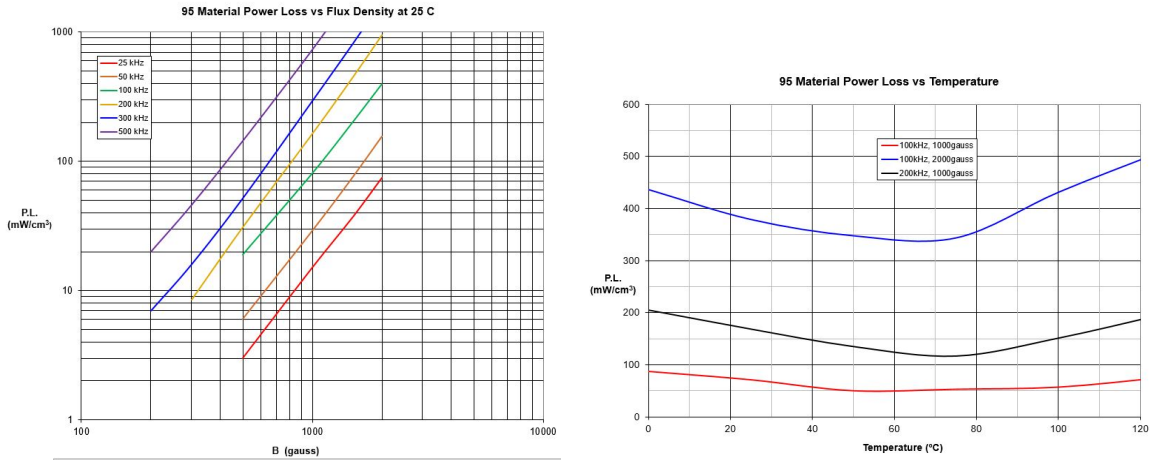
$$P_{core} = K_c(\Delta B)^m f_{eq}^{n-1} f_r, \tag{3.48}$$

where

- $f_{eq} = \frac{2}{(\Delta B)^2 \pi^2} \int_0^T (\frac{\mathrm{d}B(t)}{\mathrm{d}t})^2 \mathrm{d}t$, is the equivalent frequency
- $\frac{\mathrm{d}B(t)}{\mathrm{d}t}$ the core loss magnetization rate.

A more detailed comparison between the various empirical models (original, modified, generalized, improved-generalized and natural Steinmetz equations) is presented in [142].

Another way of estimating the core losses is through the measurements that are provided from the manufacturers. The vast majority of cores are accompanied by the power loss per unit volume P_V in the datasheet. P_V increases as the switching frequency (f_s) and the magnetic flux density (B) increases, as illustrated in Fig. 3.22a, for an indicative case (Fair-Rite 95). It also depends on the temperature, as illustrated in 3.22b, for the same material, presenting an optimum area of operation in the neighborhood of 60-80 ^{o}C. Utilizing the datasheet figures, a rough estimate of the losses can be derived without the knowledge of material constants like K_c, m, and n.



(a) As a function of frequency and magnetic flux.

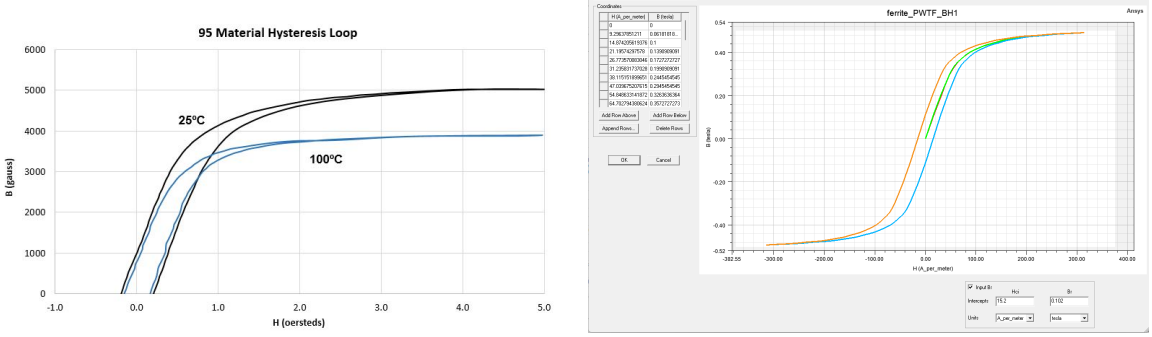
(b) As a function of temperature.

Figure 3.22 Core losses per unit volume for the Fair-Rite 95 material (7895400721).

Core losses can also be estimated via proper simulation methods, i.e., FEM models utilizing the BH hysteresis loop. Maxwell3D of ANSYS enables this calculation when the initial magnetization curve and the H_c, B_r are known. As illustrated in Fig. 3.23, using the BH curve from the datasheet, converting all variables to the SI, and importing them to the hysteresis loop properties, can result in an accurate model.

3.5.2 Advantages and Disadvantages of Core Utilization in PWs

Both (3.47) and (3.48) imply that an increase in the switching frequency would require a decrease in the magnetic flux swing to maintain the same loss level. The magnetic flux density (B) inside the material depends on the product of ($A_e \cdot N$) as in



(a) BH curve from datasheet. **(b)** Simulated BH curve for 25 ^{o}C.

Figure 3.23 BH curve for the Fair-Rite 95 material (7895400721).

$$B = K_d \frac{m_f}{N A_e}, \tag{3.49}$$

where

- B is the magnetic flux density [T]
- K_d a dimensional constant
- m_f the excitation [Vs] or [AH]
- N the number of turns
- A_e the effective cross-section of the core [m^2].

Hence, to decrease the magnetic flux swing, an increase in the cross-section A_e is required, while maintaining the same amount of turns. However, increased A_e suggests larger core volume V_c, which increases the core losses. Due to their shape, cores for PWs can achieve large cross-section area but with a relatively small total volume, meaning that the ratio A_e/V_c is larger compared to most conventional cores. For the same reason, heat dissipation is more efficient for PWs cores.

However, the utilization of a ferrite core comes with various disadvantages. The cost of an off-the-shelf core is several times that of the winding, which can further increase if a custom design is required. The estimation of the inductance becomes significantly less accurate due to the uncertainty, the non-linearity, and the temperature-dependence of the relative permeability. Furthermore, the surface of the materials is not perfectly flat, hence, for two-piece cores (EI, EE, UI, etc.) inconsistent and small air-gaps are created in the point of contact. The applied pressure which holds the two pieces affects the total inductance, meaning that inductance can start drifting with time.

It is, therefore, difficult to accurately calculate the magnetizing and leakage inductance of a cored MLRPW. Many approaches have been developed, presenting analytical solutions [144] and designing tools for optimization [145, 146], or rely on computational intelligence

methods, like differential evolution algorithms [147]. Others propose asymmetrical winding designs with core air-gaps to control the leakage inductance, which is crucial for active bridge and resonant converters [148].

3.5.3 Analysis, Simulation and Experimental Results

For the sake of completeness, an indicative example of a cored MLRPW with dimensions D_1= 53 mm, D_2= 99.8 mm, w= 2.5 mm, s= 0.1 mm, N_T= 8 turns, and N_L= 4 layers is presented. The equivalent reluctance model for the Fair-Rite 7895400721 core is illustrated in Fig. 3.24 and the corresponding values in Table 3.16. It is known that the reluctance is given by

$$R_i = \frac{l_i}{\mu_r \mu_0 \mathrm{A}} \tag{3.50}$$

where l_i is the effective length of the i core segment, μ_r the relative permeability, and A the effective cross-section. The equivalent length of the corner reluctance is discussed in [149]. The lengths and areas of each core segment are defined in Table 3.16, where d_c is the depth of the core, and the absolute dimensions of the core are given by the manufacturer in [150]. In the case of the air-gap section $\mu_r = 1$ and the fringe effect is considered too small to play a significant role.

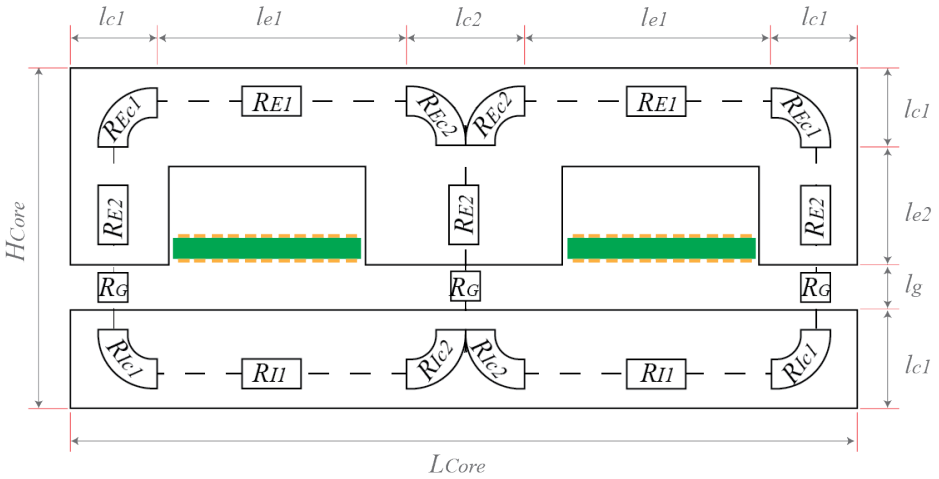


Figure 3.24 Reluctance model of Fair-Rite 7895400721.

The equivalent reluctance model is presented in Fig. 3.25, where

$$\begin{aligned} R_l &= R_{Ec2} + R_{E1} + R_{Ec1} + R_{E2} + R_G + R_{Ic1} + R_{I1} + R_{Ic2}, \\ R_c &= R_{E2} + R_G, \\ R_r &= R_{Ec2} + R_{E1} + R_{Ec1} + R_{E2} + R_G + R_{Ic1} + R_{I1} + R_{Ic2}, \end{aligned} \tag{3.51}$$

and the corresponding magnetic fluxes are given by

Table 3.16 Lengths are areas of the core segments.

Segment	Length		Area	
	formula	l [m]	formula	A [m^2]
R_{E1}	l_{e1}	21.75e-3	$l_{c1} \cdot d_c$	260.10e-6
R_{E2}	l_{e2}	5.30e-3	$l_{c1} \cdot d_c$	260.10e-6
R_{Ec1}	$\pi(l_{c1} + l_{c1})/8$	4.01e-3	$(l_{c1} + l_{c1})/2 \cdot d_c$	260.10e-6
R_{Ec2}	$\pi(l_{c1} + l_{c1}/2)/8$	3.00e-3	$(l_{c1} + l_{c1}/2)/2 \cdot d_c$	195.08e-6
R_g	l_g		$l_{c1} \cdot d_c$	
R_{I1}	l_{e1}	21.75e-3	$l_{c1} \cdot d_c$	260.10e-6
R_{Ic1}	$\pi(l_{c1} + l_{c1})/8$	4.01e-3	$(l_{c1} + l_{c1})/2 \cdot d_c$	260.10e-6
R_{Ic2}	$\pi(l_{c1} + l_{c1}/2)/8$	3.00e-3	$(l_{c1} + l_{c1}/2)/2 \cdot d_c$	195.08e-6

$$\begin{aligned} \phi_l &= \frac{1}{2}\frac{R_l R_r}{R_l R_c + R_c R_r + R_l R_r} NI, \\ \phi_c &= \frac{R_l R_r}{R_l R_c + R_c R_r + R_l R_r} NI, \\ \phi_r &= \frac{1}{2}\frac{R_l R_r}{R_l R_c + R_c R_r + R_l R_r} NI. \end{aligned} \tag{3.52}$$

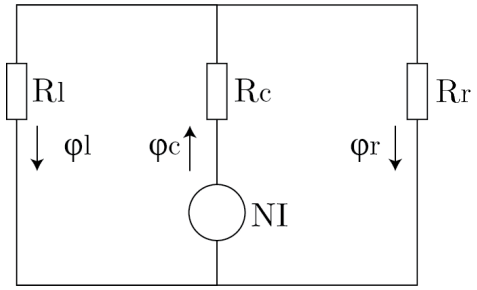
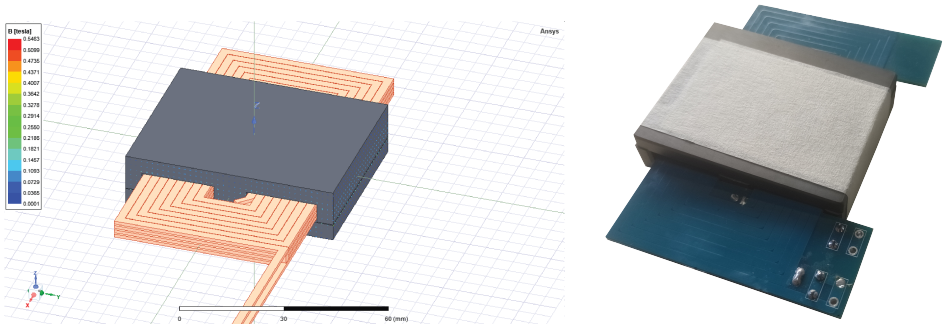


Figure 3.25 Reluctance model of Fair-Rite 7895400721.

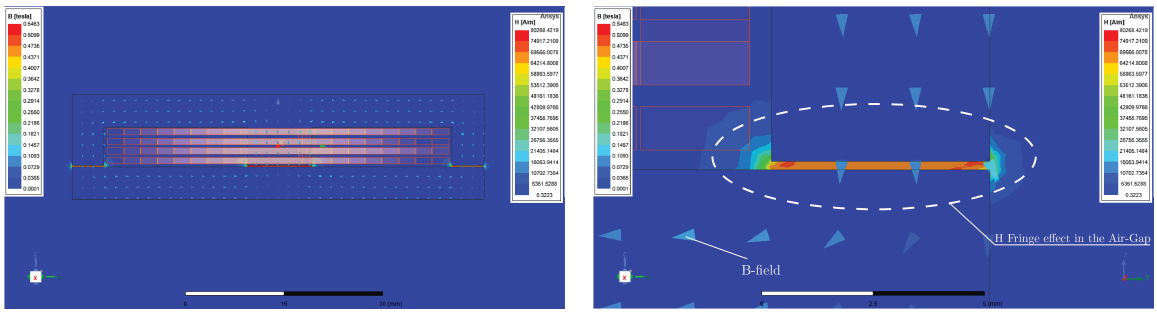
The 3D model of the winding in Maxwell3D (ANSYS) is presented in Fig. 3.26a, while the laboratory prototype is constructed and presented in Fig. 3.26b. As already explained, the imperfections on the connection of the EI core are modeled as a small air-gap, in the order of μm. The magnetic field density $\boldsymbol{B}$ and intensity $\boldsymbol{H}$ are presented in Fig. 3.27a, while in Fig. 3.27b the $\boldsymbol{H}$ fringe effect of a 100 μm air-gap is illustrated. The simulation verifies the assumption that small air-gaps do not experience significant fringing, and the magnetic flux passes though an effective area equal to that of the ferrite core.

Ranging the l_g from 20 to 100 μm air-gap, the results of the simulation do not vary more that 4%. For $l_g = 50$ μm, the simulation estimates an inductance $L_{\text{SIM}} = 15.650$ mH. It should be noted that simulation results are as accurate as the precise knowledge of the relative permeability and the BH curve, especially its slope. In this case, the region of analysis can be reduced as the vast majority of the magnetic flux is detained inside the core.



(a) Simulated MLRPW with core. **(b)** Laboratory MLRPW with core.

Figure 3.26 Cored multi-layer rectangle shaped winding.



(a) X-axis oriented view. **(b)** Zoomed at the air-gap.

Figure 3.27 Simulated cored multi-layer rectangle shaped winding.

The experimentally measured inductance was found $L_{\mathrm{EXP}} = 15.200$ mH. However, the pressure applied to the real-world core, can affect the measured inductance by 7%. In this case, the two parts of the EI core are mildly pressed and held together by paper tape. If the winding is designed to operate under extreme temperature differences, metal clips and adhesive paste shall be used.

3.6 Conclusions

In this chapter the design and inductance estimation of planar windings is discussed, along with their advantages and disadvantages. Several applications that can make use of the low z-profile of the PWs are presented, in commercial and industrial applications.

The effect of each geometrical parameter is discussed, and the state-of-the-art estimation equations are presented for single-layer square- and rectangle-shape windings. By slightly modifying three well-known equations, namely Wheeler, Rosa, and the Monomial, it is possible to estimate the inductance of rectangle-shaped windings without the need of complex analytical solutions.

The modified equations, especially Wheeler and Rosa, provide accurate results, with less than 1.5% mean absolute error for the specified dataset of high-power windings. In addition, an algorithm for estimating the inductance per turn is presented, in order to ensure the safe operation of the winding.

In the case of multi-layer RPWs, a monomial-like equation is developed and its coefficients are adjusted to a large dataset of windings via multiple linear regression. The new equation provide accurate results with mean value $\mu = 0\%$, standard deviation $\sigma = 1.77\%$, and mean absolute error less than 1.5%.

A comparison between the aforementioned equations is carried out for single-layer and multi-layer RPWs separately. Rosa and Wheeler equations outperform all the others for the single-layer case, with the new monomial equation, introduced in this thesis, following close. The deformation factor $\boldsymbol{D_1/D_2}$ does not seem to play a significant role for these equations. However, the new monomial equations outperforms any other equation for the multilayer case, by a large factor.

Finally, a brief discussion on the introduction of a ferrite core is made. The advantages and disadvantages are presented and an indicative example of Fair-Rite 7895400721 is analyzed, simulated and experimentally verified.

Chapter 4

Resonant Converter

4.1 Introduction

The current trends in power electronic converters demand for high-energy density, compact solutions [151, 152, 153], often requiring galvanic isolation between the input and the output stages for safety and protection purposes [154, 155]. This can be achieved by raising the switching frequency and the voltage and current ratings of the switching devices. It also demands good spatial planing of the PCB and special consideration for the magnetic components [156, 157, 158], issues that are discussed in detail in the previous chapters. Magnetic integration of planar windings [120] can lead to further volume and cost reduction.

From the switching components side, the main restriction to increase the switching frequency and the current handling capability of a converter is the heat dissipation. High-power high-frequency hard-switching converters suffer from both increased conduction and switching losses, due to the large current passing through (limited area of) the transistors, as well as the voltage and current they have to frequently interrupt. In order to assure the proper operation of the converter, either the switching frequency is limited or large heatsinks are deployed, increasing the volume and reducing the power density.

To compensate these issues, resonant power converters have emerged as a compelling solution for achieving high efficiency levels, increasing power density, and reducing switching losses. Resonant power converters, designed more than a half century ago for turning-off thyristors [159], utilize the principles of resonant circuits to optimize energy transfer and minimize losses, making them well-suited for a wide range of applications, from high-frequency power supplies to renewable energy systems and electric vehicle chargers. The structure of some indicative cases of these unidirectional and bidirectional power flow converters are illustrated in Fig. 1.1, and discussed in subsection 1.2.1.

4.1.1 Design Aspects

One of the primary benefits of resonant converters is their ability to achieve high efficiency through zero-voltage (ZVS) or zero-current switching (ZCS). This switching technique significantly reduces switching losses, resulting in an improved overall efficiency and reduced heat production. As a result, the voltage, the current and eventually the thermal stress on the semiconductor devices (such as MOSFETs or IGBTs) can be reduced. Some studies have shown that replacing the Si-based semiconductors with SiC-based can lead to even more efficient energy conversion [160, 161].

Resonant converters emit lower electromagnetic radiation and cause less interference (less EMI) due to their inherent ability to produce more sinusoidal waveforms (less harmonic content), minimizing the need for additional EMI filtering [162, 163]. Moreover, due to the resonant components, they provide an inherent protection against output short-circuit faults. Control methods that can protect against short-circuits and overloads have been proposed from the early days of resonant converters [164], but is still an interesting research topic. As proposed in [165], with proper modifications, they can also achieve fault protection against short- and open-circuit faults of the semiconductor devices.

However, resonant power converters do come with certain limitations. One notable drawback is the larger peak current they exhibit compared to traditional converters and the large voltage levels that can be developed in the resonant circuit. This can lead to significant increase in losses and challenges in designing the magnetic components. Control plays a crucial role on the correct and efficient operation of the converter, and an inappropriate implementation can cause less efficient performance, even when compared to hard-switching converters. A detailed review on the modulation strategies can be found in [166], where various configurations of LLC circuits are considered, including variable resonant inductors [167, 168] and capacitors. The impact of the dead-time, regarding unipolar and bipolar switching devices can be found in [169]. Moreover, in [170] an extremely simple control scheme is proposed, where the two active bridges of a CLLC converter operate in synchronization, and can achieve up to 98.7% efficiency.

Furthermore, the design of resonant converters can prove challenging when parallel multiple branches or three-phase topologies are employed [171], to handle higher power levels. Proper synchronization and control become crucial in parallel operation to prevent undesired interactions and ensure stable performance. This issue has been analyzed in depth in [172], where the resonant capacitor is connected on the DC side of a full bridge. Therefore, the effective capacitance can be regulated by the control of the full bridge, and compensate for any mismatch between the interleaved branches. Another method has been proposed in [173], where a phase-shift modulation technique is used to regulate the current between mismatched components of each high-frequency link. The stability of such topologies is explored in [174], utilizing large- and small-signal models of the parallel-connecting converters

in closed-loop control. Partial power processing techniques have been proposed, like in [175], where each parallel branch can be decoupled and designed separately, simplifying the control and the optimization process.

Additionally, resonant converters may exhibit a narrower operating range compared to some other converter topologies, necessitating careful design considerations to match the converter to the specific application requirements. For example large voltage swings in the input can lead to significant reduction in efficiency. Countermeasures have been proposed [176], which include proper control of the converter in the boundary DCM region. Ongoing research and advancements in resonant converter technologies aim to address these drawbacks, further enhancing their appeal in high-performance power conversion applications.

4.1.2 Time and Frequency-Domain Analysis

To understand the fundamental concepts, working principles, and design considerations of series-resonant (LC-SR) and LLC resonant power converters, frequency- and time-domain analyses (FDA and TDA) can be useful.

From the first steps of resonant converters, state-space models for unidirectional, LC-SR half-primary-bridge topologies have been proposed [64, 177]. The same work assisted with simplifying the non-linear rectifier bridge and load with an equivalent resistance, which consumes the same amount of power as the non-linear model. However, it should be noted that the waveforms of the simplified circuit do not correspond to those of the real converter. Other researchers proposed analytical solutions for the neutral-point half-bridge [63] and full-bridge [66] LC-SR converters, however only for capacitive continuous and discontinuous current modes.

Large- and small-signal analyses [178, 179] have been proposed for the neutral-point half-bridge LC-SR converter, again, only for the capacitive operation. For the same converter, steady-state analyses have been proposed [65, 180], as well as closed-form expressions from the infinite Fourier series [181], however, restricted to the same operational region.

FDA provides simple equations that can be used to understand the behavior of the resonant circuit [182]. Nevertheless, several challenges arise when the operation of the whole converter is analyzed in the frequency domain. The non-linear behavior of the output stage and the operation under switching frequencies away from the resonant can generate inaccuracies, as it is presented in [183]. In [184] an improved first harmonic approximation (FHA) is proposed, utilizing an equivalent output impedance, making the equations more composite but providing more accurate results.

TDA provides more complex equations, which are capable to accurately describe the voltage and current at any node of the converter, a critical information when ZVS or ZCS should be achieved [70]. Reducing the order of the differential equations to simplify them has been proposed in [69], and provides adequate results. Other work has developed models

for operation under light-load conditions [67]. Furthermore, as presented in [185], TDA can model the parasitic capacitances and the dead-time of the modulation signal of the LLC converter, leading to more accurate models. Even dual-active CLLC models are available, as a general purpose converter [186] or orienting around a specific application like EV charging [187].

Other works have developed vector-based FHA [188] and TDA [68] to highlight LLC and LC-SR converter operation as a buck-mode current source. This mode can be used in certain applications like LCD and LED power supplies, PV, fuel cell and battery charging applications. The same work also comments on the disadvantages of the practical designs, like the significant overrating of the primary bridge transistors and the increase in the current stress. Other application-based TDA models are available for DCM boost mode LLC converters [189].

Generally, FDA provides models that are described by simple equations with low computational cost but are susceptible to inaccuracies when not properly used. On the other hand, TDA provides models with complex equations which are computationally demanding, but also capable of describing any operational region of the converter and provide the most accurate results.

However, there is a lack of closed-form solutions for the differential equations that describe the predominant resonant converters, like the full-bridge LC-SR and LLC, with a current-driven rectifying bridge, for the whole switching frequency range (greater, equal and less than the resonant). Furthermore, the conditions that separate each operating region within the capacitive operation are not analytically deduced, but only described as light- or heavy-load operation.

4.1.3 Structure and Contributions

In this chapter, the analytical time-domain model for the LC series-resonant (LC-SR) and LLC resonant single-active bridge converter is presented and the initial conditions are derived. This provides the exact voltage, current and instantaneous power waveforms for every switching region. Utilizing these equations allows for an in-depth understanding of the operation of the converter, and the voltage and current that the passive and active components should withstand.

For the LC-SR converter the boundary condition between the continuous and discontinuous current mode of the capacitive region is derived. This condition has as parameters the LC resonant circuit values, the load and the switching frequency, and it is experimentally verified. As long as the converter operates in the capacitive region, the DCM operation should be always be preferred compared to CCM, as it is more efficient. Also, from the time-domain analysis, the conditions that should be met in order to achieve zero-voltage or zero-current switching are obtained for each operation region.

For the LLC converter, the distinction between inductive and capacitive region is not as simple as in the LC-SR converter. For $f_s < f_0$ the LLC can still behave like operating in the inductive region, meaning that the current of the resonant circuit is lagging and during dead-time it passes through the antiparallel diodes of the switches, hence they experience ZVS-on. The different sub-regions of $f_s < f_0$ operations are explored (namely type A, B, and C), and the boundary conditions between them are discussed.

Furthermore, the criteria for proper selection of the passive components are presented, for a converter with switching frequency around 100 kHz, approximately 1 kW power-handling capability, DC bus voltage up to 400 V and peak currents up to 8 A. Several capacitor types are considered, but only two are proper for high-frequency applications with large alternating voltage swings. Off-the-shelf commercial inductors for high-frequency resonant applications are difficult to obtain. The tested cored inductors, even though oversized for this application, exceeded 100 ^{o}C, reducing the total efficiency. Hence, custom designs are mandatory in order to keep the temperatures relatively low and the efficiency high. Finally, a comparison between MOSFETs and IGBTs is made, along with differences introduced by the packaging of the components.

Publications:

- T. Papadopoulos and A. Antonopoulos, "Optimization of Gate Resistance and Dead-Time for ZVS and ZCS Operation based on the LC Series-Resonant Converter," under preparation.
- T. Papadopoulos, D. Kontos, and A. Antonopoulos, "Time-Domain Analysis of Full-Bridge Series-Resonant Converter and Boundary Conditions for DCM Operation," in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, Aalborg, Denmark, 2023, pp. 1-10.

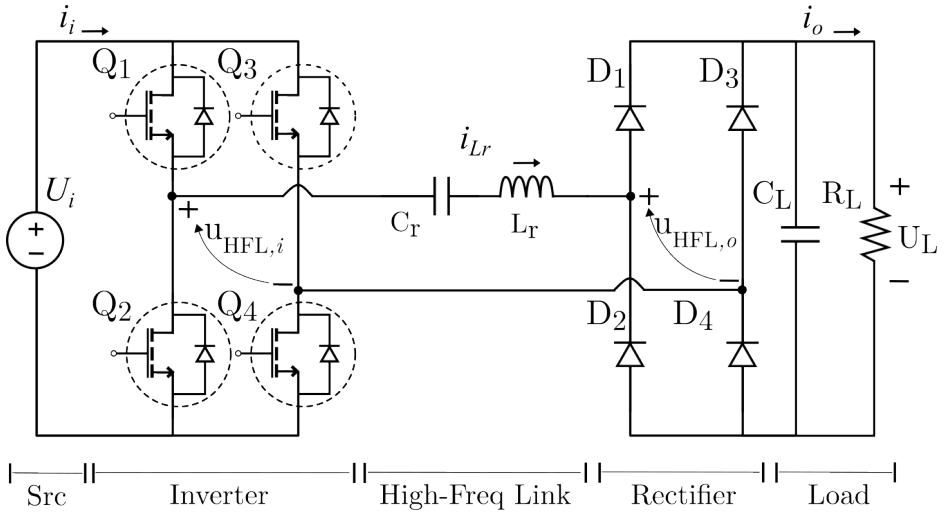


Figure 4.1 LC resonant converter.

4.2 LC Resonant Converter

The LC-series resonant (LC-SR) converter consists of an H-bridge inverter, a High-Frequency Link (HFL), a Full-Bridge Rectifier (FBR), and the load, as presented in Fig. 4.1. The H-bridge consists of two half-bridges and it is responsible for controlling the $u_{\mathrm{HFL},i}$, exciting the LC tank with a switching frequency f_s. The main advantage of this topology is that under certain conditions, the HFL enables the active components to switch state with zero (or nearly zero) losses. Furthermore, operating close to the resonant frequency can reduce the non-active power component and the electromagnetic radiation. The FBR converts the alternating current of the HFL to direct, and supplies it to the load, while the capacitor C_L is large enough to stabilize the output voltage.

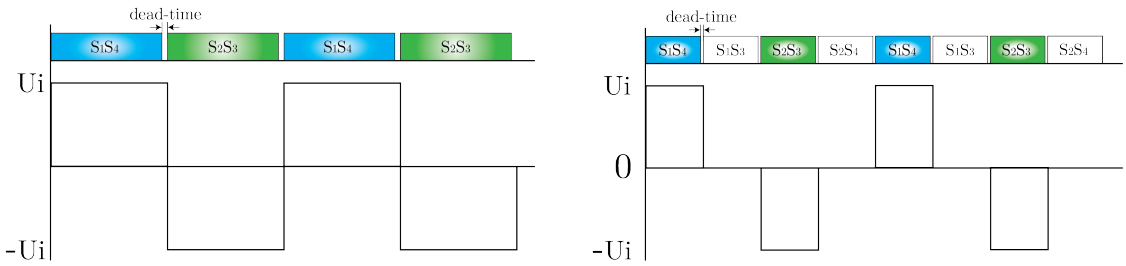
The circuit of Fig. 4.1 represents either a non-isolated resonant converter, or an isolated converter where the magnetizing inductance is much larger than the series-resonance inductance L_r and the components of the secondary side have been adjusted to the primary, as it will be discussed later.

4.2.1 LC-SR Converter Subsystems

4.2.1.1 Inverter Stage

The inverter stage consists of two half-bridges and four switching elements Q_1 to Q_4. This topology can achieve either two-level $\{+U_i, -U_i\}$ or three-level $\{+U_i, 0, -U_i\}$ output voltage, when the pairs $\{Q_1, Q_4\}$, $\{Q_2, Q_3\}$ or $\{Q_1, Q_4\}$, $\{Q_1, Q_3\}$, $\{Q_2, Q_3\}$, $\{Q_2, Q_4\}$ are conducting, respectively, as it is illustrated in Fig. 4.2.

Switching elements of the same half-bridge are prohibited to conduct at the same time, as this would result to short-circuit of the source. Real-world semiconductors cannot commutate



(a) 2 level output **(b)** 3 level output

Figure 4.2 Pulses and output voltage of the inverter stage.

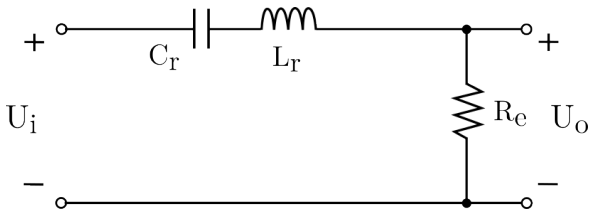


Figure 4.3 LC resonant high-frequency link circuit with power-equivalent load.

instantly from one state to the other, hence, a dead-time (or blanking-time) is required between each commutation, where the two control signals of the half-bridge are both set to low for a short time, as illustrated in Fig. 4.2. The dead-time is not taken into consideration for the time-domain model of the converter, but is examined during commutations, as it plays a major role on the (partial or full) soft-switching process.

4.2.1.2 High-Frequency Link (LC-Series)

The HFL consists of a capacitor C_r and an inductor L_r connected in series. As it is proved in [177], and extended in [190], the resistive load R_L can be adjusted to the output of the HFL, as it will be discussed later. The circuit is presented in Fig. 4.3, where the R_e is the power equivalent resistance of R_L.
The transfer function of the HFL, as presented in Fig. 4.3, can be easily deduced

$$G_{LC}(s) = \frac{sC_rR_e}{s^2L_rC_r + sC_rR_e + 1}, \tag{4.1}$$

and therefore the steady-state amplitude is

$$\frac{U_o}{U_i} = \frac{\omega C_rR_e}{\sqrt{(1-\omega^2L_rC_r)^2 + (\omega C_rR_e)^2}}, \tag{4.2}$$

and the phase

$$\theta = \arctan\left(\frac{1-\omega^2L_rC_r}{\omega R_eC_r}\right). \tag{4.3}$$

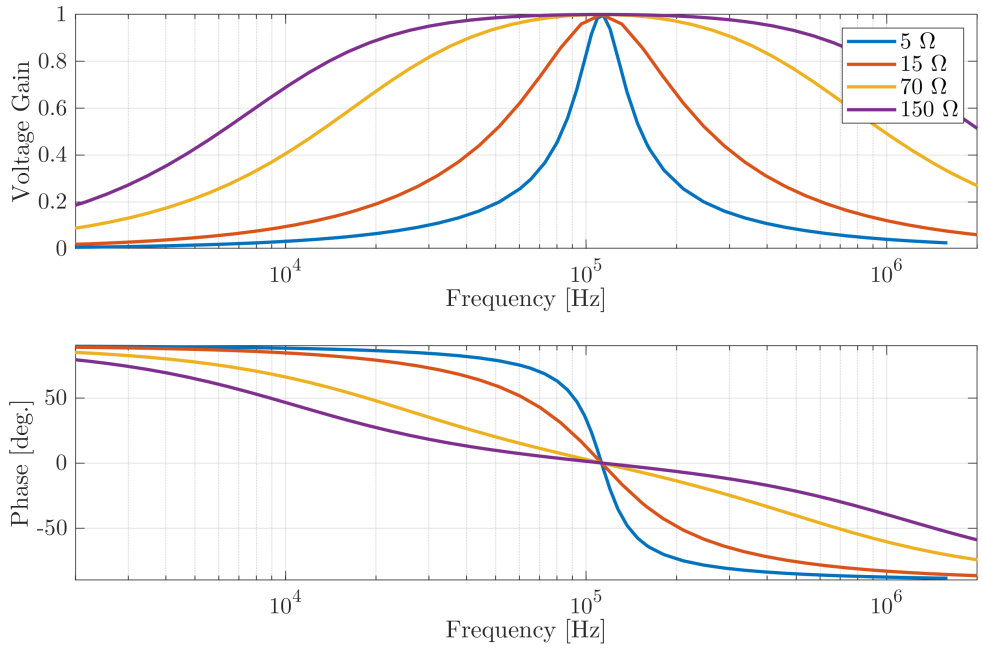


Figure 4.4 Bode diagram for $f_0 \approx 112$ kHz, $L = 20$ µH, $C = 100$ nF resonant circuit, with respect to different loads.

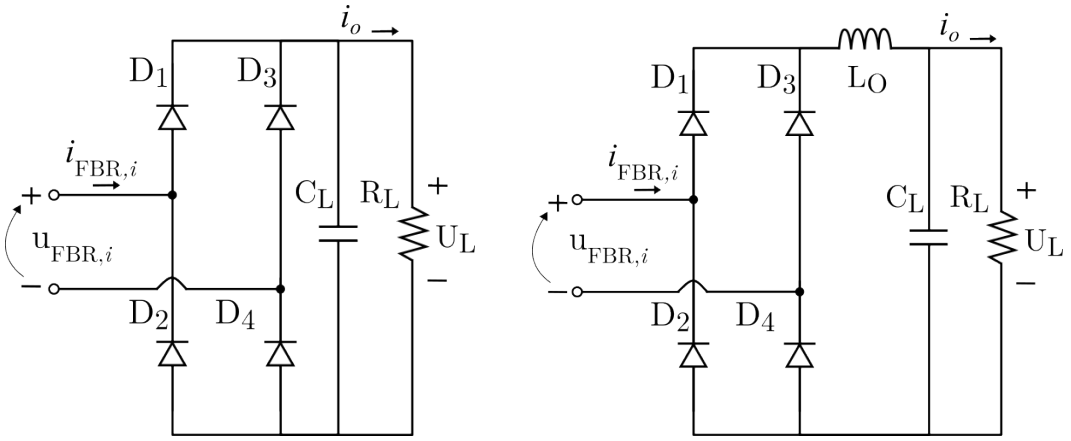
The Eqs. (4.2) and (4.3) can be rewritten as

$$\frac{U_o}{U_i} = \frac{1}{\sqrt{1 + \frac{1}{R_e^2}\frac{L_r}{C_r}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2}}, \quad \text{and}$$
$$\theta = \arctan\left(\frac{1}{R_e}\sqrt{\frac{L_r}{C_r}}\left(\frac{\omega_0}{\omega} - \frac{\omega}{\omega_0}\right)\right), \tag{4.4}$$

where the amplitude and the phase are given as a function of ω with respect to the resonance angular frequency $\omega_0 = 1/\sqrt{LC}$. From (4.4) it is easy to conclude that the global maximum is achieved for $\omega = \omega_0$, while for any other value of ω, the voltage gain will be less than 1.

This observation is verified in Fig. 4.4, where the voltage gain U_o/U_i and the phase difference θ are presented, with respect to different loads R_e. As the load increases (as the resistance decreases), the voltage gain curve becomes more steep. This means that for high loads small changes in the switching frequency results in large changes in output voltage. For smaller loads the output voltage remain almost constant in the vicinity of the resonance frequency.

While the quality factor $Q = \frac{\sqrt{L_r C_r}}{R_e}$ is commonly used to describe the stored vs. the dissipated energy of a filter, there is no benefit for utilizing it in power applications, since the resistance R_e does not represent the parasitics of the LC components, but an actual load.



(a) Current driven **(b)** Voltage driven

Figure 4.5 Full-bridge rectifier stage, with (a) a capacitor and (b) an inductor and a capacitor at the output.

Similarly, the bandwidth (BW) of a filter is a typical characteristic, which describes the frequency for which the amplitude is equal to $1/\sqrt{2}$. In resonant converters is not as useful, as the intension of the HFL is not to remove unwanted frequencies, but to create the proper conditions to achieve zero-voltage or zero-current switching. The BW is presented only for completeness sake, and it arises from

$$\frac{U_o}{U_i} = \frac{1}{\sqrt{2}} \Rightarrow \begin{cases} \omega_1 = -\frac{R_e}{2L_r} + \sqrt{\left(\frac{R_e}{2L_r}\right)^2 + \left(\frac{1}{\omega_0}\right)^2} \\ \omega_2 = \frac{R_e}{2L_r} + \sqrt{\left(\frac{R_e}{2L_r}\right)^2 + \left(\frac{1}{\omega_0}\right)^2} \end{cases},$$

resulting in

$$\mathrm{BW} = \omega_2 - \omega_1 = \frac{R_e}{L_r}, \tag{4.5}$$

which also concludes that as R_e decreases, the curve becomes more steep and the BW decreases. The opposite is true for the inductance L_r, as it decreases, the BW increases. Furthermore, from (4.5) it can be seen that the BW is independent of the capacitance C_r.

4.2.1.3 Full-Bridge Rectifier and Load

The behavior of the FBR depends on the circuitry at the output, which can be seen as the load of the converter. When the output stage of the bridge consists only of a capacitor C_L and a resistance R_L, as it is illustrated in Fig. 4.5a, the FBR acts like a current driven rectifier. When the current $i_{\mathrm{FBR},i} > 0$ (enters the + of the bridge), diodes D_1 and D_4 are conducting, and the input voltage is $+U_L$. When $i_{\mathrm{FBR},i} < 0$ (exits the + of the bridge),

diodes D_2 and D_3 are conducting, and the input voltage is $-U_L$. In the case that $i_{\mathrm{FBR},i} = 0$, the voltage $u_{\mathrm{FBR},i}$ is defined by the previous stage circuit. Conclusively,

$$u_{\mathrm{FBR},i} = \begin{cases} +U_L, & i_{\mathrm{FBR},i} > 0 \\ -U_L, & i_{\mathrm{FBR},i} < 0 \\ \text{depends on previous stage}, & i_{\mathrm{FBR},i} = 0. \end{cases} \tag{4.6}$$

The relation between R_L and R_e in this case is

$$R_e = \frac{8}{\pi^2} R_L, \tag{4.7}$$

as [177] provides by finding an equivalent alternating current resistance R_e that consumes the same amount of power as the direct current R_L does.

When the output stage contains also an inductor L_O, as illustrated in Fig. 4.5b, the FBR acts like a voltage-driven rectifier. When $u_{\mathrm{FBR},i} > 0$, the diodes D_1 and D_4 are conducting, therefore the current $i_{\mathrm{FBR},i} = +i_o$. When $u_{\mathrm{FBR},i} < 0$, the diodes D_2 and D_3 are conducting, therefore the current $i_{\mathrm{FBR},i} = -i_o$.

$$i_{\mathrm{FBR},i} = \begin{cases} +i_o, & u_{\mathrm{FBR},i} > 0 \\ -i_o, & u_{\mathrm{FBR},i} < 0 \end{cases}. \tag{4.8}$$

The relation between R_L and R_e in this case is

$$R_e = \frac{\pi^2}{8} R_L. \tag{4.9}$$

The introduction of the inductor L_O can substantially reduce the output current i_o ripple, but requires more space and increases the weight and losses of the converter. Therefore, in the context of this work, only the current driven FBR of Fig. 4.5a is considered. However, the following analysis can be easily adjusted to consider a voltage driven FBR.

4.2.2 Analysis and Operation

The conduction mode of the converter is defined by the shape of the current of the resonant inductor i_{Lr}, as follows: Discontinuous-Current Mode (DCM) when i_{Lr} is zero for an arbitrary time interval, and Continuous-Current Mode (CCM) when i_{Lr} crosses the zero point instantaneously. DCM operation is possible only when the switching frequency is below the resonance and the load is up to a certain value, as it will be proven later. In case the switching half-period is smaller than the natural half-period of the current, the converter operates in CCM.

The input voltage of the HFL ($U_{\mathrm{HFL},i}$) is dictated directly by the pair of switches which are conducting on the inverter side. The output voltage ($U_{\mathrm{HFL},o}$) depends on the resonant

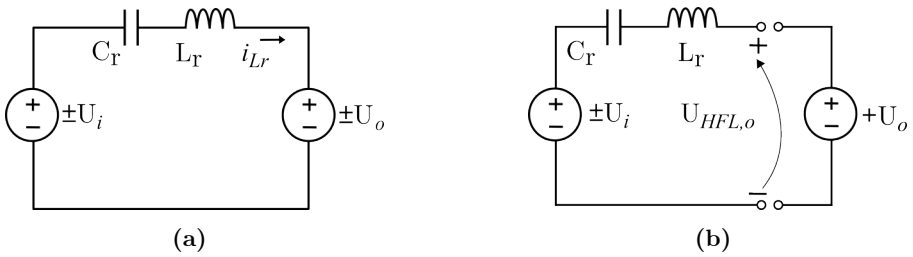


Figure 4.6 Simplified model of full-bridge LC-series circuit when resonant current i_{Lr} is (a) non-zero and the rectifier bridge is conducting, and (b) zero and the rectifier bridge is not conducting.

current. The rectifier bridge and the output capacitor C_L behave like a current-driven rectifier. When the diodes D_1 and D_4 are conducting, the output voltage of the HFL is $U_o = U_{\mathrm{HFL},o}$. Accordingly, when D_2 and D_3 are conducting the output voltage is $U_o = -U_{\mathrm{HFL},o}$. When the diodes are in cut-off state, the output voltage is equal the input voltage, as it is proven in subsection 4.2.2.3. In any case, all diodes change state under zero-current.

The equivalent simplified circuit under CCM is illustrated in Fig. 4.6a. In the case of DCM, the rectifier bridge is not conducting and the simplified circuit of this mode is presented in Fig. 4.6b.

The circuit of Fig. 4.6a can be described by

$$U_i - U_o = U_{L_r} + U_{C_r} = L_r \frac{\mathrm{d}}{\mathrm{d}t} i_{L_r} + \frac{1}{C} \int i_{L_r} \mathrm{d}t. \tag{4.10}$$

For $U_i - U_o = \text{const.}$, differentiating (4.10) with respect to t yields

$$L_r \frac{\mathrm{d}^2}{\mathrm{d}t^2} i_{L_r} + \frac{1}{C_r} i_{L_r} = 0. \tag{4.11}$$

The solution of (4.11) is

$$i_{L_r} = I_{L,0} \cos \omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \tag{4.12}$$

where:

- $I_{L,0} = i_{L_r}(0)$ is the initial condition of the inductor current,
- $U_{C,0} = U_{C_r}(0)$ is the initial condition of the capacitor voltage,
- $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$ is the resonance angular frequency,
- $Z_0 = \sqrt{\frac{L_r}{C_r}}$ is the characteristic impedance.

The voltage of the individual components of the HFL is

$$u_{L_r} = (U_i - U_o - U_{C,0}) \cos \omega_0 t - Z_0 I_{L,0} \sin \omega_0 t, \tag{4.13}$$

and

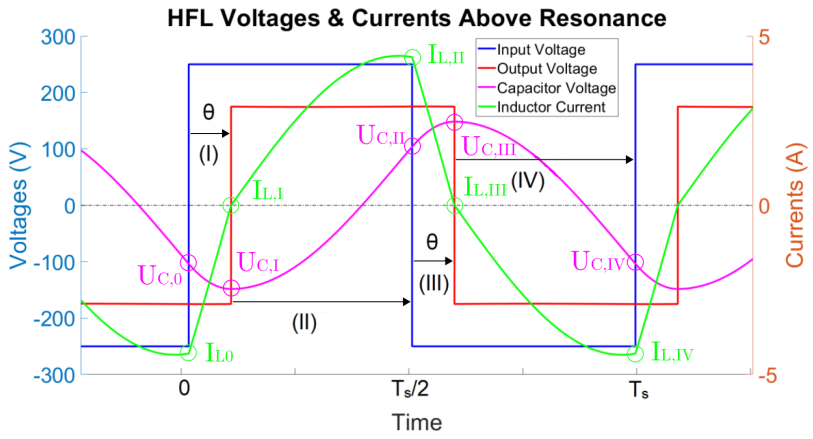


Figure 4.7 Current (i_{Lr}) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$, U_{Cr}) of the HFL for the inductance region.

$$u_{C_r} = U_i - U_o - (U_i - U_o - U_{C,0})\cos\omega_0 t + Z_0 I_{L,0}\sin\omega_0 t. \tag{4.14}$$

4.2.2.1 Operation at $f_s > f_0$ (Inductive Region)

This region is defined as inductive because (i) $X_L > X_C$ and (ii) the zero-crossing of the current through the HFL is lagging to the corresponding crossing of the HFL input voltage ($U_{\mathrm{HFL},i}$), as illustrated in Fig. 4.7.

Four time intervals are defined, based on the states of the input and the output voltages of the HFL, as follows

$$\begin{cases} \text{I:} & \{u_i(t) = +U_i \mid u_o(t) = -U_o\}, \ 0 \le t \le \frac{\theta}{2\pi}T_s, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\}, \ \frac{\theta}{2\pi}T_s \le t \le \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = -U_i \mid u_o(t) = +U_o\}, \ \frac{T_s}{2} \le t \le \frac{\theta+\pi}{2\pi}T_s, \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\}, \ \frac{\theta+\pi}{2\pi}T_s \le t \le T_s. \end{cases} \tag{4.15}$$

The terms $I_{L,I} - I_{L,IV}$ and $U_{C,I} - I_{C,IV}$ represent the final conditions of the inductor L_r currents and the capacitor C_r voltages, for each respective time interval. If operation in the steady state is assumed $I_{L,IV} = I_{L,0}$ and $U_{C,IV} = U_{C,0}$. The sign of the current i_{Lr} dictates the sign of $U_{\mathrm{HFL},o}$. Current continuity conditions dictate

$$I_{L,I} = I_{L,III} = 0. \tag{4.16}$$

The current of the HFL is described by

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0}\cos\omega_0 t + \frac{U_i+U_o-U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & \frac{U_i-U_o-U_{C,I}}{Z_0}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & I_{L,II}\cos\omega_0(t-\frac{T_s}{2}) - \frac{U_i+U_o+U_{C,II}}{Z_0}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & \frac{U_o-U_i-U_{C,III}}{Z_0}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s), \end{cases} \tag{4.17}$$

and the resonant inductor voltage by

$$u_{Lr} = \begin{cases} \text{I:} & (U_i+U_o-U_{C,0})\cos\omega_0 t - Z_0 I_{L,0}\sin\omega_0 t, \\ \text{II:} & (U_i-U_o-U_{C,I})\cos\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & -(U_i+U_o+U_{C,II})\cos\omega_0(t-\frac{T_s}{2}) - Z_0 I_{L,II}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & (U_o-U_i-U_{C,III})\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s). \end{cases} \tag{4.18}$$

Since $i_{Lr} = i_{Cr}$ and in steady-state operation the mean value of the current $\langle i_{Lr}\rangle = \langle i_{Cr}\rangle = 0$ and voltage $\langle u_{Lr}\rangle = 0$, the following conditions apply:

$$I_{L,0} = -I_{L,II},\ U_{C,0} = -U_{C,II},\ U_{C,I} = -U_{C,III}. \tag{4.19}$$

From the final condition of i_{Lr} in interval I

$$I_{L,I} = 0 = I_{L,0}cos\frac{\omega_0}{\omega_s}\theta + \frac{U_i+U_o-U_{C,0}}{Z_0}sin\frac{\omega_0}{\omega_s}\theta \Rightarrow \tan\frac{\omega_0}{\omega_s}\theta = \frac{Z_0 I_{L,0}}{U_{C,0}-U_i-U_o}. \tag{4.20}$$

Similarly, from the final conditions of interval IV

$$\left.\begin{aligned} I_{L,IV} = I_{L,0} &= \frac{U_o-U_i-U_{C,III}}{Z_0}\sin\frac{\omega_0}{\omega_s}\theta \\ U_{C,IV} = U_{C,0} &= U_o-U_i-(U_o-U_i-U_{C,III})\cos\frac{\omega_0}{\omega_s}(\pi-\theta) \end{aligned}\right\} \Rightarrow \tan\frac{\omega_0}{\omega_s}\theta = \frac{Z_0 I_{L,0}}{U_{C,0}-U_i-U_o}. \tag{4.21}$$

Finally, from (4.20) and (4.21), the initial conditions ($t = 0$) are given as

$$I_{L,0} = -\frac{2\frac{U_i}{Z_0}}{\cot\frac{\omega_0}{\omega_s}\theta + \cot\frac{\omega_0}{\omega_s}(\pi-\theta)} \tag{4.22}$$

$$U_{C,0} = U_o + U_i\left(1 - \frac{2\tan\frac{\omega_0}{\omega_s}(\pi-\theta)}{\tan\frac{\omega_0}{\omega_s}\theta + \tan\frac{\omega_0}{\omega_s}(\pi-\theta)}\right), \tag{4.23}$$

while the initial conditions for intervals I and III are

$$U_{C,I} = -U_{C,III} = U_i + U_o - (U_i + U_o - U_{C,0})\cos\frac{\omega_0}{\omega_s}\theta + Z_0 I_{L,0}\sin\frac{\omega_0}{\omega_s}\theta. \tag{4.24}$$

The power transfer is given from $p_i(t) = u_i(t)i_{Lr}(t)$ and $p_o(t) = u_o(t)i_{Lr}(t)$ for the input and output ports, respectively. Using (4.17) and (4.18) and applying the mean value, the active power is given

$$\begin{aligned} P_i = \frac{U_i}{\pi}\frac{\omega_s}{\omega_0}\Bigg(I_{L,0}\sin\frac{\omega_0}{\omega_s}\theta + \frac{U_i + U_o - U_{C,0}}{Z_0}\left(1 - \cos\frac{\omega_0}{\omega_s}\theta\right) \\ + \frac{U_i - U_o - U_{C,I}}{Z_0}\left(1 - \cos\frac{\omega_0}{\omega_s}(\pi - \theta)\right)\Bigg), \end{aligned} \tag{4.25}$$

$$\begin{aligned} P_o = \frac{U_o}{\pi}\frac{\omega_s}{\omega_0}\Bigg(-I_{L,0}\sin\frac{\omega_0}{\omega_s}\theta - \frac{U_i + U_o - U_{C,0}}{Z_0}\left(1 - \cos\frac{\omega_0}{\omega_s}\theta\right) \\ + \frac{U_i - U_o - U_{C,I}}{Z_0}\left(1 - \cos\frac{\omega_0}{\omega_s}(\pi - \theta)\right)\Bigg). \end{aligned} \tag{4.26}$$

In this region, the converter achieves ZVS during turn-on commutations, but turn-off commutations are forced through hard switching. For example, Q_1 and Q_4 are forced to turn-off when the current passing through is $I_{L,II}$. During the dead time this current flows through the antiparallel diodes of Q_2 and Q_3, which then turn-on with zero-voltage drop across. Note that as f_s approaches f_0, $I_{L,II}$ becomes smaller and the hard turn-off commutations produce less losses.

4.2.2.2 Operation at $f_s = f_0$ (Resonant Frequency)

As the inverter excites the HFL with its self-resonant frequency, (i) $X_L = X_C$ and (ii) the zero-crossing of the resonance current is in-phase to the corresponding crossing of the HFL input voltage ($U_{\mathrm{HFL},i}$), as illustrated in Fig. 4.8. As $U_{\mathrm{HFL},o}$ is in-phase with the HFL current, only two time intervals are defined, as in

$$\begin{cases} \text{I: } \{u_i(t) = +U_i | u_o(t) = +U_o\}, \ 0 \le t \le \frac{T_s}{2}, \\ \text{II: } \{u_i(t) = -U_i | u_o(t) = -U_o\}, \ \frac{T_s}{2} \le t \le T_s. \end{cases} \tag{4.27}$$

As in the previous mode, due to current and voltage continuity conditions, the following relations hold:

$$\begin{aligned} I_{L,0} = I_{L,I} = I_{L,II} = 0, \\ U_{C,0} = U_{C,II} = -U_{C,I}. \end{aligned} \tag{4.28}$$

Eqs. (4.17) and (4.18) can be simplified, using Eq. (4.28)

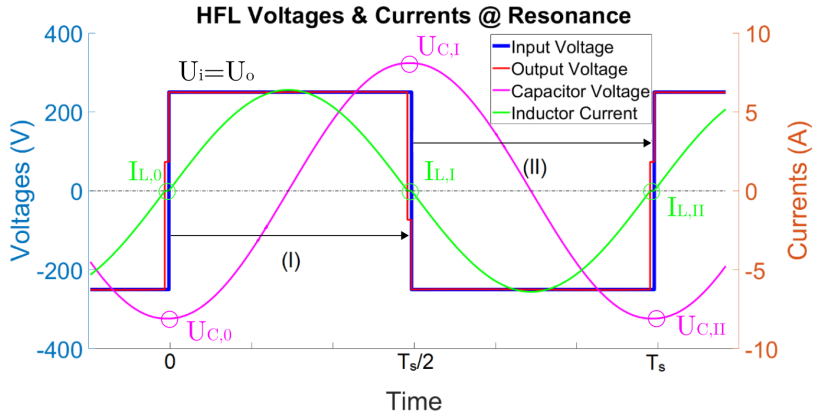


Figure 4.8 Current (i_{Lr}) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$, U_{Cr}) of the HFL at the resonance point.

$$i_{Lr} = \begin{cases} \text{I:} & \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t \\ \text{II:} & -\frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}) \end{cases} \Rightarrow i_{Lr} = \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \tag{4.29}$$

$$u_{Lr} = \begin{cases} \text{I:} & (U_i - U_o - U_{C,0}) \cos \omega_0 t \\ \text{II:} & -(U_i - U_o - U_{C,0}) \cos \omega_0 (t - \frac{T_s}{2}) \end{cases} \Rightarrow u_{Lr} = (U_i - U_o - U_{C,0}) \cos \omega_0 t. \tag{4.30}$$

The voltage of the resonant capacitor is given by

$$u_{Cr}(t) = U_i - U_o - (Ui - U_o - U_{C,0}) \cos \omega_0 t. \tag{4.31}$$

The active power through the HFL can be found as the mean value of the instantaneous power

$$\begin{aligned} P_i &= U_i \frac{2}{\pi} \frac{U_i - U_o - U_{C,0}}{Z_0}, \\ P_o &= U_o \frac{2}{\pi} \frac{U_i - U_o - U_{C,0}}{Z_0}, \end{aligned} \tag{4.32}$$

and since $P_i = P_o \Rightarrow U_i = U_o$. Hence, Eq. (4.32) can be rewritten as

$$P_i = P_o = -\frac{2}{\pi} \frac{U_i U_{C,0}}{Z0}. \tag{4.33}$$

Finally, the initial condition of the resonance capacitor is given by

$$-\frac{2}{\pi} \frac{U_i U_{C,0}}{Z0} = \frac{U_o^2}{R_L} \Rightarrow U_{C,0} = -U_i \frac{\pi}{2} \frac{Z_0}{R_L}. \tag{4.34}$$

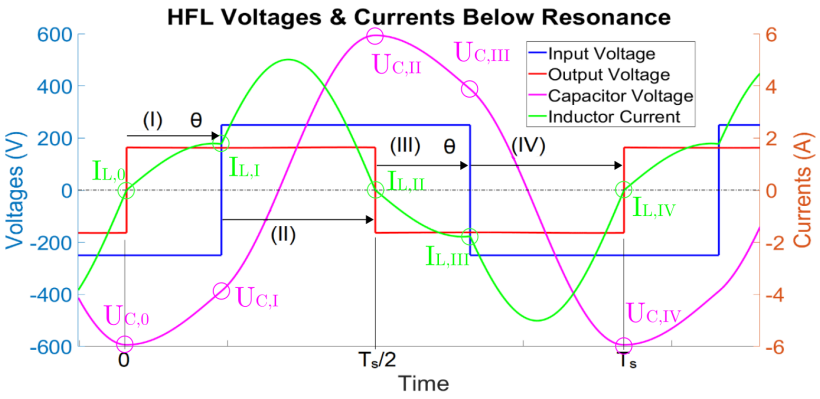


Figure 4.9 Current (i_{Lr}) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$, U_{Cr}) of the HFL for the capacitive region and CCM operation.

Hence, Eqs. (4.29) and (4.30) take their final form, as

$$\begin{aligned} i_{Lr}(t) &= \frac{\pi}{2}\frac{U_i}{R_L}\sin\omega_0 t, \\ u_{Cr}(t) &= -u_{Lr}(t) = -\frac{\pi}{2}\frac{U_i}{R_L}Z_0\cos\omega_0 t. \end{aligned} \tag{4.35}$$

In resonant operation all switches operate under ZCS, since the resonant current performs one half-cycle during each state of the inverter. When considering the effect of the dead-time, switches turn-off at a near-zero current, since the half-cycle has not been completed. In practice, knowing precisely the resonant frequency is not a trivial task since parasitic component come into play, and deviation from the nominal values of C_r and L_r is possible due to changes in temperature.

4.2.2.3 Operation at $\frac{f_0}{2} < f_s < f_0$ (Capacitive Region)

This region is defined as capacitive because (i) $X_C > X_L$ and (ii) the fact that the first harmonic of the resonant current, in both CCM and DCM operations is leading the input voltage of the HFL. Switching frequencies below $f_0/2$ will not be considered in this analysis, since the RMS current is significantly increased, and resonant converters are not usually designed to operate in such low frequencies.

Continuous Current Mode (CCM) An indicative case of this operation is presented in Fig. 4.9, along with the intervals for each switching state of the converter. The voltages of the simplified model of Fig. 4.6a are

$$\begin{cases} \text{I:} & \{u_i(t) = -U_i \mid u_o(t) = +U_o\},\ 0 \le t \le \frac{\theta}{2\pi}T_s, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\},\ \frac{\theta}{2\pi}T_s \le t \le \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = +U_i \mid u_o(t) = -U_o\},\ \frac{T_s}{2} \le t \le \frac{\theta+\pi}{2\pi}T_s, \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\},\ \frac{\theta+\pi}{2\pi}T_s \le t \le T_s. \end{cases} \tag{4.36}$$

As explained in the inductive region subsection, by definition $I_{L,IV} = I_{L,0}$ and $U_{C,IV} = U_{C,0}$. The sign of the current i_{Lr} dictates the sign of U_o and by current continuity conditions

$$I_{L,0} = I_{L,II} = 0. \tag{4.37}$$

The current through the HFL, in the four different intervals, is described by

$$i_{Lr} = \begin{cases} \text{I:} & -\frac{U_i+U_o+U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & I_{L,I}\cos\omega_0(t-\frac{\theta}{2\pi}T_s) + \frac{U_i-U_o-U_{C,I}}{Z_0}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & \frac{U_i+U_o+U_{C,II}}{Z_0}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & I_{L,III}\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) + \frac{U_o-U_i-U_{C,III}}{Z_0}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s), \end{cases} \tag{4.38}$$

and the resonant inductor voltage by

$$u_{Lr} = \begin{cases} \text{I:} & -(U_i+U_o+U_{C,0})\cos\omega_0 t, \\ \text{II:} & (U_i-U_o-U_{C,I})\cos\omega_0(t-\frac{\theta}{2\pi}T_s) - Z_0 I_{L,I}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & (U_i+U_o-U_{C,II})\cos\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & (U_o-U_i-U_{C,III})\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) - Z_0 I_{L,III}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s). \end{cases} \tag{4.39}$$

Since $\langle i_{Lr}\rangle = \langle i_{Cr}\rangle = 0$ and $\langle u_{Lr}\rangle = 0$

$$I_{L,I} = -I_{L,III},\ U_{C,0} = -U_{C,II},\ U_{C,I} = -U_{C,III}. \tag{4.40}$$

Following the same steps as before, the initial conditions of interval II are

$$I_{L,I} = -\frac{2\frac{U_i}{Z_0}}{\cot\frac{\omega_0}{\omega_s}\theta - \cot\frac{\omega_0}{\omega_s}(\pi-\theta)}, \tag{4.41}$$

$$U_{C,I} = -U_o + U_i\left(1 - \frac{2\tan\frac{\omega_0}{\omega_s}\theta}{\tan\frac{\omega_0}{\omega_s}\theta - \tan\frac{\omega_0}{\omega_s}(\pi-\theta)}\right), \tag{4.42}$$

while the initial conditions for intervals I and III are

$$U_{C,0} = -U_{C,II} = U_o - U_i - (U_o - U_i + U_{C,I})\cos\frac{\omega_0}{\omega_s}(\pi-\theta) + Z_0 I_{L,I}\sin\frac{\omega_0}{\omega_s}(\pi-\theta). \quad (4.43)$$

The active power passing through the HFL

$$\begin{aligned} P_i = \frac{U_i}{\pi}\frac{\omega_s}{\omega_0}\Bigg(& I_{L,I}\sin\frac{\omega_0}{\omega_s}(\pi-\theta) + \frac{U_i + U_o + U_{C,0}}{Z_0}\left(1-\cos\frac{\omega_0}{\omega_s}\theta\right) \\ & + \frac{U_i - U_o - U_{C,I}}{Z_0}\left(1-\cos\frac{\omega_0}{\omega_s}(\pi-\theta)\right)\Bigg), \end{aligned} \quad (4.44)$$

$$\begin{aligned} P_o = \frac{U_o}{\pi}\frac{\omega_s}{\omega_0}\Bigg(& I_{L,I}\sin\frac{\omega_0}{\omega_s}(\pi-\theta) - \frac{U_i + U_o + U_{C,0}}{Z_0}\left(1-\cos\frac{\omega_0}{\omega_s}\theta\right) \\ & + \frac{U_i - U_o - U_{C,I}}{Z_0}\left(1-\cos\frac{\omega_0}{\omega_s}(\pi-\theta)\right)\Bigg). \end{aligned} \quad (4.45)$$

In the CCM operation, all switches experience hard switching at turn-on and ZVS at turn-off. For example, when Q_1 and Q_4 are conducting, the commutation occurs under a negative current $I_{L,III}$, which means that the voltage across the switch is clamped by the antiparallel (or body) diode.

Discontinuous Current Mode (DCM) DCM is possible only in the capacitive region and for specific combinations of output power and switching frequency, as it will be presented later. In this mode, when $i_{Lr} \neq 0$ and the rectifier diodes are conducting, the simplified model of Fig. 4.6a applies. When the current goes to zero, the rectifier is cut off and the voltage of the load differs from the output voltage of the HFL, as it is illustrated in Fig. 4.6b. The duration under which the current is zero depends only on the switching frequency and the resonance frequency of the HFL, as in

$$\tau_{\mathrm{DCM}} = \pi\left(\frac{1}{\omega_s} - \frac{1}{\omega_0}\right). \quad (4.46)$$

During this time, $U_{\mathrm{HFL},o} = U_i - U_{C,0}$. An indicative case of DCM operation is presented in Fig. 4.10, along with the intervals where the converter operates in different states.

$$\begin{cases} \text{I:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\},\ 0 \le t \le \frac{\pi}{\omega_0}, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = U_i + U_{C,0}\},\ \frac{\pi}{\omega_0} \le t \le \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\},\ \frac{T_s}{2} \le t \le \pi\left(\frac{1}{\omega_s} + \frac{1}{\omega_0}\right), \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = -U_i - U_{C,0}\},\ \pi\left(\frac{1}{\omega_s} + \frac{1}{\omega_0}\right) \le t \le T_s. \end{cases} \quad (4.47)$$

By definition of DCM, the initial current of each region is zero, hence $I_{L,0} = I_{L,I} = I_{L,II} = I_{L,III} = I_{L,IV} = 0$. The voltage and current of the resonant inductor are

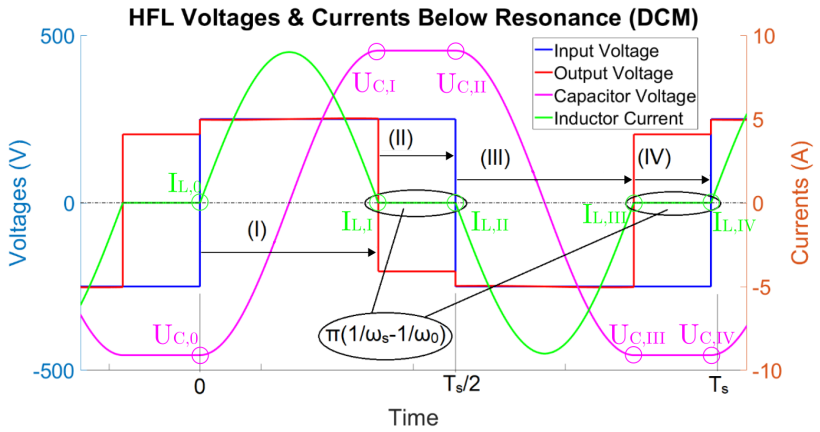


Figure 4.10 Current (i_{Lr}) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$, U_{Cr}) of the HFL for the capacitive region and DCM operation.

$$i_{Lr} = \begin{cases} \text{I:} & \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} & 0, \\ \text{III:} & -\frac{U_i - U_o + U_{C,II}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV:} & 0, \end{cases} \tag{4.48}$$

$$u_{Lr} = \begin{cases} \text{I:} & (U_i - U_o - U_{C,0}) \cos \omega_0 t, \\ \text{II:} & 0, \\ \text{III:} & -(U_i - U_o + U_{C,II}) \cos \omega_0 (t - \frac{T_s}{2}), \\ \text{IV:} & 0. \end{cases} \tag{4.49}$$

Due to voltage continuity conditions, and since $\langle i_{Lr} \rangle = \langle i_{Cr} \rangle = 0$

$$U_{C,I} = U_{C,II},\ U_{C,0} = U_{C,III} = U_{C,IV},\ U_{C,0} = -U_{C,I} \tag{4.50}$$

apply.

Similarly to resonance region subsection, the active power is given by

$$\begin{aligned} P_i &= U_i \frac{2}{\pi} \frac{\omega_s}{\omega_0} \frac{U_i - U_o - U_{C,0}}{Z_0}, \\ P_o &= U_o \frac{2}{\pi} \frac{\omega_s}{\omega_0} \frac{U_i - U_o - U_{C,0}}{Z_0}, \end{aligned} \tag{4.51}$$

and since $P_i = P_o \Rightarrow U_i = U_o$. Hence, Eq. (4.51) can be written as

$$P_i = P_o = -\frac{2}{\pi} \frac{\omega_s}{\omega_0} \frac{U_i U_{C,0}}{Z0}. \tag{4.52}$$

Finally, the initial condition of the resonant capacitor is given by

$$-\frac{2}{\pi}\frac{\omega_s}{\omega_0}\frac{U_i U_{C,0}}{Z0} = \frac{U_o^2}{R_L} \Rightarrow U_{C,0} = -U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}. \tag{4.53}$$

Hence, $i_{Lr}(t)$ and $u_{Cr}(t)$ can be written as

$$i_{Lr} = \begin{cases} \text{I:} & \frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{U_i}{R_L}\sin\omega_0 t, \\ \text{II:} & 0, \\ \text{III:} & -\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{U_i}{R_L}\sin\omega_0, (t-\frac{T_s}{2}) \\ \text{IV:} & 0, \end{cases} \tag{4.54}$$

$$u_{Cr} = \begin{cases} \text{I:} & -U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}\cos\omega_0 t, \\ \text{II:} & U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}, \\ \text{III:} & U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}\cos\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & -U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}. \end{cases} \tag{4.55}$$

The peak current of the HFL and the peak voltage of the capacitor can be easily deduced as in

$$\begin{aligned} I_{Lr,\mathrm{MAX}} &= \frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{U_i}{R_L}, \\ U_{Cr,\mathrm{MAX}} &= U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}. \end{aligned} \tag{4.56}$$

As already explained, in the DCM operation all switches commutate under ZCS, since the current is zero during turn-off of the switches, and has a relatively small slope (when compared to the corresponding voltage drop) during turn-on.

Boundary Condition Below a specific switching frequency f_s and for a load higher than a certain value (below a specific R_L), the converter operates at CCM. The conditions for this transition between CCM and DCM are interesting for controlling the converter and optimize the switching losses.

Starting from CCM conditions, as shown in Fig. 4.9, the boundary between the CCM-DCM can be deduced from the instants when the current is zero, i.e., $I_{L,0}$, $I_{L,II}$. From Kirchhoff voltage law $U_i + U_o + U_{C,0} = 0$ at the boundary operation. However, the property $U_i = U_o$ of DCM region is also true. Furthermore the voltage of the resonant capacitor is given from (4.53), hence

$$2U_i = -U_{C,0} = U_i\frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L} \Rightarrow \frac{\pi}{4}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L} = 1. \tag{4.57}$$

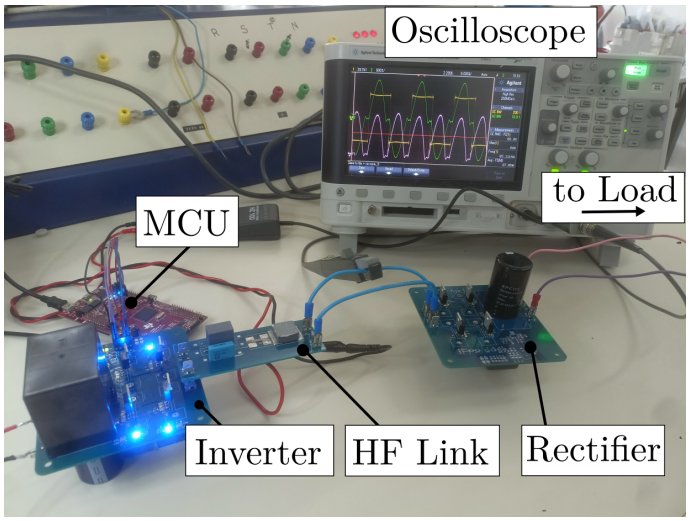


Figure 4.11 Experimental setup.

Table 4.1 Experimental setup parameters.

C_r	L_r	f_0	Z_0	R_{BD}
39 nF	63.4 μH	100 kHz	40.32 Ω	25.33 Ω @ 80 kHz

Eq. (4.57) provides the boundary between DCM and CCM operation. By solving for any variable, the corresponding boundary value can be extracted as

$$R_{L,BD} = Z_0 \frac{\pi}{4} \frac{\omega_0}{\omega_s} \Rightarrow \begin{cases} R_L > R_{L,BD} \Rightarrow \text{DCM} \\ R_L < R_{L,BD} \Rightarrow \text{CCM} \end{cases} \tag{4.58}$$

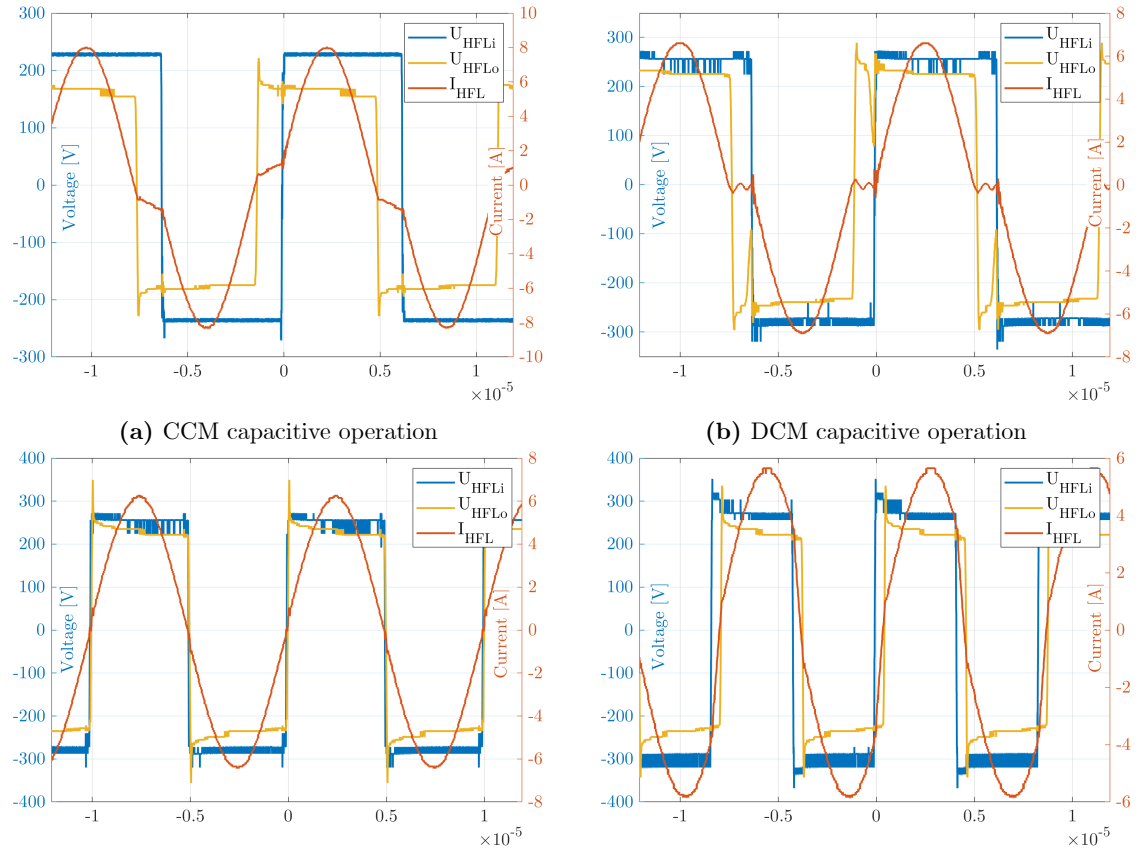
$$f_{s,BD} = f_0 \frac{\pi}{4} \frac{Z_0}{R_L} \Rightarrow \begin{cases} f_s > f_{s,BD} \Rightarrow \text{DCM} \\ f_s < f_{s,BD} \Rightarrow \text{CCM} \end{cases} \tag{4.59}$$

Note that for $R_L < \frac{\pi}{4} Z_0$, the boundary condition of switching frequency f_s exceeds that of the resonant f_0, therefore, the converter operates in CCM region, for any f_s value.

4.2.2.4 Experimental Verification

For the laboratory verification, a high-frequency high-density inverter is developed. The HFL and the rectifier bridge are designed as separate boards in order to facilitate the measuring procedures. The converter and the measuring devices are illustrated in Fig. 4.11 and the experimental parameters are given in Table 4.1.

The CCM operation of the converter is illustrated in Fig. 4.12a and is in agreement with the previous analysis and Fig. 4.9. In the DCM operation, however, the parasitic



(a) CCM capacitive operation

(b) DCM capacitive operation

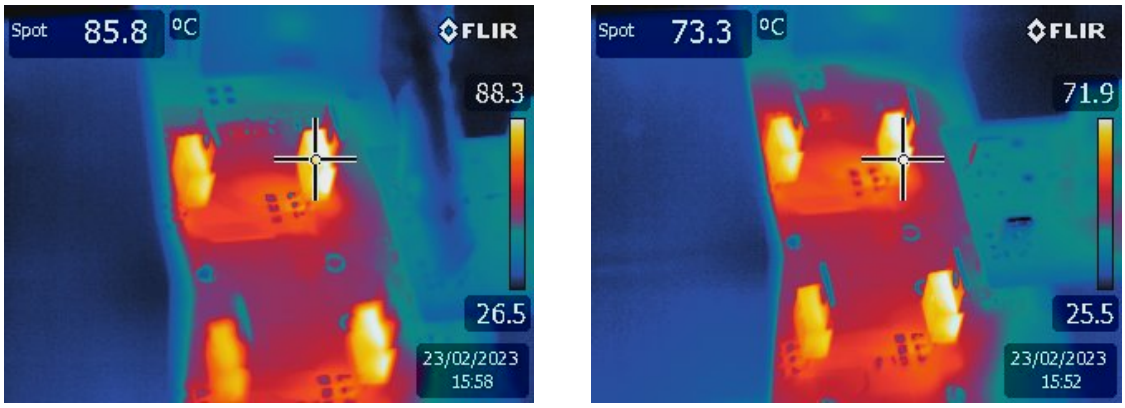
(c) Resonant operation

(d) Inductive operation

Figure 4.12 Experimental waveforms of the current and the input and the output voltage of the HFL for approximately $P_{\text{INV}} = 1$ kW, (a) CCM operation with $R_L = 23.3\ \Omega$ and $f_s = 80$ kHz, (b) DCM operation with $R_L = 32.6\ \Omega$ and $f_s = 80$ kHz, (c) resonance operation at $f_s = 100$ kHz, and (d) inductive operation with $f_s = 120$ kHz.

capacitances of the circuit, in combination with the HFL inductor, result in a small oscillation of the current during the zero-current intervals, as illustrated in Fig. 4.12b. This also affects the $U_{\text{HFL},o}$, since the rectifier bridge does not fully turn off. Nevertheless, the oscillation is quickly damped and the commutation of the switches occurs with $i_{Lr} < 0.1$ A, thus under near-zero current. The different voltage levels of $U_{\text{HFL},i}$ and $U_{\text{HFL},o}$ are caused due to the voltage drop at the inductor and it depends on the current I_{HFL}.

The resonant and inductive operation regions are illustrated in Fig. 4.12c and 4.12d, respectively. The laboratory behavior is in agreement with the aforementioned analysis and simulations. As it is expected, voltage overshoots are present when the converter changes state and the current commutates from one leg of the inverter or the rectifier bridge to the other.



(a) CCM operation **(b)** DCM operation

Figure 4.13 Thermal image of the inverter switches, illustrating the case temperature of one switch, for (a) CCM and (b) DCM operation.

For the same amount of input power $P_i = 150$ W, the thermal image of the inverter is illustrated in Fig. 4.13, for CCM and DCM operation, respectively. The images are caught with a FLIR E60 thermal camera.

It can be noted that heatsinks are not employed in these experiments, so the thermal effect on the case temperature is amplified at relatively low power levels. The case temperature increases with semiconductor losses (conduction and switching), meaning that higher losses lead to higher case temperature. Hence, as it is presented in Fig. 4.13 the CCM operation is less efficient compared to the DCM.

A rough estimate of the losses can be given based on the junction to ambient thermal resistance $R_{\text{th,J-A}}$. For the SiHP25N50E MOSFET $R_{\text{th,J-A}} = 61.5$ °C/W and for an ambient temperature of 20 °C, the losses on the illustrated switch are roughly 1.07 W for the CCM and 0.87 W for the DCM operation, respectively. This difference is partially caused by the non-zero switching loss of the CCM operation, but also from the slightly higher RMS current (since the output voltage is slightly reduced), as can be observed in Fig. 4.12a.

It is worth mentioning that experimentally demonstrating the effect of the switching losses individually is not easy. A fair comparison would require not just equal amount of input power, but also equal output voltage and RMS current. However, each operating region has different characteristics, i.e., DCM capacitive and resonant regions present $U_i = U_L$, while CCM capacitive and inductive regions exhibit $U_i > U_L$. In order to maintain a constant power level for all regions, the load, the input voltage or the switching frequency should be adjusted.

Keeping the input voltage constant, a comparison is made, for different input-power levels to confirm the more efficient behavior of DCM. The experiments were performed on two implementations: one using the SiHP25N50E MOSFETs and a second the FGPF15N60UNDF IGBTs. The bipolar device was employed in order to amplify loss effects due to the switch-

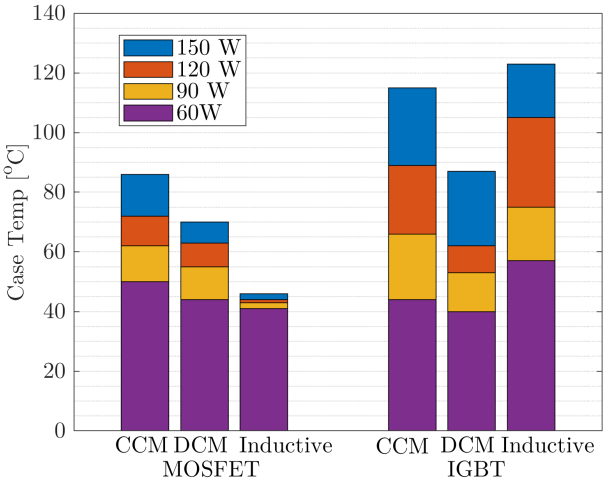


Figure 4.14 Losses for MOS and IGBT switches, with respect to the operation region and the input power.

ing behavior. As can be observed in Fig. 4.13 the DCM operation is always preferable to the CCM, both for the unipolar and for the bipolar device, since the case temperature is lower. However, when comparing DCM to inductive region of operation, the type of the semiconductor has a significant effect.

An interesting observation made from Fig. 4.13 is that the MOSFET device, while operating in the inductive region, presents a small rise in case temperature as the input power increases. This remark provides promising results for achieving high-power levels with very high-efficiency figures. Without employing a heatsink or forced-air cooling, inductive operation achieved 1.1 kW of power with an efficiency approximately 95%, as it is electrically measured from the two DC sides. It should also be noted that while the inductive operation provides the best results for the MOSFET, in the IGBT case the inductive operation is the less efficient.

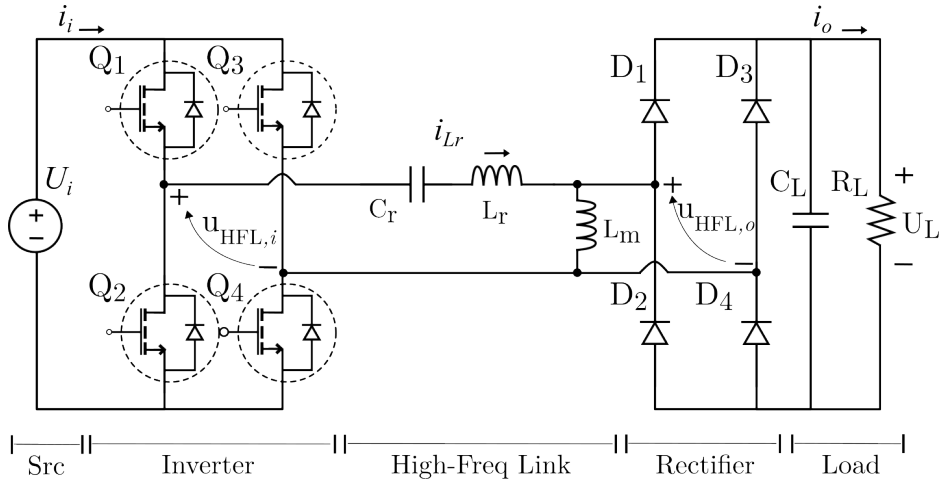


Figure 4.15 LLC resonant converter.

4.3 LC Resonant Converter with Isolation (LLC)

The LLC topology is a resonant converter, capable of zero-voltage or zero-current switching when operating under the proper conditions, hence providing high-efficiency figures. Like LC-SR converter, it consists of a primary and a secondary bridge and a resonant tank (or high-frequency link) connecting the two. The resonant tank consists of a capacitor and a inductor connected in series, with an additional transverse inductor, as illustrated in Fig. 4.15. This inductor corresponds to the magnetizing inductance of the isolation transformer. In order to further reduce the cost and total volume, the resonant and magnetizing inductors can both be parts of one transformer, taking advantage of the inherent leakage inductance.

The role of the primary and secondary bridges stand the same as in the LC-SR case, and are not rediscussed here. The behavior of the high-frequency link (HFL) changes, especially for switching frequencies f_s below the resonant f_0, as it is shown in subsection 4.3.1. The effect it has on the operation of the bridges is considered in subsection 4.3.2, along with the time-domain model and the mandatory conditions for ZVS or ZCS for the semiconductors.

4.3.1 High-Frequency Link (LLC)

The HFL consists of a capacitor C_r and an inductor L_r connected in series, and a second typically larger transverse inductor L_m, as it is illustrated in Fig. 4.16. The transfer function is

$$G_{LLC}(s) = \frac{s^2 L_m C_r R_e}{s^3 L_r L_m C_r + s^2 (L_m + L_r) C_r R_e + s L_m + R_e} \tag{4.60}$$

and therefore, the steady-state amplitude is

$$\frac{U_o}{U_i} = \frac{\omega^2 L_m C_r R_e}{\sqrt{(\omega^2(L_m + L_r)C_r R_e - R_e)^2 + (\omega^3 L_m L_r C_r - \omega L_m)^2}} \tag{4.61}$$

and the phase

$$\theta = \arctan\left(\frac{\omega L_m - \omega^3 L_m L_r C_r}{\omega^2(L_m + L_r)R_e C_r - R_e}\right). \tag{4.62}$$

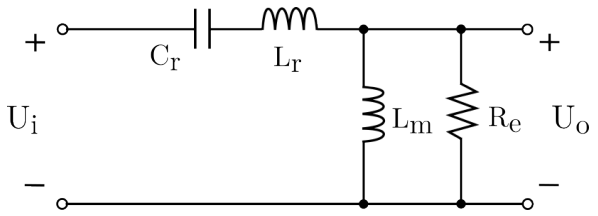


Figure 4.16 LLC resonant high-frequency link circuit with power-equivalent load.

The LLC presents two resonant frequencies, one is produced by L_r and C_r as in

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4.63}$$

and the other by the sum $L_r + L_m$ and C_r as in

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}. \tag{4.64}$$

The power equivalent resistance $R_e = \frac{\pi^2}{8} R_L$ remains the same as in the LC case.

Another major difference between LC and LLC HFLs is illustrated in Fig. 4.17, where different ratios of L_m/L_r are considered. When the ratio is less than 30, operating in the region $f_s < f_0$ results in an increase of the output voltage. However, when the ratio is greater than 30, the bode diagram resembles that of the LC-SR converter, with a global maximum gain of 1 near the resonant frequency f_0.

Similar observations can be made when different R_e loads are considered, as it is presented in Fig. 4.18. For low loads (high R_e values), switching at frequencies below resonant can result in a voltage gain much higher than 1. As the load increases (R_e becomes smaller), the HFL resembles more that of the LC-SR converter, which maximum voltage gain of 1 at f_0.

4.3.2 Analysis and Operation

The LLC converter can be analyzed in a similar manner as the LC-SR converter of Section 4.2. There are two simplified circuits, illustrated in Fig. 4.19, depending on the state of the converter. When power flows from the primary to the secondary bridge Fig. 4.19a applies, and the converter is described by

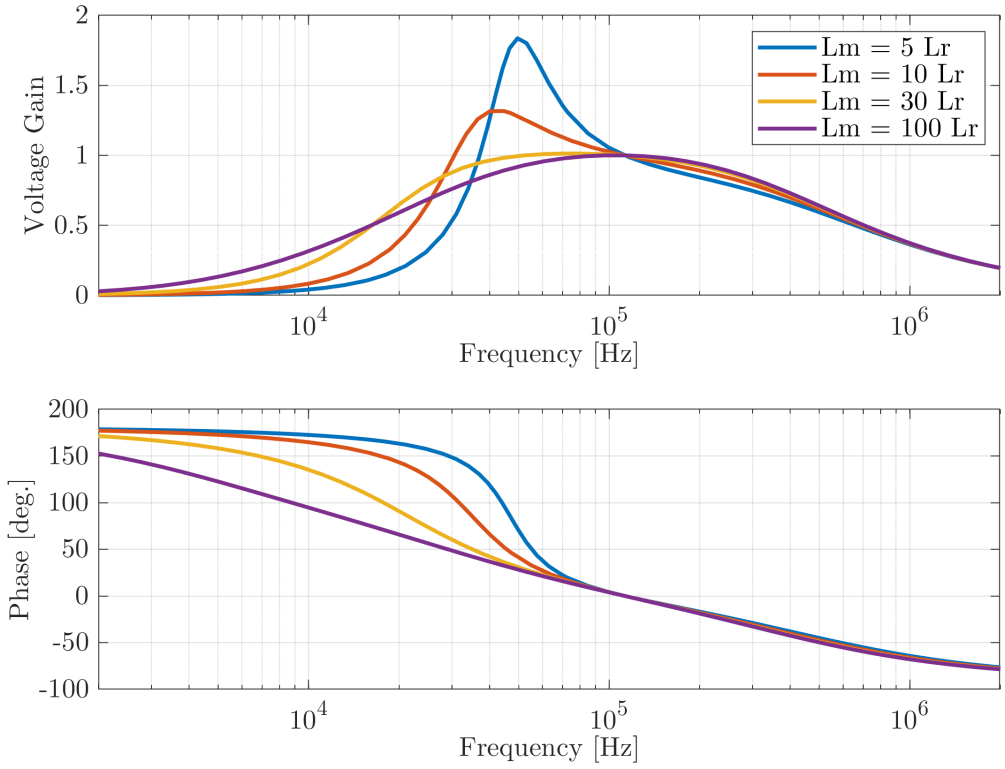


Figure 4.17 Bode diagram for $f_0 \approx 112$ kHz, $L = 20$ µH, $C = 100$ nF resonant circuit, with respect to different ratios L_m/L_r.

$$U_i - U_o = u_{Cr} + u_{Lr} = L_r \frac{\mathrm{d}}{\mathrm{d}t} i_{Lr} + \frac{1}{C_r} \int i_{Lr} \mathrm{d}t. \tag{4.65}$$

Similar to the LC-SR case, for $U_i - U_o = \text{const.}$, differentiating (4.65) with respect to t yields

$$L_r \frac{\mathrm{d}^2}{\mathrm{d}t^2} i_{L_r} + \frac{1}{C_r} i_{L_r} = 0. \tag{4.66}$$

The solution of (4.66) is

$$i_{L_r} = I_{L,0} \cos \omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \tag{4.67}$$

where:

- $I_{L,0} = i_{L_r}(0)$ is the initial condition of the inductor current,
- $U_{C,0} = U_{C_r}(0)$ is the initial condition of the capacitor voltage,
- $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$ is the resonance angular frequency,
- $Z_0 = \sqrt{\frac{L_r}{C_r}}$ is the characteristic impedance.

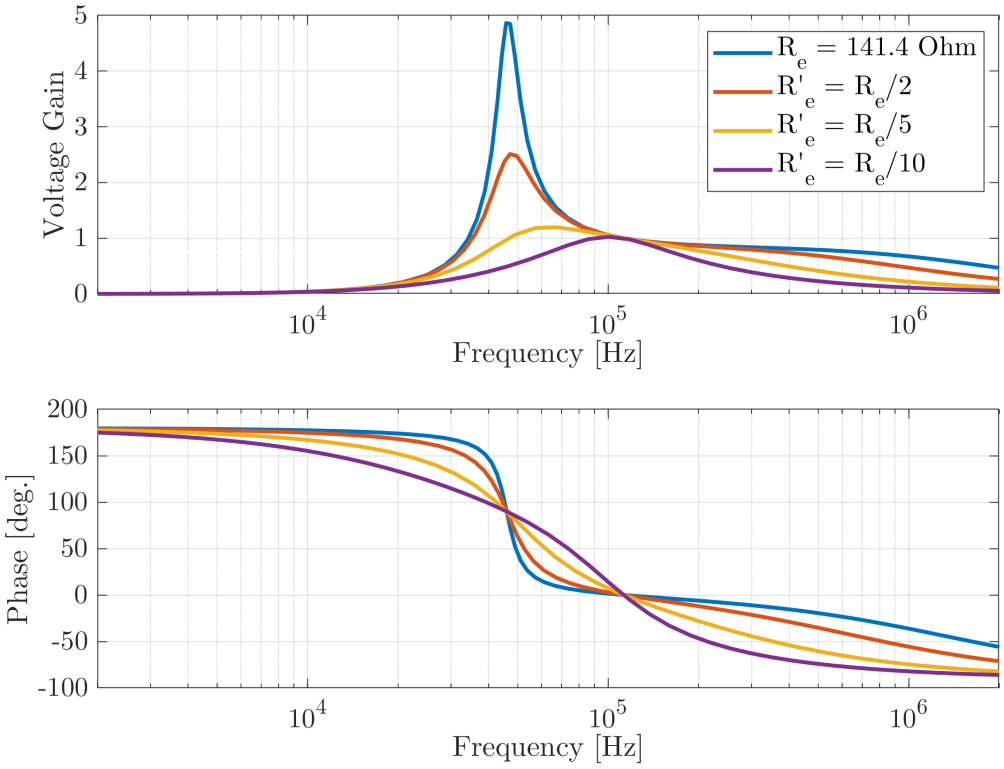


Figure 4.18 Bode diagram for $f_0 \approx 112$ kHz, $L = 20$ µH, $C = 100$ nF resonant circuit, with respect to different loads.

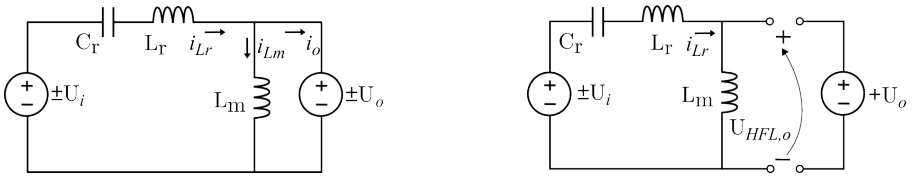


Figure 4.19 Simplified model of full-bridge LLC circuit when the rectifier bridge is (a) conducting, and (b) not conducting.

The voltage of the inductor L_r is

$$u_{L_r} = (U_i - U_o - U_{C,0}) \cos \omega_0 t - Z_0 I_{L,0} \sin \omega_0 t, \tag{4.68}$$

and the voltage of the capacitor C_r

$$u_{C_r} = U_i - U_o - (U_i - U_o - U_{C,0}) \cos \omega_0 t + Z_0 I_{L,0} \sin \omega_0 t. \tag{4.69}$$

The voltage drop across L_m is constant and equal to U_o, so

$$i_{Lm} = \frac{U_o}{L_m} t + I_{Lm,0}, \tag{4.70}$$

where $I_{Lm,0}$ is the initial condition of the magnetizing inductor current. When a square-wave voltage is applied across it, the current forms a triangular waveform, with zero mean value.

From Kirchhoff's current law, the current flowing through the equivalent U_o source is

$$i_o = i_{Lr} - i_{Lm}. \tag{4.71}$$

When no power is flowing from the primary to the secondary bridge, the converter is in load cutoff (or freewheeling) operation. The equivalent simplified circuit is presented in Fig. 4.19b. As the current of the rectifier bridge is zero, the bridge does not conduct and the magnetizing inductor L_m is connected in series with the resonant capacitor C_r and inductor L_m. In this case, the converter is described by

$$U_i = u_{Cr} + u_{Lr} + u_{Lm} = (L_r + L_m)\frac{\mathrm{d}}{\mathrm{d}t} i_{Lr} + \frac{1}{C_r}\int i_{Lr}\mathrm{d}t, \tag{4.72}$$

and differentiating with respect to t

$$(L_r + L_m)\frac{\mathrm{d}^2}{\mathrm{d}t^2} i_{L_r} + \frac{1}{C_r} i_{L_r} = 0. \tag{4.73}$$

The solution of 4.73 is

$$i_{L_r} = I_{L,0}\cos\omega_m t + \frac{U_i - U_{C,0}}{Z_m}\sin\omega_m t, \tag{4.74}$$

- $I_{L,0} = i_{L_r}(0)$ is the initial condition of the inductor current,
- $U_{C,0} = U_{C_r}(0)$ is the initial condition of the capacitor voltage,
- $\omega_m = \frac{1}{\sqrt{(L_r+L_m)C_r}}$ is the resonance angular frequency,
- $Z_m = \sqrt{\frac{L_r+L_m}{C_r}}$ is the characteristic impedance.

The voltages across the passive components are given by

$$u_{L_r} = \frac{L_r}{L_m + L_r}(U_i - U_{C,0})\cos\omega_m t - \sqrt{\frac{L_r}{L_m + L_r}}(Z_0 I_{L,0})\sin\omega_m t, \tag{4.75}$$

$$u_{L_m} = \frac{L_m}{L_m + L_r}(U_i - U_{C,0})\cos\omega_m t - \frac{L_m}{\sqrt{L_r(L_m + L_r)}} Z_0 I_{L,0}\sin\omega_m t, \text{ and} \tag{4.76}$$

$$u_{C_r} = U_i - (U_i - U_{C,0})\cos\omega_m t + Z_m I_{L,0}\sin\omega_m t. \tag{4.77}$$

Note that the relation between ω_m and ω_0 is

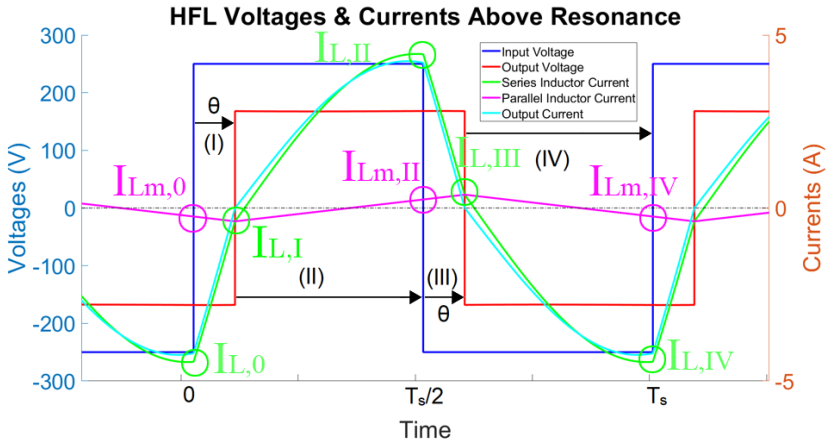


Figure 4.20 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL for the inductance region.

$$\omega_0 = \sqrt{\frac{L_m + L_r}{L_r}}\omega_m, \tag{4.78}$$

which means that as L_m/L_r increases, ω_m becomes significantly smaller than ω_0. Hence, as the converter operates in the load cutoff, the corresponding voltages and currents oscillate significantly slower compared to those in the power-flowing operation.

4.3.2.1 Operation at $f_s > f_0$ (Inductive Region)

Similar to the LC-SR case, this region is defined as inductive because (i) $X_{Lr} > X_{Cr}$ and (ii) the zero-crossing of the currents i_{Lr} and i_o are lagging to the corresponding crossing of the HFL input voltage $U_{HFL,i}$, as illustrated in Fig. 4.20.

Four time intervals are defined, based on the states of the input and the output voltages, as in

$$\begin{cases} \text{I:} & \{u_i(t) = +U_i \mid u_o(t) = -U_o\}, \ 0 \le t \le \frac{\theta}{2\pi}T_s, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\}, \ \frac{\theta}{2\pi}T_s \le t \le \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = -U_i \mid u_o(t) = +U_o\}, \ \frac{T_s}{2} \le t \le \frac{\theta+\pi}{2\pi}T_s, \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\}, \ \frac{\theta+\pi}{2\pi}T_s \le t \le T_s. \end{cases} \tag{4.79}$$

If stead-state operation is assumed $I_{L,IV} = I_{L,0}$, $I_{Lm,IV} = I_{Lm,0}$, and $U_{C,IV} = U_{C,0}$. As the voltage $U_{\mathrm{HFL},o}$ changes sign, the output current $i_o = 0$, hence $I_{Lr,I} = I_{Lm,I}$ and $I_{Lr,III} = I_{Lm,III}$.

Based on the analysis for the conducting simplified model of Fig. 4.19a, the current of the inductor L_r, for each respective time interval, is

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0}\cos\omega_0 t + \frac{U_i+U_o-U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & I_{L,I}\cos\omega_0(t-\frac{\theta}{2\pi}T_s) + \frac{U_i-U_o-U_{C,I}}{Z_0}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & I_{L,II}\cos\omega_0(t-\frac{T_s}{2}) - \frac{U_i+U_o+U_{C,II}}{Z_0}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & I_{L,III}\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) - \frac{U_i-U_o+U_{C,III}}{Z_0}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s), \end{cases} \tag{4.80}$$

while the voltage

$$u_{Lr} = \begin{cases} \text{I:} & (U_i+U_o-U_{C,0})\cos\omega_0 t - Z_0 I_{L,0}\sin\omega_0 t, \\ \text{II:} & (U_i-U_o-U_{C,I})\cos\omega_0(t-\frac{\theta}{2\pi}T_s) - Z_0 I_{L,I}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & -(U_i+U_o+U_{C,II})\cos\omega_0(t-\frac{T_s}{2}) - Z_0 I_{L,II}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & (U_o-U_i-U_{C,III})\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) - Z_0 I_{L,III}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s). \end{cases} \tag{4.81}$$

The current of the magnetizing inductance L_m is

$$i_{Lm} = \begin{cases} \text{I:} & -\frac{U_o}{L_m}t + I_{Lm,0}, \\ \text{II:} & \frac{U_o}{L_m}(t-\frac{\theta}{2\pi}T_s) + I_{Lm,I}, \\ \text{III:} & \frac{U_o}{L_m}(t-\frac{T_s}{2}) + I_{Lm,II}, \\ \text{IV:} & -\frac{U_o}{L_m}(t-\frac{\theta+\pi}{2\pi}T_s) + I_{Lm,III}. \end{cases} \tag{4.82}$$

In the steady-state, the current of C_r and the voltage of L_r must have zero mean value, i.e., $\langle i_{Lr}\rangle = \langle i_{Cr}\rangle = 0$ and $\langle u_{Lr}\rangle = 0$, so the following conditions apply:

$$I_{L,0} = -I_{L,II},\ I_{L,I} = -I_{L,III},\ U_{C,0} = -U_{C,II},\ U_{C,I} = -U_{C,III}. \tag{4.83}$$

The final values of time intervals I and III are given by

$$\begin{cases} I_{L,I} & = i_{Lr}(\frac{\theta}{2\pi}T_s) = I_{L,0}\cos\frac{\omega_0}{\omega_s}\theta + \frac{U_i+U_o-U_{C,0}}{Z_0}\sin\frac{\omega_0}{\omega_s}\theta \\ I_{L,III} & = i_{Lr}(\frac{\theta+\pi}{2\pi}T_s) = I_{L,II}\cos\frac{\omega_0}{\omega_s}\theta - \frac{U_i+U_o-U_{C,II}}{Z_0}\sin\frac{\omega_0}{\omega_s}\theta \end{cases} \tag{4.84}$$

and

$$\begin{cases} I_{Lm,I} & = i_{Lm}(\frac{\theta}{2\pi}T_s) = -\frac{U_o}{L_m}\frac{\theta}{2\pi}T_s + I_{Lm,0} \\ I_{Lm,III} & = i_{Lm}(\frac{\theta+\pi}{2\pi}T_s) = \frac{U_o}{L_m}\frac{\theta}{2\pi}T_s + I_{Lm,II} \end{cases} \tag{4.85}$$

where ω_s is the switching frequency of the converter.

Substituting the symmetries of the half-period from (4.83) to (4.80) and (4.82) yields

$$I_{Lm,0} = -I_{Lm,II},\ I_{Lm,I} = -I_{Lm,III}, \tag{4.86}$$

and

$$I_{Lm,III} = I_{L,III} = -I_{Lm,I} = -I_{L,III} = \frac{\pi}{2}\frac{U_o}{\omega_s L_m}, \tag{4.87}$$

From (4.87), it turns out that the maximum and minimum magnetizing current is proportional to U_o and inversely proportional to the magnetizing inductance L_m and the switching frequency f_s. Substituting (4.87) to (4.85), the initial conditions are derived

$$I_{Lm,0} = -I_{Lm,II} = \frac{U_o}{L_m}T_s(\frac{\theta}{2\pi} - \frac{1}{4}). \tag{4.88}$$

The relationship between the initial conditions $I_{L,0}$ and $I_{L,II}$ is given in (4.83). However, aiming for an elegant closed-form equation is challenging. A good approximation is given by considering that the initial condition is given as the sum of the corresponding initial condition of the LC-SR converter $I_{L,0,LC}$ from (4.22) and the initial condition of the magnetizing current $I_{Lm,0}$ from (4.88), as in

$$\begin{aligned} &I_{L,0} \approx I_{L,0,LC} + I_{Lm,0} \Rightarrow \\ &I_{L,0} \approx -\frac{2\frac{U_i}{Z_0}}{\cot\frac{\omega_0}{\omega_s}\theta + \cot\frac{\omega_0}{\omega_s}(\pi - \theta)} + \frac{U_o}{L_m}T_s(\frac{\theta}{2\pi} - \frac{1}{4}). \end{aligned} \tag{4.89}$$

The magnetizing current crosses zero two times within a period, the first time in interval II and the second in interval IV. Solving (4.82) for $i_{Lm} = 0$ yields

$$\tau_{i_{Lm}=0} = \begin{cases} T_s(\frac{\theta}{2\pi} + \frac{1}{4}), \\ T_s(\frac{\theta}{2\pi} + \frac{3}{4}), \end{cases} \tag{4.90}$$

which means that i_{Lm} crosses zero exactly in the middle of the pulse of the output voltage U_o, something that is intuitively expected since the $\langle i_{Lm}\rangle = 0$ and is dictated by the output voltage. The current of the resonant inductor i_{Lr} crosses zero at

$$\tau_{i_{Lr}=0} = \begin{cases} \frac{\theta}{2\pi}T_s + \frac{1}{\omega_0}\arctan\frac{-Z_0 I_{L,I}}{U_i - U_o - U_{C,I}}, \\ \frac{\theta+\pi}{2\pi}T_s + \frac{1}{\omega_0}\arctan\frac{-Z_0 I_{L,III}}{U_o - U_i - U_{C,III}}. \end{cases} \tag{4.91}$$

The instantaneous input power is

$$p_{in} = u_{in} i_{Lr} = \begin{cases} \text{I: } U_i I_{L,0} \cos \omega_0 t + U_i \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II: } U_i I_{L,I} \cos \omega_0 (t - \frac{\theta}{2\pi} T_s + U_i \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta}{2\pi} T_s, \\ \text{III: } U_i I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) + U_i \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV: } U_i I_{L,I} \cos \omega_0 (t - \frac{\theta+\pi}{2\pi} T_s + U_i \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta+\pi}{)} 2\pi T_s. \end{cases} \tag{4.92}$$

Similarly, the instantaneous output power is

$$p_{out} = u_{out} i_o = u_{out} i_{Lr} - u_{out} i_{Lm}$$

but $u_{out} i_{Lm}$ has a mean value of zero within a period, and its term is omitted for sake of simplicity. The instantaneous output power, for each time interval, is

$$p_{out} = \begin{cases} \text{I: } -U_o I_{L,0} \cos \omega_0 t - U_o \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II: } U_o I_{L,I} \cos \omega_0 (t - \frac{\theta}{2\pi} T_s + U_o \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta}{2\pi} T_s, \\ \text{III: } -U_o I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) - U_o \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV: } U_o I_{L,I} \cos \omega_0 (t - \frac{\theta+\pi}{2\pi} T_s + U_o \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta+\pi}{2\pi} T_s. \end{cases} \tag{4.93}$$

The active power flowing through the HFL is given by the mean values of p_{in} and p_{out} within a switching period, as in

$$P_i = \frac{U_i}{\pi} \frac{\omega_s}{\omega_0} \left(I_{L,0} \sin \frac{\omega_0}{\omega_s} \theta + I_{L,I} \sin \frac{\omega_0}{\omega_s} (\pi - \theta) + \frac{U_i + U_o - U_{C,0}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} \theta \right) + \frac{U_i - U_o - U_{C,I}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} (\pi - \theta) \right) \right), \tag{4.94}$$

and

$$P_o = \frac{U_o}{\pi} \frac{\omega_s}{\omega_0} \left(-I_{L,0} \sin \frac{\omega_0}{\omega_s} \theta + I_{L,I} \sin \frac{\omega_0}{\omega_s} (\pi - \theta) - \frac{U_i + U_o - U_{C,0}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} \theta \right) + \frac{U_i - U_o - U_{C,I}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} (\pi - \theta) \right) \right). \tag{4.95}$$

Since the link is considered ideal, without any resistive elements, the input power P_i is equal to the output P_o and equal to U_o^2 / R_L.

In this region, the converter achieves ZVS during turn-on commutations, but turn-off commutations are forced through hard switching. For example, Q_1 and Q_4 are forced to turn-off when the current passing through is $I_{L,II}$. During the dead time this current flows through

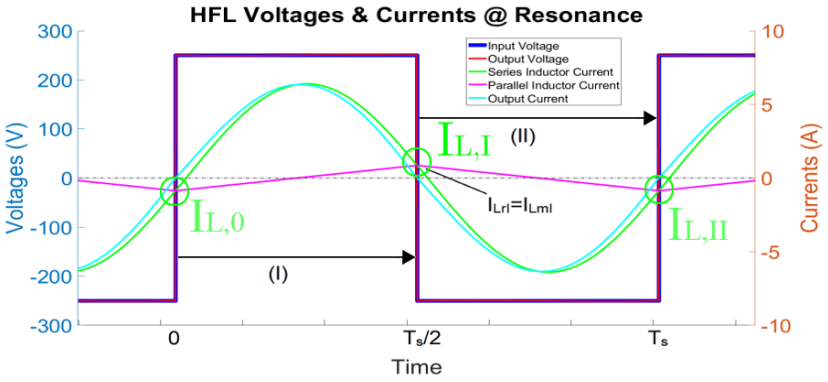


Figure 4.21 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL at the resonance point.

the antiparallel diodes of Q_2 and Q_3, which then turn-on with zero voltage-drop across. Note that as f_s approaches f_0, $I_{L,II}$ becomes smaller and the hard turn-off commutations produce less losses.

4.3.2.2 Operation at $f_s = f_0$ (Resonant Region)

When the switching frequency is equal to the resonant frequency ω_0, (i) $X_L = X_C$ and (ii) the zero-crossing of the output current i_o is in-phase to the corresponding crossing ot the input and output voltage $U_{\mathrm{HFL},i}$ and $U_{\mathrm{HFL},o}$, as illustrated in Fig. 4.21. Note that the resonant current i_{Lr} crosses the zero point after the i_o, presenting a phase delay.

$$\begin{cases} \text{I:} \ \{u_i(t) = +U_i | u_o(t) = +U_o\}, \ 0 \le t \le \frac{T_s}{2}, \\ \text{II:} \ \{u_i(t) = -U_i | u_o(t) = -U_o\}, \ \frac{T_s}{2} \le t \le T_s. \end{cases} \tag{4.96}$$

Since $\theta = 0$, the time intervals I and III of subsection 4.3.2.1 are omitted. Due to the voltage and current continuity conditions, combined with (4.83), and (4.86)

$$\begin{aligned} I_{L,0} &= -I_{L,I} = I_{L,II} = I_{Lm,0} = -I_{Lm,I} = I_{Lm,II}, \\ U_{C,0} &= U_{C,II} = -U_{C,I}. \end{aligned} \tag{4.97}$$

Eqs. (4.80) and (4.81) can be simplified, using Eq. (4.97)

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0} \cos \omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t \\ \text{II:} & -I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) - \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}) \end{cases} \Rightarrow$$

$$i_{Lr} = I_{L,0} \cos \omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \tag{4.98}$$

$$u_{Lr} = \begin{cases} \text{I:} & -Z_0 I_{L,0} \sin \omega_0 t + (U_i - U_o - U_{C,0}) \cos \omega_0 t \\ \text{II:} & Z_0 I_{L,0} \sin \omega_0 (t - \frac{T_s}{2}) - (U_i - U_o - U_{C,0}) \cos \omega_0 (t - \frac{T_s}{2}) \end{cases} \Rightarrow$$

$$u_{Lr} = -Z_0 I_{L,0} \sin \omega_0 t + (U_i - U_o - U_{C,0}) \cos \omega_0 t. \tag{4.99}$$

The main difference compared to the LC-SR converter is that the resonant current i_{Lr} is not in-phase with HFL voltages, due to the magnetizing current. The voltage of the resonant capacitor is

$$u_{Cr} = U_i - U_o - (U_i - U_o - U_{C,0}) \cos \omega_0 t + Z_0 I_{L,0} \sin \omega_0 t. \tag{4.100}$$

Regarding the instantaneous power, given in (4.92) and (4.93) can be simplified as

$$p_{in} = u_{in} i_{Lr} = \begin{cases} \text{I:} & U_i I_{L,0} \cos \omega_0 t + U_i \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} & U_i I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) + U_i \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \end{cases} \tag{4.101}$$

$$p_{out} = \begin{cases} \text{I:} & U_o I_{L,0} \cos \omega_0 t + U_o \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} & U_o I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) + U_o \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}). \end{cases} \tag{4.102}$$

The active power is given by

$$\begin{aligned} P_i &= U_i \frac{2}{\pi} \frac{U_i - U_o - U_{C,0}}{Z_0}, \\ P_o &= U_o \frac{2}{\pi} \frac{U_i - U_o - U_{C,0}}{Z_0}, \end{aligned} \tag{4.103}$$

and since the HFL is considered ideal, $P_i = P_o$ yields $U_i = U_o$, for any load.

The zero-crossings of the currents i_{Lr} and i_{Lm} take place at

$$\tau_{i_{Lr}=0} = \frac{1}{\omega_0} \arctan \frac{Z_0 I_{L,0}}{U_{C,0}}, \tag{4.104}$$

and

$$\tau_{i_{Lm}=0} = \begin{cases} -I_{Lm,0} \frac{L_m}{U_i}, \\ -I_{Lm,I} \frac{L_m}{U_i} + \frac{T_s}{2}, \end{cases} \tag{4.105}$$

which, from (4.90) and $\theta = 0$, correspond to the middle of the half-period voltage square waveform. Hence

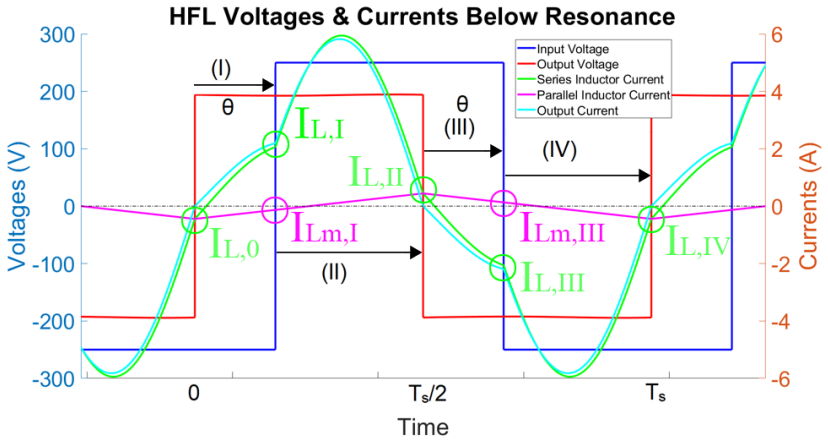


Figure 4.22 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL for the capacitive CCM operation.

$$I_{Lm,I} = -I_{Lm,0} = -I_{L,0} = \frac{\pi}{2}\frac{U_o}{\omega_s L_m}. \tag{4.106}$$

Substituting $P_o = U_o^2/R_L$ to (4.103), yields

$$U_{C,0} = -U_o\frac{\pi}{2}\frac{Z_0}{R_L}. \tag{4.107}$$

meaning that the initial voltage of C_r is proportional to the input voltage U_i and inversely proportional to the output resistor R_L.

Contrary to the LC-SR case, the i_{Lr} does not present a pure resistive, but an inductive-resistive behavior, lagging with respect to the input voltage by a time interval defined in 4.104. Hence, the behavior of the primary bridge is similar to that of subsection 4.3.2.1. The converter experiences ZVS during turn-on and hard switching during turn-off, but the forced commuted current i_{Lr} is as small as possible.

4.3.2.3 Operation at $\frac{f_0}{2} < f_s < f_0$ (Capacitive CCM or Type A Region)

In contrast to the LC-SR converter, for $\frac{f_0}{2} < f_s < f_0$ and from the perspective of the primary bridge, the HFL can behave as an inductive-resistive or capacitive-resistive load, depending on the switching frequency f_s and the load R_L as presented in [191, 192, 193]. In this subsection the capacitive CCM or type A region (heavy-load) is discussed.

This region is defined as capacitive since (i) $X_C > X_L$ and (ii) the first harmonic of the i_{Lr} is leading the input voltage of the HFL. The angle θ is defined as the negative of (4.62) for the sake of simplicity.

An indicative case of this operation is presented in Fig. 4.22, along with the intervals for each switching state of the converter. The voltages are

$$\begin{cases} \text{I:} & \{u_i(t) = -U_i \mid u_o(t) = +U_o\},\ 0 \le t \le \frac{\theta}{2\pi}T_s, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\},\ \frac{\theta}{2\pi}T_s \le t \le \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = +U_i \mid u_o(t) = -U_o\},\ \frac{T_s}{2} \le t \le \frac{\theta+\pi}{2\pi}T_s, \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\},\ \frac{\theta+\pi}{2\pi}T_s \le t \le T_s. \end{cases} \tag{4.108}$$

For every commutation of the rectifying current-driven bridge i_o is zero, hence, $I_{L,0} = I_{Lm,0},\ I_{L,II} = I_{Lm,II}$. Based on the analysis for the conducting simplified model, the current and the voltage of L_r are

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0}\cos\omega_0 t - \frac{U_i+U_o+U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & I_{L,I}\cos\omega_0(t-\frac{\theta}{2\pi}T_s) + \frac{U_i-U_o-U_{C,I}}{Z_0}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & I_{L,II}\cos\omega_0(t-\frac{T_s}{2}) + \frac{U_i+U_o-U_{C,II}}{Z_0}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & I_{L,III}\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) - \frac{U_i-U_o+U_{C,III}}{Z_0}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s), \end{cases} \tag{4.109}$$

and

$$u_{Lr} = \begin{cases} \text{I:} & -(U_i+U_o+U_{C,0})\cos\omega_0 t - Z_0 I_{L,0}\sin\omega_0 t, \\ \text{II:} & (U_i-U_o-U_{C,I})\cos\omega_0(t-\frac{\theta}{2\pi}T_s) - Z_0 I_{L,I}\sin\omega_0(t-\frac{\theta}{2\pi}T_s), \\ \text{III:} & (U_i+U_o-U_{C,II})\cos\omega_0(t-\frac{T_s}{2}) - Z_0 I_{L,II}\sin\omega_0(t-\frac{T_s}{2}), \\ \text{IV:} & -(U_i-U_o+U_{C,III})\cos\omega_0(t-\frac{\theta+\pi}{2\pi}T_s) - Z_0 I_{L,III}\sin\omega_0(t-\frac{\theta+\pi}{2\pi}T_s). \end{cases} \tag{4.110}$$

The magnetizing current arises from the integration of the output voltage, as in

$$i_{Lm} = \begin{cases} \text{I:} & \frac{U_o}{L_m}t + I_{Lm,0}, \\ \text{II:} & \frac{U_o}{L_m}(t-\frac{\theta}{2\pi}T_s) + I_{Lm,I}, \\ \text{III:} & -\frac{U_o}{L_m}(t-\frac{T_s}{2}) + I_{Lm,II}, \\ \text{IV:} & -\frac{U_o}{L_m}(t-\frac{\theta+\pi}{2\pi}T_s) + I_{Lm,III}. \end{cases} \tag{4.111}$$

In the steady-state, the current of C_r and the voltage of L_r must have zero mean value, i.e., $\langle i_{Lr}\rangle = \langle i_{Cr}\rangle = 0$ and $\langle u_{Lr}\rangle = 0$, so the following conditions apply:

$$\begin{aligned} I_{L,II} &= I_{L,I}\cos\frac{\omega_0}{\omega_s}(\pi-\theta) + \frac{U_i-U_o-U_{C,I}}{Z_0}\sin\frac{\omega_0}{\omega_s}(\pi-\theta) \\ I_{L,IV} = I_{L,0} &= I_{L,II}\cos\frac{\omega_0}{\omega_s}(\pi-\theta) - \frac{U_i-U_o+U_{C,III}}{Z_0}\sin\frac{\omega_0}{\omega_s}(\pi-\theta) \end{aligned} \tag{4.112}$$

$$\begin{aligned} I_{Lm,II} &= \frac{U_o}{L_m}\frac{\pi-\theta}{2\pi}T_s + I_{Lm,I} \\ I_{Lm,IV} = I_{Lm,0} &= -\frac{U_o}{L_m}\frac{\pi-\theta}{2\pi}T_s + I_{Lm,III} \end{aligned} \tag{4.113}$$

Similar to (4.86), from (4.113) and due to continuity of the current

$$I_{Lm,0} = -I_{Lm,II},\ I_{Lm,I} = -I_{Lm,III}, \tag{4.114}$$

The final value of time interval I for the current i_{Lm} is

$$I_{Lm,I} = \frac{U_o}{L_m}\frac{\theta}{2\pi}T_s + I_{Lm,0}. \tag{4.115}$$

Replacing (4.115) to (4.113), yields

$$I_{Lm,II} = I_{L,II} = -I_{Lm,0} = -I_{L,0} = \frac{\pi}{2}\frac{U_o}{\omega_0 L_m}. \tag{4.116}$$

which is the same as (4.87) for the inductive region.

Replacing (4.116) to (4.113), yields

$$I_{Lm,I} = -I_{L,III} = \frac{U_o}{L_m}T_s(\frac{\theta}{2\pi} - \frac{1}{4}). \tag{4.117}$$

The magnetizing current i_{Lm} crosses zero two times, first in interval II and then in interval IV. The exact time can be found by equating (4.111) to zero and substituting (4.117)

$$\tau_{i_{Lm}=0} = \begin{cases} \frac{T_s}{4}, \\ \frac{3}{4}T_s, \end{cases} \tag{4.118}$$

which means that i_{Lm} crosses zero exactly in the middle of the output voltage U_o, something that is intuitively expected since the $\langle i_{Lm}\rangle = 0$ and is dictated by the output voltage. The current of the resonant inductor i_{Lr} crosses zero at

$$\tau_{i_{Lr}=0} = \begin{cases} \frac{1}{\omega_0}\arctan\frac{Z_0 I_{L,0}}{U_i+U_o+U_{C,I}}, \\ \frac{T_s}{2} + \frac{1}{\omega_0}\arctan\frac{-Z_0 I_{L,0}}{U_i+U_o-U_{C,II}}. \end{cases} \tag{4.119}$$

The instantaneous input power is

$$p_{in} = u_{in} i_{Lr} = \begin{cases} \text{I:} \quad -U_i I_{L,0} \cos \omega_0 t + U_i \frac{U_i + U_o + U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} \quad U_i I_{L,I} \cos \omega_0 (t - \frac{\theta}{2\pi} T_s + U_i \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta}{2\pi} T_s, \\ \text{III:} \quad -U_i I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) + U_i \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV:} \; U_i I_{L,I} \cos \omega_0 (t - \frac{\theta + \pi}{2\pi} T_s + U_i \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta + \pi}{)} 2\pi T_s. \end{cases} \tag{4.120}$$

Similarly, the instantaneous output power is

$$p_{out} = u_{out} i_o = u_{out} i_{Lr} - u_{out} i_{Lm}$$

but $u_{out} i_{Lm}$ has a mean value of zero within a period, and its term is omitted for sake of simplicity. The instantaneous output power, for each time interval, is

$$p_{out} = \begin{cases} \text{I:} \quad U_o I_{L,0} \cos \omega_0 t - U_o \frac{U_i + U_o + U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} \quad U_o I_{L,I} \cos \omega_0 (t - \frac{\theta}{2\pi} T_s + U_o \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta}{2\pi} T_s, \\ \text{III:} \; U_o I_{L,0} \cos \omega_0 (t - \frac{T_s}{2}) - U_o \frac{U_i + U_o - U_{C,0}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV:} \; U_o I_{L,I} \cos \omega_0 (t - \frac{\theta + \pi}{2\pi} T_s + U_o \frac{U_i - U_o - U_{C,I}}{Z_0} \sin \omega_0 (t - \frac{\theta + \pi}{2\pi} T_s. \end{cases} \tag{4.121}$$

The active power flowing through the HFL is given by the mean values of p_{in} and p_{out} within a switching period, as in

$$P_i = \frac{U_i}{\pi} \frac{\omega_s}{\omega_0} \left(-I_{L,0} \sin \frac{\omega_0}{\omega_s} \theta + I_{L,I} \sin \frac{\omega_0}{\omega_s} (\pi - \theta) + \frac{U_i + U_o + U_{C,0}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} \theta \right) + \frac{U_i - U_o - U_{C,I}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} (\pi - \theta) \right) \right), \tag{4.122}$$

and

$$P_o = \frac{U_o}{\pi} \frac{\omega_s}{\omega_0} \left(I_{L,0} \sin \frac{\omega_0}{\omega_s} \theta + I_{L,I} \sin \frac{\omega_0}{\omega_s} (\pi - \theta) - \frac{U_i + U_o + U_{C,0}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} \theta \right) + \frac{U_i - U_o - U_{C,I}}{Z_0} \left(1 - \cos \frac{\omega_0}{\omega_s} (\pi - \theta) \right) \right). \tag{4.123}$$

Since the link is considered ideal, without any resistive elements, the input power P_i is equal to the output P_o and equal to U_o^2 / R_L.

Similar to the corresponding operation region of the LC-SR converter, all switches experience hard switching at turn-on and ZVS at turn-off. For example, when Q_1 and Q_4 are conducting, the commutation occurs under a negative current $I_{L,III}$, which means that the

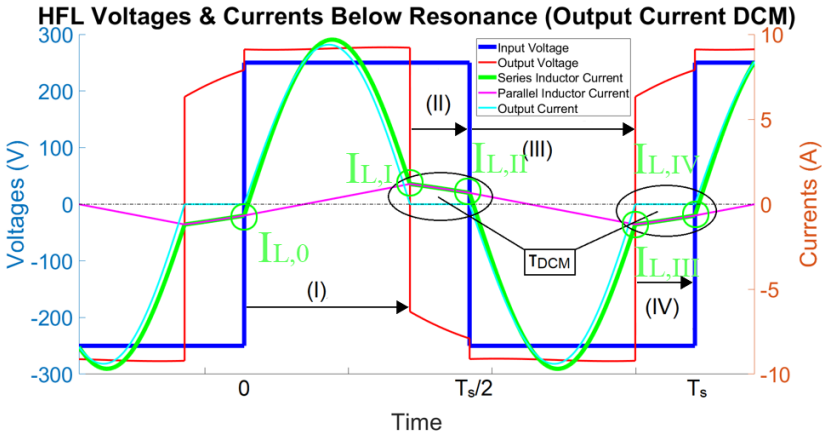


Figure 4.23 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL for the capacitive DCM operation.

voltage across the switch is clamped by the antiparallel (or body) diode. Then Q_2 and Q_3 turn-on under an initial voltage equal to that of the DC bus, experiencing hard-switching.

4.3.2.4 Operation at $\frac{f_0}{2} < f_s < f_0$ (Discontinuous Power Flow - DCM or Type B Region)

In this case, DCM is regarded with respect to the output current i_o. The current i_{Lr} becomes instantaneously equal to zero, during zero-crossing. In contrast, i_o goes to zero for an arbitrary time interval before every switching state of the primary bridge. When power flows from the primary to the secondary bridge ($i_o \neq 0$) the equivalent circuit is presented in Fig. 4.19a, while for the load cut-off operation ($i_o = 0$) the equivalent circuit is depicted in Fig. 4.19b.

The switching frequency remains under the resonant, meaning that $X_C > X_L$ and the first harmonic of i_{Lr} is still leading the input voltage of the HFL, as illustrated in Fig. 4.23. However, it should be noted that when the load cuts-off and the magnetizing inductor becomes part of the resonant circuit, the resonant frequency f_m is significantly smaller compared to f_0. As the switching frequency remains the same, from the perspective of the primary bridge, the rest of the circuit behaves like an inductive-resistive load.

The four time intervals are defined as

$$\begin{cases} \text{I:} & \{u_i(t) = +U_i \mid u_o(t) = +U_o\}, \ 0 \leq t \leq \frac{T_s}{2} - \tau_{\mathrm{DCM}}, \\ \text{II:} & \{u_i(t) = +U_i \mid u_o(t) = u_{Lm}\}, \ \frac{T_s}{2} - \tau_{\mathrm{DCM}} \leq t \leq \frac{T_s}{2}, \\ \text{III:} & \{u_i(t) = -U_i \mid u_o(t) = -U_o\}, \ \frac{T_s}{2} \leq t \leq T_s - \tau_{\mathrm{DCM}}, \\ \text{IV:} & \{u_i(t) = -U_i \mid u_o(t) = u_{Lm}\}, \ T_s - \tau_{\mathrm{DCM}} \leq t \leq T_s, \end{cases} \tag{4.124}$$

where u_{Lm} is the voltage of the magnetizing inductor, for the time interval that the load is cutoff ($i_o = 0$). In accordance with the previous analyses, due to current continuity and symmetry, in the steady-state the initial values are given as

$$I_{Lm,0} = I_{L,0} = I_{Lm,IV} = I_{L,IV},\ I_{Lm,I} = I_{L,I},\ I_{Lm,II} = I_{L,II},\ I_{Lm,III} = I_{L,III}. \tag{4.125}$$

The current and voltage of L_r are

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0}\cos\omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & I_{L,I}\cos\omega_m(t - \frac{T_s}{2} + \tau_{\text{DCM}}) + \frac{U_i - U_{C,I}}{Z_m}\sin\omega_m(t - \frac{T_s}{2} + \tau_{\text{DCM}}), \\ \text{III:} & I_{L,II}\cos\omega_0(t - \frac{T_s}{2}) - \frac{U_i - U_o + U_{C,II}}{Z_0}\sin\omega_0(t - \frac{T_s}{2}), \\ \text{IV:} & I_{L,III}\cos\omega_m(t - T_s + \tau_{\text{DCM}}) - \frac{U_i + U_{C,III}}{Z_m}\sin\omega_m(t - T_s + \tau_{\text{DCM}}), \end{cases} \tag{4.126}$$

and

$$u_{Lr} = \begin{cases} \text{I:} & (U_i - U_o - U_{C,0})\cos\omega_0 t - Z_0 I_{L,0}\sin\omega_0 t, \\ \text{II:} & \frac{L_r}{L_m + L_r}(U_i - U_{C,I})\cos\omega_m(t - \frac{T_s}{2} + \tau_{\text{DCM}}) \\ & -\sqrt{\frac{L_r}{L_m + L_r}}Z_0 I_{L,I}\sin\omega_m(t - \frac{T_s}{2} + \tau_{\text{DCM}}), \\ \text{III:} & -(U_i - U_o + U_{C,II})\cos\omega_0(t - \frac{T_s}{2}) - Z_0 I_{L,II}\sin\omega_0(t - \frac{T_s}{2}), \\ \text{IV:} & -\frac{L_r}{L_m + L_r}(U_i + U_{C,III})\cos\omega_m(t - T_s + \tau_{\text{DCM}}) \\ & -\sqrt{\frac{L_r}{L_m + L_r}}Z_0 I_{L,III}\sin\omega_m(t - T_s + \tau_{\text{DCM}}), \end{cases} \tag{4.127}$$

while the voltage and current of L_m are

$$u_{Lm}=\begin{cases}\text{I:}\quad U_o,\\ \text{II:}\quad \dfrac{L_m}{L_m+L_r}(U_i-U_{C,I})\cos\omega_m(t-\dfrac{T_s}{2}+\tau_{\text{DCM}})\\ \quad -\dfrac{L_m}{\sqrt{L_r(L_m+L_r)}}Z_0 I_{Lm,I}\sin\omega_m(t-\dfrac{T_s}{2}+\tau_{\text{DCM}}),\\ \text{III:}\quad -U_o,\\ \text{IV:}\quad -\dfrac{L_m}{L_m+L_r}(U_i+U_{C,III})\cos\omega_m(t-T_s+\tau_{\text{DCM}})\\ \quad -\dfrac{L_m}{\sqrt{L_r(L_m+L_r)}}Z_0 I_{Lm,III}\sin\omega_m(t-T_s+\tau_{\text{DCM}}),\end{cases}\tag{4.128}$$

and

$$i_{Lm}=\begin{cases}\text{I:}\quad \frac{U_o}{L_m}t+I_{Lm,0},\\ \text{II:}\quad I_{Lm,I}\cos\omega_m(t-\frac{T_s}{2}+\tau_{\text{DCM}})+\frac{U_i-U_{C,I}}{Z_m}\sin\omega_m(t-\frac{T_s}{2}+\tau_{\text{DCM}})\\ \text{III:}\quad -\frac{U_o}{L_m}(t-\frac{T_s}{2})+I_{Lm,II},\\ \text{IV:}\quad I_{Lm,III}\cos\omega_m(t-T_s+\tau_{\text{DCM}})+\frac{U_i+U_{C,III}}{Z_m}\sin\omega_m(t-T_s+\tau_{\text{DCM}}).\end{cases}\tag{4.129}$$

In the steady-state operation, the current of the capacitor and the voltage drop across each inductor must have a zero mean value, i.e., $\langle i_{Lr}\rangle=\langle i_{Cr}\rangle=0$, $\langle u_{Lr}\rangle=0$, and $\langle u_{Lm}\rangle=0$. For these conditions to be simultaneously valid

$$I_{Lm,0}=I_{L,0}=-I_{Lm,II}=-I_{L,II},\ I_{Lm,I}=I_{L,I}=-I_{Lm,III}=-I_{L,III},\tag{4.130}$$

and

$$U_{C,0}=-U_{C,II},\ U_{C,I}=-U_{C,III},\tag{4.131}$$

should stand.

The final values of time intervals I and III are

$$\begin{cases}I_{Lm,I} &= \frac{U_o}{L_m}(\frac{T_s}{2}-\tau_{\text{DCM}})+I_{Lm,0}\\ I_{Lm,III} &= \frac{U_o}{L_m}(\frac{T_s}{2}-\tau_{\text{DCM}})+I_{Lm,II}\end{cases}\tag{4.132}$$

and for intervals II and IV

$$\begin{cases}I_{Lm,II} &= I_{L,I}\cos\omega_m\tau_{\text{DCM}}+\frac{U_i-U_{C,I}}{Z_m}\sin\omega_m\tau_{\text{DCM}}\\ I_{Lm,0} &= I_{L,III}\cos\omega_m\tau_{\text{DCM}}-\frac{U_i+U_{C,III}}{Z_m}\sin\omega_m\tau_{\text{DCM}}.\end{cases}\tag{4.133}$$

Utilizing the current equations and the conditions of (4.130), the zero-crossing of i_{Lr} and i_{Lm} is obtained, as in

$$\tau_{i_{Lr}=0} = \begin{cases} \frac{1}{\omega_0} \arctan \frac{-Z_0 I_{L,0}}{U_i - U_o - U_{C,0}}, \\ \frac{T_s}{2} + \frac{1}{\omega_0} \arctan \frac{Z_0 I_{L,II}}{U_i - U_o + U_{C,II}}, \end{cases} \tag{4.134}$$

and

$$\tau_{i_{Lm}=0} = \begin{cases} -\frac{L_m}{U_o} I_{Lm,0}, \\ \frac{T_s}{2} + \frac{L_m}{U_o} I_{Lm,II}. \end{cases} \tag{4.135}$$

As in the previous cases, the instantaneous input and output power is given by $p_{in} = u_{in} i_{Lr}$ and $p_{out} = u_{out}(i_{Lr} - i_{Lm})$ and the active input and output power by

$$\begin{aligned} P_i = \frac{U_i}{\pi} \omega_s \Bigg(& \frac{I_{L,0}}{\omega_0} \sin \omega_0 (\frac{T_s}{2} - \tau_{\mathrm{DCM}}) + \frac{I_{L,I}}{\omega_m} \sin \omega_m \tau_{\mathrm{DCM}} \\ & + \frac{U_i - U_o - U_{C,0}}{\omega_0 Z_0} \left(1 - \cos \omega_0 \left(\frac{T_s}{2} - \tau_{\mathrm{DCM}} \right) \right) + \frac{U_i - U_{C,I}}{\omega_m Z_m} \left(1 - \cos \omega_m \tau_{\mathrm{DCM}} \right) \Bigg), \end{aligned} \tag{4.136}$$

and

$$\begin{aligned} P_o = \frac{U_i}{\pi} \omega_s \Bigg(& I_{L,0} \left(\frac{1}{\omega_0} \sin \omega_0 \left(\frac{T_s}{2} - \tau_{\mathrm{DCM}} \right) - \frac{T_s}{2} + \tau_{\mathrm{DCM}} \right) \\ & + \frac{U_i - U_o - U_{C,0}}{\omega_0 Z_0} \left(1 - \cos \omega_0 \left(\frac{T_s}{2} - \tau_{\mathrm{DCM}} \right) \right) - \frac{U_o}{2 L_m} \left(\frac{T_s^2}{4} - \tau_{\mathrm{DCM}} (\tau_{\mathrm{DCM}} - T_s) \right) \Bigg) \end{aligned} \tag{4.137}$$

As in any other case, the HFL is considered ideal, therefore $P_i = P_o = \frac{U_o^2}{R_L}$.

Approximation of Inductor Current - Heavy Load To simplify the complex piecewise functions that describe the current during load cut-off ($i_o = 0$), it is possible to approximate i_{Lr} and i_{Lm} using a linear function ($y = ax + b$) during this time interval τ_{DCM}. This approximation is valid for heavy-load conditions, meaning that the converter is operating near the boundary of CCM-DCM regions. The case of light-load operation is considered in the next paragraph.

The currents of the resonant and magnetizing inductors are

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0} \cos \omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0} \sin \omega_0 t, \\ \text{II:} & \frac{U_o}{L_m} \left(t - \frac{T_s}{2} + \tau_{\mathrm{DCM}} \right) + I_{L,I}, \\ \text{III:} & I_{L,II} \cos \omega_0 (t - \frac{T_s}{2}) - \frac{U_i - U_o + U_{C,II}}{Z_0} \sin \omega_0 (t - \frac{T_s}{2}), \\ \text{IV:} & -\frac{U_o}{L_m} \left(t - T_s + \tau_{\mathrm{DCM}} \right) + I_{L,III}, \end{cases} \tag{4.138}$$

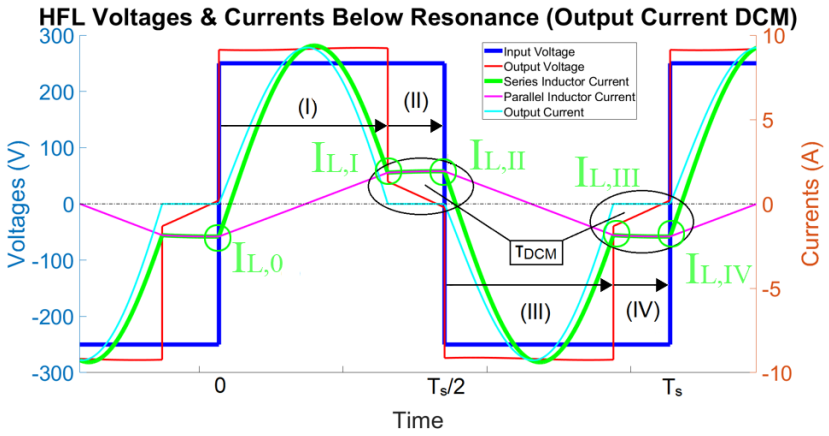


Figure 4.24 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL for the DCM B-type operation.

and

$$i_{Lm} = \begin{cases} \mathrm{I}: & \frac{U_o}{L_m} t + I_{Lm,0}, \\ \mathrm{II}: & -\frac{U_o}{L_m}\left(t - \frac{T_s}{2} + \tau_{\mathrm{DCM}}\right) + I_{Lm,I} \\ \mathrm{III}: & -\frac{U_o}{L_m}(t - \frac{T_s}{2}) + I_{Lm,II}, \\ \mathrm{IV}: & \frac{U_o}{L_m}\left(t - T_s + \tau_{\mathrm{DCM}}\right) + I_{Lm,III}. \end{cases} \tag{4.139}$$

Following the same procedure as before, the final conditions of time intervals II and IV are obtained from (4.139) and in combination with (4.130), yields

$$I_{Lm,0} = I_{L,0} = -I_{Lm,II} = -I_{L,II} = -\frac{U_o}{L_m}\left(\frac{T_s}{4} - \tau_{\mathrm{DCM}}\right). \tag{4.140}$$

Replacing (4.140) to (4.132), yield the approximated expressions for $I_{Lm,I}$ and $I_{Lm,III}$, which are the same for $I_{L,I}$ and $I_{L,III}$, and are equal to (4.87).

The points that i_{Lr} crosses zero remain the same and are given in (4.134), and the corresponding points of i_{Lm} are changed to

$$\tau_{i_{Lm}=0} = \begin{cases} \frac{T_s}{4} - \tau_{\mathrm{DCM}}, \\ \frac{3T_s}{4} - \tau_{\mathrm{DCM}}. \end{cases} \tag{4.141}$$

Finally, the active power flowing through the HFL is

$$\begin{aligned} P_i = P_o = \frac{U_i}{\pi}\omega_s \Bigg(& -\frac{U_i U_o}{\omega_0 L_m}\left(\frac{T_s}{4} - \tau_{\mathrm{DCM}}\right)\sin\omega_0\left(\frac{T_s}{2} - \tau_{\mathrm{DCM}}\right) \\ & + \frac{U_i - U_o - U_{C,0}}{\omega_0 Z_0}\left(1 - \cos\omega_0\left(\frac{T_s}{2} - \tau_{\mathrm{DCM}}\right)\right) + \frac{U_o \tau_{\mathrm{DCM}}}{2L_m}\left(\frac{T_s}{2} + \tau_{\mathrm{DCM}}\right)\Bigg). \end{aligned} \tag{4.142}$$

Approximation of Inductor Current - Light Load When the converter operates under light-load conditions and is deep in the DCM region, the current of the HFL during load cut-off ($i_o = 0$) is approximated as a constant. This is illustrated, for a specific operating point, in Fig. 4.24 for time intervals II and IV.

The resonant current can be approximated as

$$i_{Lr} = \begin{cases} \text{I:} & I_{L,0}\cos\omega_0 t + \frac{U_i - U_o - U_{C,0}}{Z_0}\sin\omega_0 t, \\ \text{II:} & I_{L,I}, \\ \text{III:} & I_{L,II}\cos\omega_0(t - \frac{T_s}{2}) - \frac{U_i - U_o + U_{C,II}}{Z_0}\sin\omega_0(t - \frac{T_s}{2}), \\ \text{IV:} & I_{L,III}, \end{cases} \tag{4.143}$$

and the magnetizing current

$$i_{Lm} = \begin{cases} \text{I:} & \frac{U_o}{L_m}t + I_{Lm,0}, \\ \text{II:} & I_{Lm,I} \\ \text{III:} & -\frac{U_o}{L_m}(t - \frac{T_s}{2}) + I_{Lm,II}, \\ \text{IV:} & I_{Lm,III}. \end{cases} \tag{4.144}$$

In steady-state operation, and due to current continuity, the initial conditions are

$$I_{Lm,0} = I_{L,0} = I_{L,III} = I_{Lm,III} = -I_{Lm,I} = -I_{L,I} = -I_{Lm,II} = -I_{L,II}. \tag{4.145}$$

Equation (4.46) can be used in this case to approximate the τ_{DCM}. The final conditions of the current for time intervals I and III, are

$$I_{Lm,I} = -I_{Lm,0} = \frac{\pi U_o}{2\omega_0 L_m}. \tag{4.146}$$

The zero-crossing of the resonant current is given in (4.134), and the corresponding points of the magnetizing current are

$$\tau_{i_{Lm}=0} = \begin{cases} \frac{\pi}{2\omega_0}, \\ \frac{1}{2}\left(T_s + \frac{\pi}{\omega_0}\right). \end{cases} \tag{4.147}$$

The active input and output power is approximated by

$$P_i = \frac{U_i}{\pi}\frac{\omega_s}{\omega_0}\left(2\frac{U_i - U_o - U_{C,0}}{Z_0} + \frac{\pi^2 U_o}{2L_m}\left(\frac{1}{\omega_s} - \frac{1}{\omega_0}\right)\right), \tag{4.148}$$

and

$$P_o = \frac{2}{\pi}\frac{\omega_s}{\omega_0}U_o\frac{U_i - U_o - U_{C,0}}{Z_0} \tag{4.149}$$

respectively.
For an ideal HFL, without any ohmic losses, $P_i = P_o = \frac{U_o^2}{R_L}$, and solving for $U_{C,0}$ yields

$$U_{C,0} = U_i - U_o\left(1 + \frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{Z_0}{R_L}\right). \tag{4.150}$$

With the initial values of the capacitor and the inductors known, Eqs. (4.143), (4.144), and (4.147) - (4.149), can be rewritten as

$$i_{Lr} = \begin{cases} \text{I:} & -\frac{\pi U_o}{2\omega_0 L_m}\cos\omega_0 t + \frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{U_o}{R_L}\sin\omega_0 t, \\ \text{II:} & \frac{\pi U_o}{2\omega_0 L_m}, \\ \text{III:} & \frac{\pi U_o}{2\omega_0 L_m}\cos\omega_0(t - \frac{T_s}{2}) - \frac{\pi}{2}\frac{\omega_0}{\omega_s}\frac{U_o}{R_L}\sin\omega_0(t - \frac{T_s}{2}), \\ \text{IV:} & -\frac{\pi U_o}{2\omega_0 L_m}, \end{cases} \tag{4.151}$$

$$i_{Lm} = \begin{cases} \text{I:} & \frac{U_o}{L_m}(t - \frac{\pi}{2\omega_0}), \\ \text{II:} & \frac{\pi U_o}{2\omega_0 L_m} \\ \text{III:} & -\frac{U_o}{L_m}(t - \frac{T_s}{2} - \frac{\pi}{2\omega_0}), \\ \text{IV:} & -\frac{\pi U_o}{2\omega_0 L_m}, \end{cases} \tag{4.152}$$

$$\tau_{i_{Lm}=0} = \begin{cases} \frac{1}{\omega_0}\arctan\frac{\omega_s R_L}{\omega_0^2 L_m}, \\ \frac{1}{\omega_0}\arctan\frac{\omega_s R_L}{\omega_0^2 L_m} + \frac{T_s}{2}, \end{cases} \tag{4.153}$$

$$P_i = P_o = U_i U_o\left(\frac{\pi}{2L_m}\frac{\omega_0 - \omega_s}{\omega_0^2} + \frac{1}{R_L}\right). \tag{4.154}$$

Finally, the voltage gain of the HFL is given as

$$\frac{U_o}{U_i} = 1 + \frac{\pi}{2}\frac{\omega_0 - \omega_s}{\omega_0^2}\frac{R_L}{L_m}. \tag{4.155}$$

The observations made in subsection 4.3.1 and from Fig. 4.17 and 4.18, are confirmed from 4.155. The voltage gain decreases as switching frequency f_s increases, until $f_s = f_0$ where $U_o = U_i$. It also decreases as the magnetizing inductor L_m and the load increase, in other words, as the ratio L_m/L_r increases and as R_L decreases.

Inverter Switch Commutations In this case, the semiconductor switches of the primary bridge do not experience the same commutation conditions as the LC-SR converter coun-

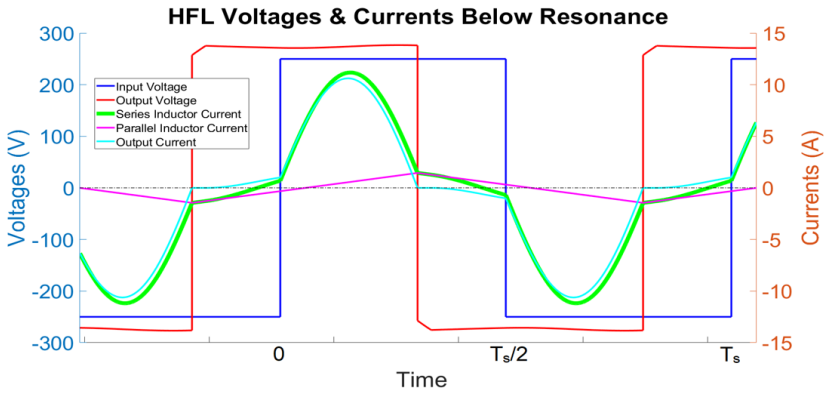


Figure 4.25 Currents (i_{Lr}, i_{Lm}, i_o) and voltages ($U_{\mathrm{HFL},i}$, $U_{\mathrm{HFL},o}$) of the HFL for the DCM C-type operation.

terpart. As explained in the previous paragraph, from the perspective of the inverter, the load behaves like resistive-inductive, and not resistive-capacitive. During the commutation at the end of the time interval II, the current that passes through the switches Q_1 and Q_4 is positive, resulting in hard-switching during turn-off. During the course of the dead-time, this current passes through the anti-parallel diodes of the other two switches Q_2 and Q_3, clamping the voltage to nearly zero, hence these switches experience ZVS during turn-on. During the commutation at the end of the time interval IV, the complementary conditions are true, i.e., Q_2 and Q_3 experience hard turn-off, while Q_1 and Q_4 turn-on under ZVS.

4.3.2.5 Operation at $\frac{f_0}{2} < f_s < f_0$ (Intermediate Power Flow Operation or Type C Region)

The LLC converter can operate in CCM (Type A) or deep DCM (Type B) regions, and the equations that describe its operation were deduced in the previous subsections. However, between the type A and type B operation, there is an intermediate region (Type C) where the waveforms present a unique behavior, which is briefly discussed in this subsection. It should be noted that region types nomenclature (type A, B, and C) is used in the context of this work, for the sake of simplicity.

As illustrated in Fig. 4.25, an intermediate power flow condition exists where the output current i_o goes to zero for an arbitrary time interval, but becomes non-zero before the primary bridge changes state, i.e., before the end of the switching half-period and before its output voltage changes from $\pm U_{DC} \leftrightarrow \mp U_{DC}$.

The output voltage $U_{\mathrm{HFL},o}$ of the HFL is similar to the type A region as it represents a square-wave with 50% duty cycle that is leading the input voltage $U_{\mathrm{HFL},i}$. However, the voltage gain is greater than unity, in contrast with the less than unity gain of region A.

Type C operation is achieved for output resistor R_L smaller (greater load) to that of type B region, but larger (smaller load) to that of type A region, hence, region C is an

intermediate region between B and A. Within the type C region, the output impedance, from the primary bridge perspective, can behave as resistive-inductive or resistive-capacitive load, which corresponds to different kinds of soft switching, described in the previous subsections.

The boundary condition between type A and type C regions is deduced from their definitions. When the LLC converter operates within the type A CCM region, the output current i_o does not become zero and the load is always connected. Consequently, the magnetizing inductor L_m does not participate in the resonant circuit, and the voltage gain of the HFL remains under or equal to one. Therefore, the boundary condition is given for the operation point where the switching frequency is less than the resonant ($f_s < f_0$) and the voltage gain is equal to one ($\frac{U_o}{U_i} = 1$), which can be approximated by (4.61).

The boundary condition between type B and type C regions can be determined by a different property of the converter. During DCM the voltage $U_{\mathrm{HFL},o}$ is equal to the voltage of the magnetizing inductor. When its voltage surpasses the voltage U_o, the rectifying bridge becomes conductive, and i_o becomes non-zero, hence $i_{Lr} \neq i_{Lm}$. From this observation, it is possible to find the boundary condition as the one that the voltage u_{Lm} reaches U_o, at the end of the switching half-period. From (4.128) of type B region, the final value of u_{Lm} of time interval II is

$$\frac{L_m}{\sqrt{L_r(L_r + L_m)}} Z_0 I_{Lm,I} \sin \omega_m \tau_{\mathrm{DCM}} - \frac{L_m}{L_m + L_r}(U_i - U_{C,I}) \cos \omega_m \tau_{\mathrm{DCM}} = U_o, \tag{4.156}$$

which is the boundary condition between type C and B regions.

4.4 Selection of Passive and Active Components

The analyses presented in Sections 4.2 and 4.3 consider the passive components as ideal and linear, and do not examine the electrical restrictions and the non-linearities. Regarding the semiconductor switches, only the output capacitance is considered, indirectly, by commenting on the non-instantaneous transitions between on and off states.

In this section, the selection of the passive resonant components is discussed, along with the utilization of proper semiconductor switches for the primary bridge. The most important criterion that should be satisfied is the operating voltage of each component does not exceed its breakdown voltage. Current restrictions should be considered in combination with the existence of a heatsink and forced-air cooling.

4.4.1 Resonant Capacitor

The HFL resonant capacitor of all resonant converters experiences high-voltage drop across its terminals (even greater from the DC bus voltage for capacitive operation), with a high alternating current passing though. Therefore, the selection of the proper type of the capacitor is of paramount importance. Resonant capacitors should present low equivalent series resistance (ESR) and inductance (ESL) to maintain the efficiency high and not interfere with the resonant frequency. These properties also assist in the longevity of the capacitor and guarantees that the capacitance will not drift over time and over multiple thermal cycles. Additionally, is should not be polarized, hence electrolytic and tantalum capacitors are not considered. In [194] a short description of the properties and the application of mica, film and ceramic capacitors are presented.

Film capacitors employ a thin plastic film as the dielectric material, achieved through a sophisticated film drawing process. Following the manufacturing process, the film may undergo metallization or be left untreated, depending on the desired capacitor properties. Various types of film capacitors exist, such as polyester, metallized, polypropylene, PTFE, and polystyrene. The crucial distinction between these capacitor variants lies in the dielectric material employed, necessitating careful selection based on the intended application. A notable advantage of film capacitors is their non-polarized nature, rendering them suitable for AC signal and power utilization.

One prominent feature of film capacitors is their ability to achieve high precision capacitance values, which also exhibit enhanced stability compared to other capacitor types over time. Furthermore, film capacitors boast extended shelf life and operational longevity, being exceptionally reliable with a remarkably low average failure rate. Additionally, they exhibit characteristics such as low ESR and ESL, and consequently, negligible dissipation factor. These attributes enable them to withstand high voltages, even reaching the kilovolt range, while also offering the ability to deliver robust surge current pulses.

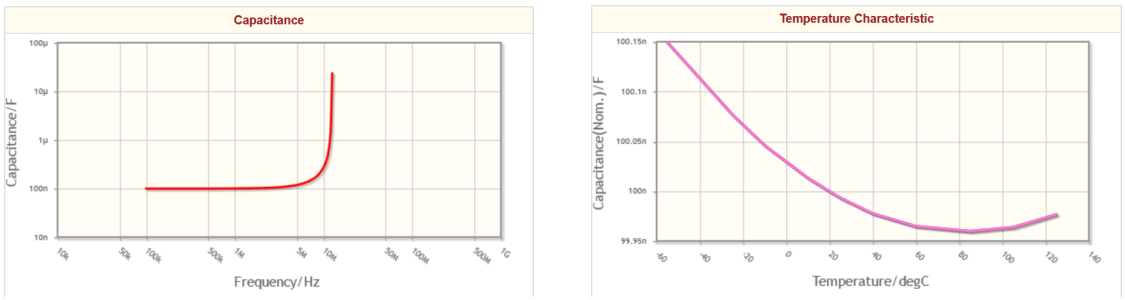
Power film capacitors find widespread application in the realm of power electronics devices, including phase shifters, X-ray flashes, and pulsed lasers. Conversely, their low-power counterparts serve as essential components in decoupling capacitors, and filters. Notably, film capacitors serve diverse roles as safety capacitors, mitigating electromagnetic interference, operating in fluorescent light ballasts, and fulfilling the function of snubber capacitors. They excel in storing energy and facilitating its discharge during high-current pulses, a critical feature employed in powering pulsed lasers and generating lighting discharges. In particular, snubber capacitors play a protective role in counteracting inductive kickback voltage spikes. The choice of film capacitors in snubber design is informed by their favorable attributes, such as low self-inductance, high peak current handling capacity, and low equivalent series resistance (ESR). Polypropylene film capacitors, in particular, find predominant use in these circuits.

Ceramic capacitors utilize ceramic material as the dielectric, and owing to its well-known insulating properties, ceramics were among the earliest materials employed in capacitor production. In modern electronics, two common types of ceramic capacitors are prevalent: the multi-layer ceramic capacitor, also known as the ceramic multi-layer chip capacitor (MLCC), and the ceramic disc capacitor.

Contemporary ceramic capacitors are categorized into two classes. Class 1 capacitors are sought after when high stability and minimal losses are essential. They exhibit exceptional accuracy, with the capacitance value remaining stable across varying applied voltage levels, temperature ranges, and frequencies. For instance, the NP0 series of capacitors offers a capacitance thermal stability of $\pm 0.54\%$ throughout the entire temperature spectrum from -55 to +125 °C. The tolerances for the nominal capacitance value can be as low as 1%. Class 2 capacitors boast a higher capacitance-to-volume ratio and are utilized in less sensitive applications. These capacitors typically exhibit thermal stability of around $\pm 15\%$ within the operating temperature range, with nominal value tolerances of approximately 20%.

Ceramic capacitors find diverse applications in various scenarios. Notably, they are employed in high-precision, high-power applications, such as in resonant circuits within transmitter stations. Additionally, they serve a crucial role in DC-DC converters, which subject components to significant stress in the form of high frequencies and electrical noise. Moreover, ceramic capacitors are commonly utilized as general-purpose capacitors, owing to their non-polarized nature and wide availability in a broad range of capacitances, voltage ratings, and sizes.

Silver mica capacitors incorporate mica, a group of sulcate minerals, as the dielectric medium. They present pronounced high-frequency attributes by virtue of low parasitic inductance and resistance, thereby maintain frequency-independent characteristics, rendering them useful to high-frequency applications. However, these properties are accompanied by



(a) (b)

Figure 4.26 Capacitance vs frequency and temperature for TDK MLCC [195].

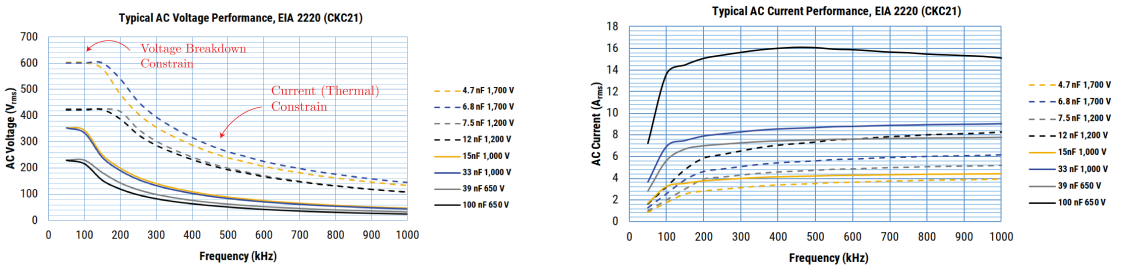
significant trade-offs, as silver mica capacitors exhibit a substantial form factor and commensurate cost. Nonetheless, their indispensability endures in specific domains; for instance, applications necessitating elevated power levels, such as in the realm of RF transmitters. Moreover, they remain extensively utilized in high-voltage applications due to mica's remarkable breakdown voltage.

In conclusion, all three types of capacitors share common and desired properties, namely independence of capacitance versus frequency and temperature, low ESR and ESL, low tolerance from nominal value, and longevity. Certain manufacturers offer, aside from datasheets, detailed information on these characteristics, for each capacitor separately, as illustrated in Fig. 4.26 for an indicative case of an MLCC. This can provide a holistic picture on the behavior of the capacitor in real-world scenarios.

Regarding the cost, for the same capacitance value and voltage rating, film capacitors are the most economical solution, with MLCCs following behind. Mica capacitors are extremely more expensive, especially when considering capacitances in the order of hundreds of nF and voltages up to 650 V. Therefore, micas are not further considered in this study.

Between film and MLCCs, the first type is generally more bulky for the same capacitance and rating from the second, but is also less expensive. However, MLCCs have better documentation and guaranteed to maintain the nominal capacitance regardless of the switching frequency and the temperature. In practice, both types were tested and they behaved as expected up to 1 kW of transferred power through the HFL.

Another figure that is regularly provided in datasheets, is the alternating voltage and current versus the switching frequency, for a family of capacitors. The different capacitance values are drawn as a parameter, as it is illustrated in Fig. 4.27. Fig. 4.27a and 4.27b carry complementary information, since the testing circuit consists only from an AC source and the capacitor. This means that initially, the maximum voltage is equal to the breakdown voltage of the component. As frequency increases and reactance $X_C = \frac{1}{2\pi f C}$ decreases, the applied voltage drops as the current passing through the capacitor increases. In the resonant



(a) (b)

Figure 4.27 Alternating voltage and current versus switching frequency for an indicative Kemet MLCC family [196].

converter, however, this is not the case, given that the current is set by the power flow and the impedance of the whole HFL.

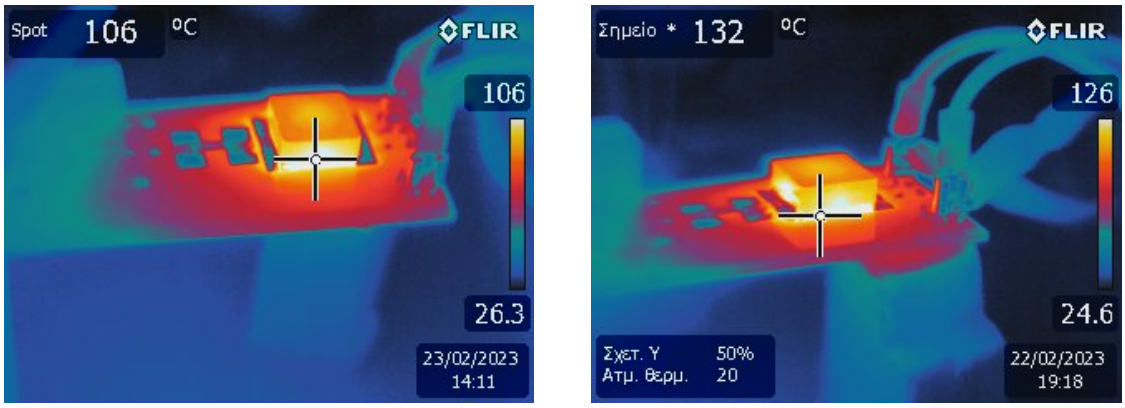
As it is presented in the previous subsections, for operation in the resonant and capacitive regions, the voltage across the capacitor exceed the voltage of the DC bus. This fact should considered during the selection of the proper capacitor for the HFL.

4.4.2 Resonant Inductor and Transformer

Air-cored inductors are relatively simple components, consisting only of copper wire with the proper architecture to achieve the desired inductance, as it is discussed in Chapter 3. The ohmic DC resistance (R_{DC}) can be calculated knowing the cross-section of the copper and its length. This may increase if the width of the copper is larger than the skin depth corresponding to the switching frequency of the converter, but can be calculated from improved Dowell's model, as in [197, 198, 199] or approximated. Calculating the efficiency is a straight forward process, since $P_{\text{IND.}} = \tilde{I}^2 \cdot R$. Hence, high-power high-frequency air-cored inductors are relatively easy to either select as an off-the-shelf component or create a custom design, only by considering the inductance and the nominal current (or resistance).

Acquiring an off-the-shelf cored inductor, with the desired current capability and inductance value, for high-frequency high-power applications in not a trivial task. Ferrite cores add another layer of complexity, introducing core losses, which depend on the magnetic field and the switching frequency, and non-linear effects, which are briefly discussed in Section 3.5, and are in detail analyzed in the literature. Most commercial cored inductors are designed with DC-DC power converters in mind, where the current has a large direct component with a small ripple. Utilizing these inductors as parts of the resonant circuit, where the current is alternating, can result in high temperatures for the ferrite, as illustrated in Fig. 4.28.

More specifically IHLP6767GZER470M51 of Vishay is a 47 μH shielded inductor that claims a maximum 7.25 A of direct current and 7 A saturation current. Under significantly lower conditions, operating as the LC-SR inductor with a sinusoidal current of approximately 2.8 A peak (or 2 A RMS), the ferrite develops temperatures up to 135 ^{o}C. Exceeding this



(a) $P_i = 100$ W **(b)** $P_i = 150$ W

Figure 4.28 Thermal images of Vishay 47 μH cored inductor [200], at $f_s = 100$ kHz.

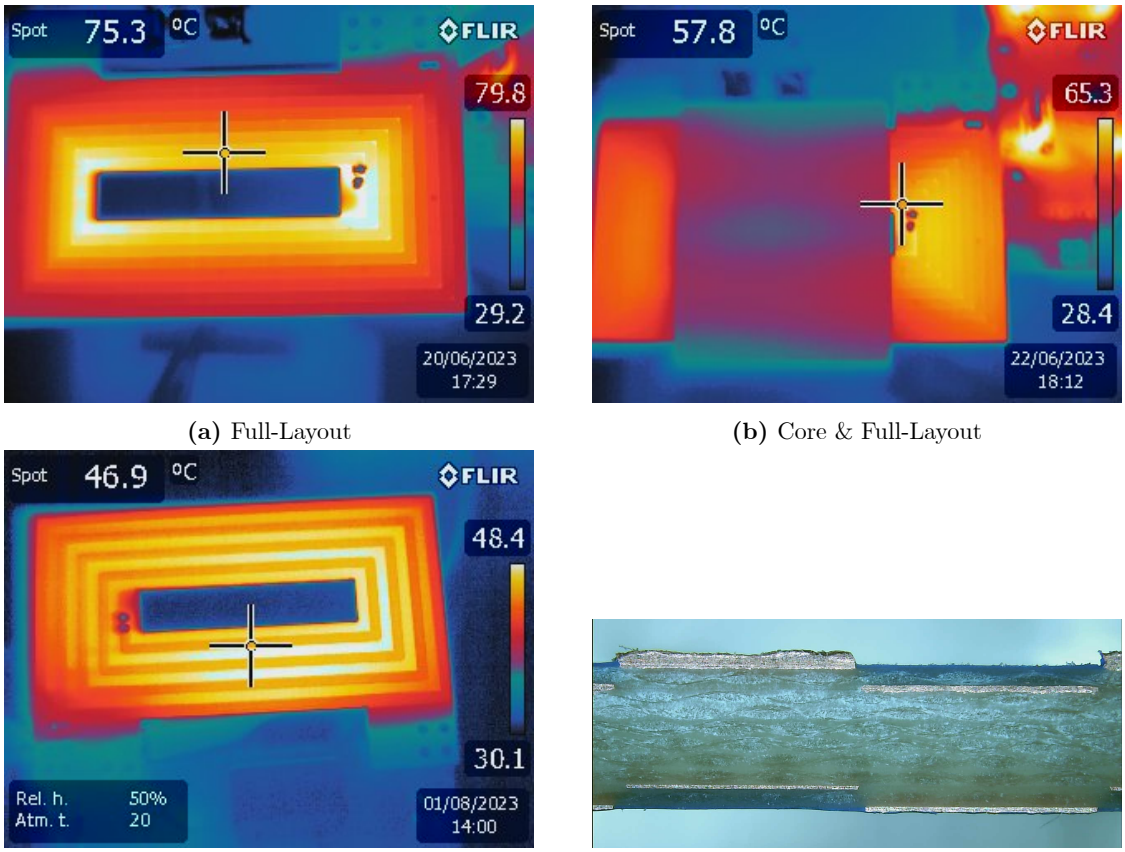
value may lead to the destruction of the inductor, so 150 W (approximately 75 V under 2 A) is the maximum power flow for the specific topology for this inductor. The introduction of a heatsink reduces the temperature and increases the maximum power up to 350 W. Only forced-air cooling can enable the 1 kW desired power transfer, but it is considered excessive for this application.

Contrary, a custom made planar inductor of approximately the same inductance can operate at notably lower temperatures, even for higher amounts of transferred power, as illustrated in Fig. 4.29. However, it should be noted that the planar windings that are depicted have a much larger surface area, compared to IHLP6767GZER470M51, and therefore can dissipate heat more efficiently.

The temperature of the winding in Fig. 4.29a can reach 80 ^{o}C in certain point, for $P_i = 500$ W. To reduce the operating temperature, without placing a heatsink, it is possible to introduce a ferrite core, like the one that is considered in Section 3.5. By doing so, the thermal mass is increased along with the surface area, resulting in the reduction of the temperature, which is also spread much more evenly on the surface of the winding. It should be noted that as the core produces its own losses, a more extensive study is required, to optimize the operation of the inductor and the HFL as a whole.

Another way to reduce the operating temperature is to redesign the planar inductor by removing half of the turns and thus increase the distance between two adjacent traces, as it is presented in Fig. 4.29c. For convenience, this design is named half-layout, since copper traces occupy only half of the surface area of the inductor. By reducing the number of turns per layer, the total inductance is reduced approximately 3.5 times. This can be compensated by increasing the number of layers, or adjusting the resonant capacitor to maintain the same resonant frequency.

Furthermore, half-layouts with proper alignment of the layers, as illustrated in Fig. 4.29d can lead to reduced parasitic capacitance. An alternative way to reduce the intrawind-



(a) Full-Layout

(b) Core & Full-Layout

(c) Half-Layout

(d) Half-Layout Cross-Section

Figure 4.29 Thermal images of custom planar windings, at $f_s = 100$ kHz and $P_i = 500$ W.

ing parasitic capacitance is alternating between primary and secondary, which is explored, specifically for the LLC converter, in [201]. To properly estimate and optimize the thermal behavior of a PW, a model has been proposed in [202], showing promising results and verified via FEM simulations and experimental measurements.

In conclusion, acquiring an off-the-self cored inductor for the HFL, while not impossible, is not trivial. Large distributors within EU, like Mouser, do not specifically categorize inductors based on their capability of handling pure alternating current or direct current with ripple. Some manufacturers, like Coilcraft [203], claim that they produce inductors for high-frequency high-power resonant applications, but the variety of available inductance values and current handling capability is limited. Utilizing a commercial air-core or designing one, cored or coreless, for the specific application can provide much better results.

Commercial high-power high-frequency transformers are generally not available from distributors and must be ordered from a manufacturer. In this case, the leakage inductance is utilized as the resonant inductor, and its value is usually available in the datasheet. Designing a custom transformer, tailored to the application needs is also an option, but

special care must be taken regarding the AC effects and the core (if one is used). Overall design characteristics and practices can be found in [136, 204, 205].

The voltage and the current for the capacitor and the inductor of the HFL can be derived from the time-domain analysis of Sections 4.2 and 4.3, for the LC-SR and the LLC converter respectively.

4.4.3 Switching Components

Losses on the primary bridge can be attributed to conduction $P_{\text{COND.}}$ and switching losses $P_{\text{SW.}}$ of the semiconductor devices. Conduction losses depend on the current and the conduction resistance $R_{DS,\text{ON}}$ or saturation voltage $U_{CE,\text{SAT}}$ for MOSFETs and IGBTs, respectively. For a given semiconductor device there are no measures the designer can take to reduce them, other than selecting the lowest possible $R_{DS,\text{ON}}$ or $U_{CE,\text{SAT}}$ for the nominal power current and U_{GE}. Considering the conduction losses, it is generally advised to select IGBTs for high-current applications since their losses increase linearly with the current, where for MOSFETs increase quadratically. However, this selection should take into account the switching frequency and the ratio f_s/f_0.

Switching losses depend on multiple factors, like the voltage and the current across the switch, and the overlap of their waveforms. The overlap is generally given as a function of rise (t_r) and fall (t_f) time, but each manufacturer uses slightly different notation. The transient behavior depends on characteristics of the switching device, like its type (unipolar, bipolar), the electron mobility, and the parasitic capacitance and inductance. As it is illustrated in [206], for a specific operating point and resonant circuit parameters, it is possible for one type of transistors to be much more efficient compared to the other.

Parasitic inductance is always present in any conductive path, bondwire, loop area etc. Designing as short as possible conduction paths and loop areas is always recommended for the minimization of voltage overshoots and switching losses. Parasitic inductance is also affected by the packaging of the semiconductor components. While datasheets do not provide any relative information, it is well known that larger packages (in volume and surface area) generally lead to increased inductance. Literature proposes various custom packaging designs, in order to reduce the parasitic inductance, tailored to the need of a particular application [207, 208, 209]. Other, off-the-shelf component packages, offer an auxiliary source or emitter as a forth leg, which can reduce the gate loop inductance and increase the efficiency of the transistors [210].

However, it would be interesting to investigate if the most popular packages, like TO-220, 247, 252, 263 etc., have an effect on the output parasitic capacitance of the semiconductor components. In hard-switching converters, in the off-state the output capacitances of the switch charge up to the DC bus voltage level. As soon the switch turns-on, the stored energy gets dissipated in the device, further increasing the switching losses. When a soft-switching

converter operates in inductive or resonant regions, the switches turn-on with the parasitic capacitances fully discharged, eliminating this issue. However, in the DCM region, the switch experiences turn-on losses due to this phenomenon.

The output capacitance $C_{oss} = C_{ds} + C_{gd}$ of several IGBTs, Si MOSFETs and SiC MOSFETs is considered, categorized by their packaging, and sorted in descending order. The breakdown voltages of the IGBTs and Si MOSFETs range from 600 to 650 V, and for the SiC MOSFETs from 650 to 900 V. The maximum current ranges from 15 to 35 A for the IGBTs, from 15 to 25 A for the Si MOSFETs, and from 25 to 35 A for the SiC. The data were collected from each datasheet, under similar testing conditions.

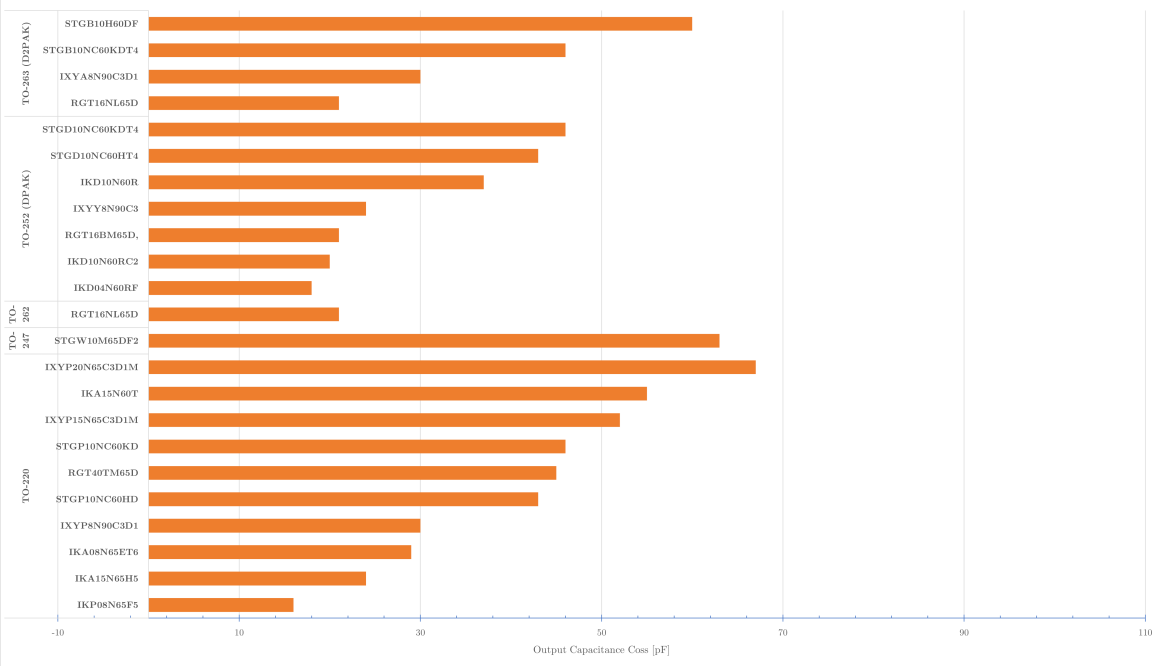


Figure 4.30 C_{oss} for 600-650 V 15-35 A IGBTs categorized by their packaging.

The capacitances of the selected IGBTs are illustrated in Fig. 4.30. As can be seen, all categories have components with high and low capacitance C_{oss}, and no subgroup presents systematically smaller C_{oss} values. It is possible to find components with $C_{oss} < 25$ nF in any category, although TO-252 (DPAK) appears to have the lowest mean value. This, however, could be related to the specific set of IGBTs that are selected and compared.

In Fig. 4.31 the capacitances of some selected Si MOSFETs are presented. In this case TO-252 (DPAK) and PQFN present systematically low C_{oss}, less than 30 and 35 nF, respectively. Nevertheless, it is possible to find components with the same capacitance for any other packaging.

Finally, in Fig. 4.32 the capacitances of some SiC MOSFET are illustrated. These components are rated for higher current and voltage breakdown, hence there are not many available in the 600-650 V range, in order for the comparison to be fair. Those that were

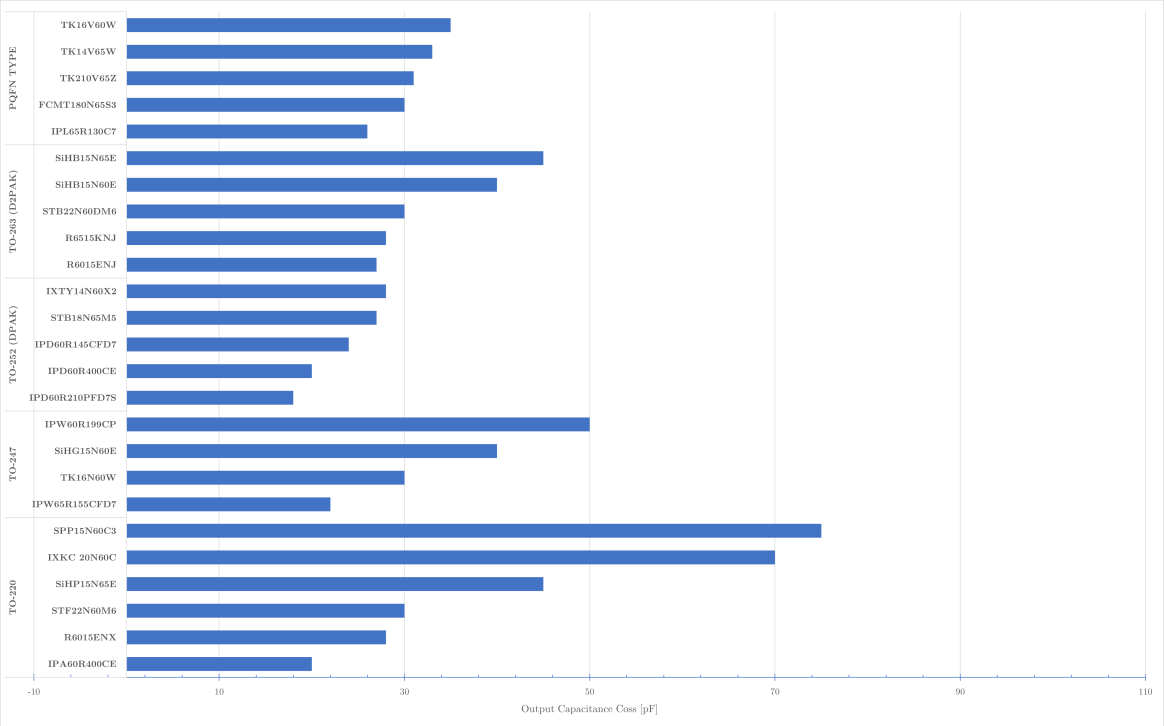


Figure 4.31 C_{oss} for 600-650 V 15-25 A Si MOSFETs categorized by their packaging.

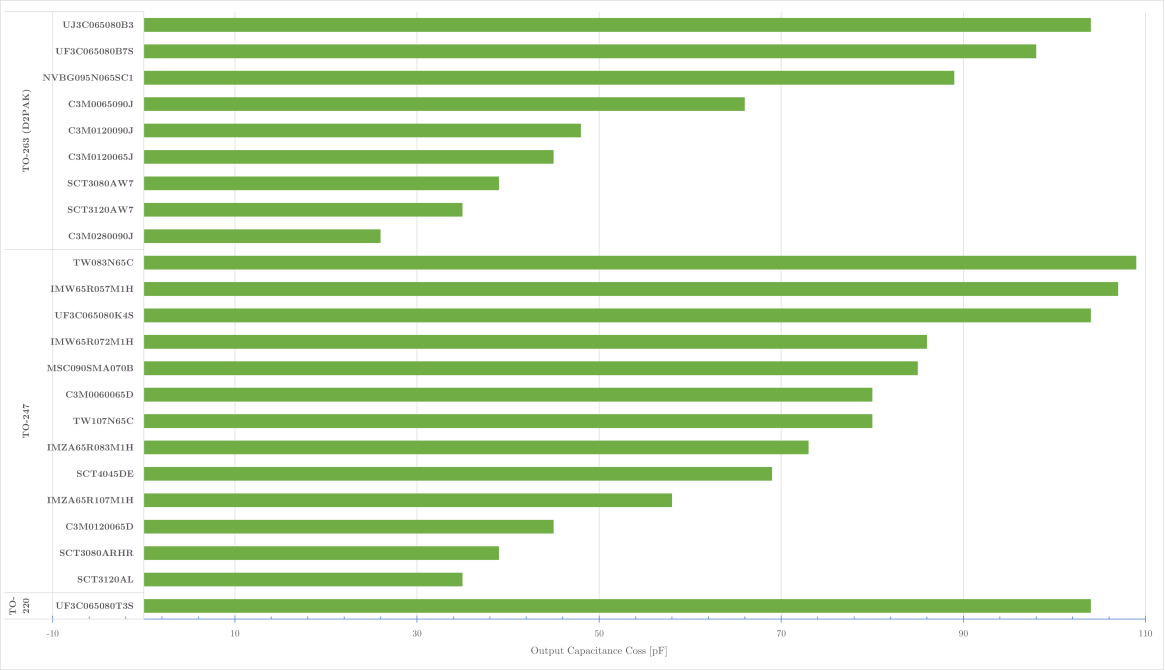


Figure 4.32 C_{oss} for 650-900 V 25-35 A SiC MOSFETs categorized by their packaging.

found present larger maximum current (and lower $R_{DS,\mathrm{ON}}$), but also generally greater output capacitance.

In conclusion, selecting low-profile and volume transistor packaging leads to reduced parasitic inductance and potentially lower parasitic capacitance. The designer should also consider the voltage overshoot during commutations in order to properly select the switching device. The overshoot depends, also, on the parasitic inductance of the PCB, the value of the gate resistor, and the switching frequency. Experimentally determining the gate resistance for a given PCB and semiconductor seems the most efficient solution, but further research is required in order to provide a model that can offer the optimal $\boldsymbol{R_G}$ without the need of exhaustive laboratory experiments.

4.5 Conclusions

In this chapter the topic of high-energy-density resonant converters is discussed, presenting their benefits and inherent advantages, including low or zero switching losses, reduced EMI, easy magnetic integration and possible improvement by utilizing SiC-based transistors. The most important issues that arise when the converter is not properly designed and controlled are also discussed, such as increased conduction and switching losses, increased losses in the magnetic components, and paralleling (or interleaving) for increased power-handling capability. A brief state-of-the-art review on treating such issues in made, presented the most recent articles and overviews in controlling schemes. Furthermore, the frequency- and time- domain mathematical models which have been developed are presented for a wide variety of LC-SR and LLC, single-active bridge topologies.

The LC-SR converter is analyzed in great detail in the time-domain. The function and equations of each part are presented and simplified equivalent circuits are derived. The operation is divided into four separate regions, inductive, resonant and continuous and discontinuous conduction capacitive region, focusing on the resonant current that passes through the high-frequency link and the voltage drop across the resonant capacitor. The initial values for each region are derived, giving a closed-form solution for every possible operation point. Based on this analysis, the conditions to commutate under ZVS or ZCS for the primary bridge components are presented. The boundary conditions between capacitive CCM and DCM operation are obtained, and an experimental verification is carried out, comparing MOSFETs and IGBTs for the different operating regions.

The differential equations that describe the operation of the LLC converter are also presented, like in the LC-SR case. The behavior of the high-frequency link, regarding the load and the magnetizing inductor, is presented, along with the simplified equivalent circuits. In the LLC case, the separation between inductive and capacitive operating region is not defined only by the switching frequency, as in LC-SR, but also from the load and the resonant tank parameters. The operation under heavy and light load is used to provide insight in the boundary condition between type A and B regions, corresponding to the CCM and DCM of the LC-SR. Some of the initial values of the differential equation solutions are challenging to derive, due to the complexity of the circuit, but good approximation equations are provided, verified via simulations.

Finally, a guide on the selection of the passive resonant and active components is presented. Three capacitor type candidates are considered, namely film, ceramic, and mica, with the third been rejected due to its significantly higher cost. The issues related with the selection of an off-the-shelf inductor are discussed, and the need for custom design are presented. Namely, AC commercial inductors are difficult to obtain and high-frequency high-power transformers are not available from large distributors and require to be ordered from the manufacturer. The selection of the active components should be based on the specific

characteristics of the application and the cost. Low profile packaging can be advantageous, since they reduce the inherent inductance and in some cases the output capacitance. SiC-based transistors can be considered if the extra cost for the gate driver and the device itself is acceptable.

The tools developed for the aforementioned analyses can also be used to provide accurate time-domain models for the LC and LLC dual-active bridge converters, in the future. The main difference stands in the fact that DABs do not naturally change states with the sign of the resonant current, but force commutations by controlling the secondary bridge, which has an active source capable of power production and consumption. Moreover, a more extensive study on the behavior of different types of transistors is required, to highlight the advantages and disadvantages as well as the optimal configuration (supply voltage, gate resistance, dead-time, etc.) for efficient operation, for each separate region.

Parts of this topic are discussed in [211], where a method of achieving zero-switching losses while in DCM operation for the LLC is highlighted. In [70], a method for estimating MOSFET losses for a half-bridge LLC converter is presented. In [212], the dead-time range is calculated for achieving ZVS, via improved TDA for the LLC, with respect to the output capacitances of the MOSFETs. Further investigation is mandatory to connect these approaches, include the effect of the gate resistance, and compare the different types of semiconductors.

Chapter 5

Conclusions and Future Research

5.1 Conclusions

This dissertation aims to contribute to the vast topic of resonant converters, addressing issues that arise with an improper PCB layout and providing a set of good designing practices. It is generally advised to design high-frequency traces (independently of their power level) as short as possible and with small cross-sectional area. However, to minimize the undesirable parasitic capacitance between AC traces, return paths should not overlay the positive traces. Placing the bypass/decoupling capacitors close to the components, as well as minimizing the trace length and loop inductance area, improves their performance.

When multilayer boards are used, optimizing the layer sequence, as discussed in subsection 2.3.2, can reduce switching losses up to 26%. Special consideration must be given to the surface area of switching nodes, to improve thermal dissipation, reduce voltage oscillations across the switching device, and reduce EMI. Placing switching devices in parallel should also be carefully done, equalizing the parasitic inductances on drain, source and gate traces, respectively, to improve current sharing between the devices.

Furthermore, this work delves into the field of planar magnetics. This type of windings can be utilized as inductors and transformers, offering low manufacturing cost, highly repeatable inductance in mass production, and low z-profile. The geometric parameters are analyzed and their effect on the inductance is discussed. Three well-established equations, for estimating the inductance of square-shaped planar windings, are modified to properly accommodate for the rectangle-shaped case. The modified Wheeler and Rosa equations provide as accurate estimations as the original equations with less that 1.5% mean absolute error. In addition, the developed voltage (or inductance) per turn is presented, a useful detail for designing robust components.

Multilayer rectangle-shaped windings introduce another designing degree of freedom, as multiple layers can be stacked one upon the other, increasing the inductance exponentially while maintain low z-profile, typically from 0.8 to 2.0 mm. The modifications applied on

Wheeler and Rosa equations can provide accurate results for two-layered boards and for some cases for three-layered boards. A new data-fitted monomial-like equation is presented, providing accurate results for a wide range of winding dimensions and up to 4-layer boards. The error mean value is 0% with a 1.77% standard deviation and a less than 1.5% mean absolute error.

Custom designs can further decrease the parasitic capacitance by increasing the vertical distance between the layers, without compromising the low-z profile of the winding. For example two 1.6 mm two-layered boards connected in series with a blank intermediate 1.6 board, can greatly reduce the capacitance, and keep the its height relative low at 4.8 mm.

A comparison between the modified and new equations shows that for single-layer boards Wheeler and Rosa provide the most accurate results, with less than 2% mean absolute error, independently of the deformation ratio $\boldsymbol{D_1/D_2}$. The new monomial-like equations follows closely with less than 4%, but presents systematically the best results for multilayered boards.

This chapter closes with a brief investigation on the effects the ferrite core introduces. A review of the losses estimation equation is presented, along with the core selection criteria. The equivalent magnetic circuit, for the most usual case, is presented and the reluctance and magnetic flux for each leg are derived. The effect of the air-gap is briefly commented. It is, however, necessary to expand this topic, in order to better describe the behavior of cored inductors and transformers.

Finally, this research provides an exhaustive analysis for the single-active bridge LC-SR and LLC converters, in the time-domain. The operation regions of the converters are defined based on the switching frequency with respect to the resonant frequency of the HFL, providing an in-depth understanding and closed-form solutions of every voltage and current of the converter. The properties of each region are discussed, and especially for the capacitive case, the distinction between continuous and discontinuous current modes is highlighted.

For the SAB LC-SR case, an experimental verification of the theoretical and simulation analysis is carried out. The advantages of operating in capacitive DCM region over the CCM are verified, and a comparison of the three CCM, DCM and inductive regions, for MOSFETs and IGBTs is presented. Depending on the type of the semiconductor switch, inductive or DCM may be preferable, but further investigation is necessary.

The selection of the proper active and passive components for these types of converter is discussed. MLC and film capacitors present the best behavior, with constant capacitances in a wide range of frequencies and peak voltages. The issues with commercial inductors are presented, along with the behavior of the custom-designed planar windings. A comparison between different types of semiconductor packaging and output capacitance is presented.

5.2 Future Research Suggestions

Regarding the analysis and behavior of planar windings, the effect of the parasitic capacitance reduction techniques on the accuracy of the proposed modified and new equations should be discussed. As presented in Chapter 3, designing half-layouts, windings with larger distance between layers, or interleaved layers, can significantly reduce the capacitance, but it is undetermined if the estimation equations can still provide accurate results. Further investigation is also necessary for the accuracy of the proposed equations in windings with more layers ($N_L \geq 8$), which are present in interleaved architectures.

In addition, the extension of the equations when a ferrite core is utilized should be considered. There is an open question if the presented equations are capable of estimating the inductance of a winding by replacing μ_0 with $\mu = \mu_0\mu_r$. The term μ_r is not the permeability of the core, which is usually given in the datasheet, but the effective permeability which considers the cross-section of the core, the magnetic path length, and any potential air-gap.

As for the resonant converter analysis, it is crucial to develop a detailed power losses model with respect to the different dominant semiconductor types (IGBT, Si and SiC MOSFETs, and GaNs). This will provide a better and in-depth understanding of the conduction and switching losses, taking into account the specifics of the resonant circuits, and accommodate in the better selection of switching devices depending on the application.

The same model must consider the effects of the gate resistance, the parasitic input/output capacitances, as well as the trace inductance, to provide an optimization tool for selecting the R_G. The gate resistance should be large enough to suppress the voltage overshoot across the switching devices, but small enough to enable fast commutations and hence minimization of the switching losses that are present even in resonant converters. Finally, the same model should address the switching losses issues that arise with the DCM operation of LC-SR converters, defining the best operating conditions when voltage regulation is needed and the converter operated below its resonant frequency.

Moreover, the time-domain analysis should extend to the dual-active bridge for the LC-SR, LLC and CLLC high-frequency links. As it is discussed in Chapter 1, DABs, and in fact multiple active bridge topologies (TAB, QAB, etc.) are capable of revolutionizing the power management and routing paradigm. DABs offer high-efficiency low-volume solutions on power level and flow control, interconnecting different types of electric energy (DC and AC, LV and MV).

Their operation is similar to that of SAB, which is discussed in Chapter 4, but with two main differences: (i) the load is not a network of passive components (resistors, capacitors, and inductors), but an active voltage source capable of sinking and sourcing power, and (ii) the phase difference between the input and the output of the high-frequency link is not dictated by the natural commutation of the resonant circuit, but from the phase difference between the two bridges, which is defined by the control system of the converter, and it is

in fact the variable that dictates the power level and direction. Nevertheless, the operation regions are similar to those of the SAB converter, including inductive, and CCM - DCM capacitive regions.

Finally, it is important for the entire power electronics community to address the issues that arise with high-power high-frequency converter designs. The practices suggested in Chapter 2 are the tip of the iceberg, and offer only partial solutions. A more systematic review is required to direct designers to the best practices regarding: (i) the casing of the transistor (discrete through-hole and surface mount, modules, PCB embedded, etc.) (ii) bypass and decoupling capacitors placement, (iii) electromagnetic interference mitigation within the board and with external boards, with proper via drilling and plane placement and (iv) the controversial topic of large ground planes within the board and the noise propagation.

Appendix A

Semiconductor Losses

The efficiency of the converter is mostly determined by the losses of the semiconductor devices. Due to their non-ideal operation, these devices present two types of losses: (i) conduction losses, which are present when the transistor conducts current, and (ii) switching losses, which occur on every transition of the transistor (from ON to OFF, and from OFF to ON). In order to properly model these losses the transistor type (MOSFET, IGBT, etc.) is important, as each type presents relatively different behavior.

A.1 Conduction Losses

Conduction losses in semiconductor devices, such as MOSFETs and IGBTs, are critical for the efficiency of the power converter. These losses occur during the device "on" state when it conducts current, and they manifest as resistive losses due to the finite on-state resistance $R_{DS,\text{on}}$ for MOSFETs and the saturation voltage $V_{CE,sat}$ for IGBTs.

The magnitude of conduction losses for MOSFETs is directly proportional to the square of the current passing through the device,

$$P_{\text{cond,MOS}} = R_{DS,\text{on}} I_D^2, \tag{A.1}$$

resulting in a square increase with increasing current. As a result, the utilization of single MOSFETs in high-current application may present issues, such as suboptimal efficiency and high-temperature operation. Selecting a device with low $R_{DS,\text{on}}$ and placing multiple in parallel can greatly benefit the converter and mitigate the aforementioned issues.

For IGBTs the magnitude of conduction losses are

$$P_{\text{cond,IGBT}} = V_{CE,sat} I_C, \tag{A.2}$$

resulting in a linear increase with respect to the current. IGBTs generally have a wide range of breakdown voltages, and can handle tens or even hundreds of amperes. This makes them

suitable candidates for a wide variety of applications. However, due to their solid-state physics as bipolar devices, they present significantly less high-frequency operation capabilities, which are limited from their temperature as the frequency increases. This is discussed in Section A.2.

As an example regarding the conduction losses, consider a MOSFET with $R_{DS,\text{on}} = 100$ mΩ, and an IGBT with $V_{CE,sat} = 1.5$ V. For sake of simplicity these values remain constant and are independent of the operating temperature. For currents up to 15 A, the MOSFET device presents lower losses. If the current is greater than 15 A, the IGBT would be a better option, at least from a conduction-loss perspective.

A.2 Switching Losses

Switching losses in semiconductor devices, including MOSFETs and IGBTs, are a crucial aspect of power electronics. These losses arise during the transition periods when the devices switch between their "on" and "off" states, and they manifest in two components: (i) turn-on losses, which occur when the device transitions from the off-state to the on-state, and (ii) turn-off losses, which take place during the shift from the on-state to the off-state. The magnitude of switching losses is determined by several factors, including the switching frequency, the operating voltage, and the characteristics of the semiconductor device itself.

A.2.1 MOSFETs

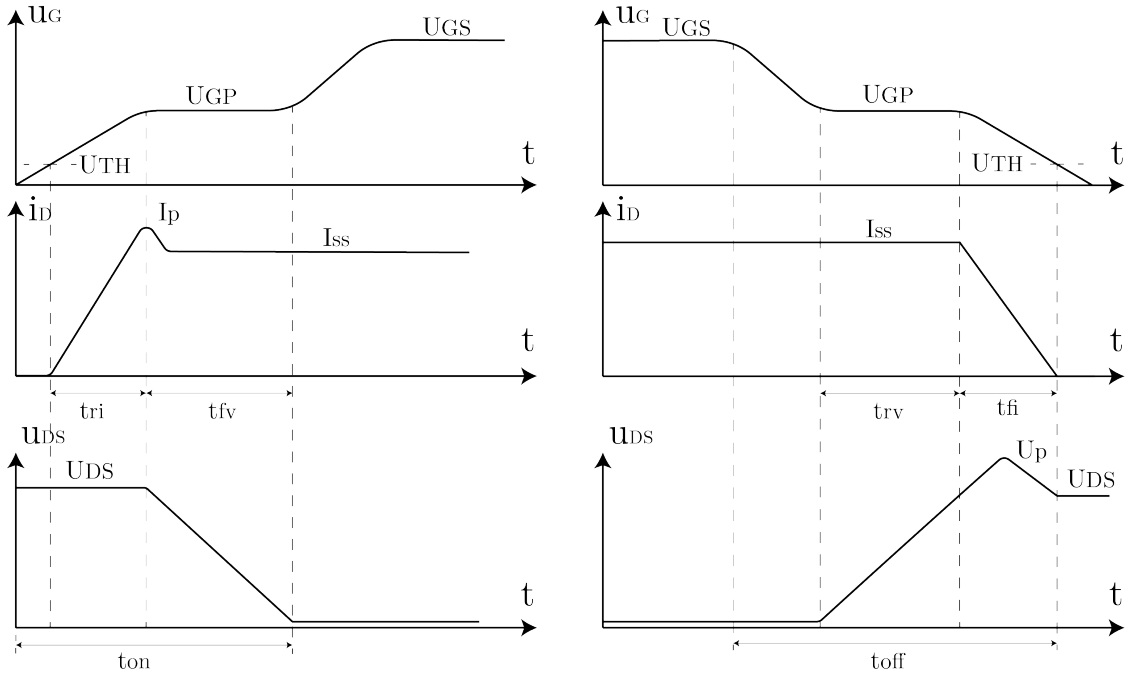
In the case of MOSFETs, switching losses primarily result from the charging and discharging of the parasitic capacitances during transitions, as it is illustrated in Fig. A.1. These losses exhibit a proportionality to both the switching frequency and the applied voltage, and they can be a significant factor in high-frequency applications.
The turn-on switching losses are

$$E_{\text{on}} = \int_{t_{\text{on}}} u_{DS}(t) i_D(t) \mathrm{d}t, \tag{A.3}$$

where, u_{DS} is the voltage across the source and drain of the device, and i_D is the current passing through. In [213], an approximation has been proposed, as

$$E_{\text{on}} = \frac{1}{2} U_{DS} I_p t_{ri} + \frac{1}{2} U_{DS} \left(\frac{1}{3} I_{ss} + \frac{2}{3} I_p \right) t_{fv}, \tag{A.4}$$

where, as illustrated in Fig. A.1a, U_{DS} is the operating voltage, I_{ss} is the steady-state current, I_p is the peak current, t_{ri} is the time interval in which the current rises to I_p while the voltage remains almost constant, and t_{fv} is the time interval in which the voltage drops to approximately zero and the current sets to its steady-state value. During this period, the



(a) Turn-on **(b)** Turn-off

Figure A.1 Commutation of a MOSFET device.

Miller effect is visible, as the parasitic capacitance for gate-to-drain C_{DS} discharges from the operating voltage to zero.

Similarly, the switching losses during turn-off are

$$E_{\text{off}} = \int_{t_{\text{off}}} u_{DS}(t) i_D(t) \mathrm{d}t, \tag{A.5}$$

and they can be approximated as

$$E_{\text{off}} = \frac{1}{2} U_{DS} I_{ss} t_{rv} + \frac{1}{2} U_p I_{ss} t_{fi}, \tag{A.6}$$

where, as illustrated in Fig. A.1b, U_p is the peak voltage, t_{rv} is the time interval in which the voltage across the device raises to its operating value, and tfi is the time interval in which the current drops to zero. This steep current transition $\mathrm{d}i/\mathrm{d}t$, in combination with the parasitic inductance L_{par} of the path, produces an over-voltage across the device, which can by approximated by $L_{par}\mathrm{d}i/\mathrm{d}t$.

The total switching losses are the sum of the turn-on and turn-off losses, as in

$$E_{\text{total}} = E_{\text{on}} + E_{\text{off}}, \tag{A.7}$$

and the total energy dissipated is

$$W_{\text{sw}} = E_{\text{total}} f_s. \tag{A.8}$$

Determining the time intervals t_{ri}, t_{vf}, t_{rv}, and t_{fi}, is far from trivial. They depend on the parasitic capacitances of the device, the internal and external gate resistance, as well as the current capabilities and voltage of the gate driver. As it is proposed in [213], the rise and fall time of the current depends on the gate resistance and the input capacitance, as in

$$t_{ri} \sim R_G(C_{GS} + C_{GD}), \tag{A.9}$$

$$t_{fi} \sim R_G(C_{GS} + C_{GD}), \tag{A.10}$$

and the fall of the voltage

$$t_{fv} \sim R_G C_{GD} \tag{A.11}$$

In [214] an estimation for the time intervals has been proposed. Namely

$$t_{ri} = R_G C_{iss} \ln \frac{U_{GS} - U_{TH}}{U_{GS} - U_{GP}}, \tag{A.12}$$

$$t_{fv} = R_G C_{GD} \frac{U_{DS}}{U_{GS} - U_{GP}}, \tag{A.13}$$

$$t_{rv} = R_G C_{GD} \frac{U_{DS}}{U_{GP}}, \tag{A.14}$$

$$t_{fi} = R_G C_{iss} \ln \frac{U_{GP}}{U_{TH}}, \tag{A.15}$$

where $C_{iss} = C_{GS} + C_{GD}$ is the input capacitance, U_{GS} the gate-source voltage of the gate driver, U_{TH} the threshold voltage of the MOSFET, and U_{GP} the Miller plateau voltage.

Depending on the manufacturer, the datasheet of a device may or may not provide the necessary variable to accurately estimate the transition time intervals. Especially as the capacitances are non-linear, the equivalent gate charge may by used instead of the given datasheet capacitance. The value of C_{GD} can be derived by dividing the gate charge Q_{GD} with the voltage swing U_{DS}, i.e.,

$$C_{GD} = \frac{Q_{GD}}{U_{DS}}, \tag{A.16}$$

which can be replaced in (A.13) and (A.14).

Similar equations have been proposed in [215], where the geometric and electrical characteristics of the MOSFET have been incorporated in the equations. This may not be as useful

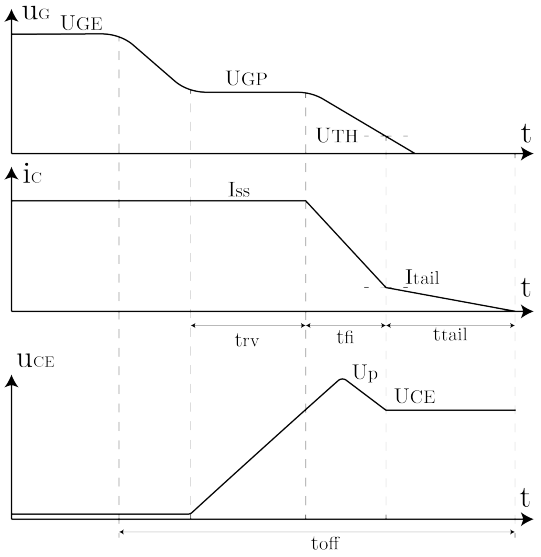


Figure A.2 Turn-off of an IGBT device.

as the datasheet-based estimation of switching losses, but can provide a better understanding on the inner-workings of the losses mechanisms.

A.2.2 IGBTs

Regarding the IGBTs, the turn-on process is similar to that of the MOSFETs, hence (A.4) still applies, and can be rewritten as

$$E_{\text{on}} = \frac{1}{2}U_{CE}I_p t_{ri} + \frac{1}{2}U_{CE}\left(\frac{1}{3}I_{ss} + \frac{2}{3}I_p\right)t_{fv}. \tag{A.17}$$

However, during turn-off, a tail-current appears as a result of the remaining charge carriers, as it is illustrated in Fig. A.2.The losses are given by

$$E_{\text{off}} = \frac{1}{2}U_{CE}I_{ss}t_{rv} + \frac{1}{2}U_p I_{ss}t_{fi} + \frac{1}{2}I_{\text{tail}}U_{CE}t_{\text{tail}}. \tag{A.18}$$

Time interval t_{tail} can be up to several microseconds, in contrast with the hundreds of nanoseconds of t_{rv} and t_{fi}. Thus, although the I_{tail} is smaller compared to the initial value of the current for the other regions, the losses that take place in the last section cannot be ignored. Determining the time interval t_{tail} and the initial value I_{tail} can be challenging. Even oscilloscope waveforms contain noise that makes it difficult to define the exact points where the phenomenon starts and ends.

Usually manufacturers provide E_{on} and E_{off} values, for specific operating conditions, so the switching losses can be estimated directly from these quantities.

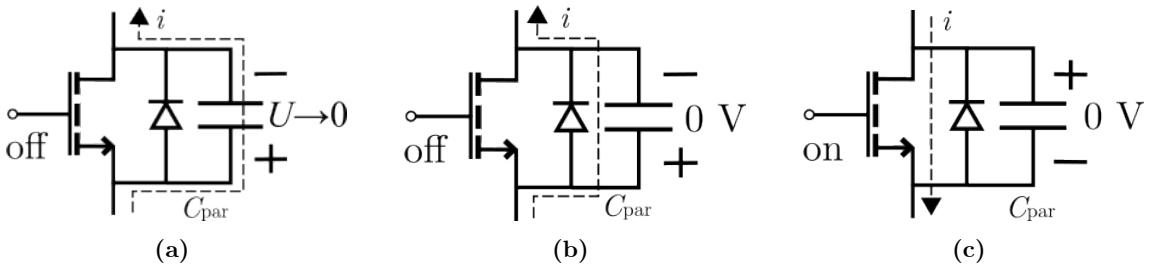


Figure A.3 MOSFET turn-on under ZVS.

As in the MOSFETs case, in [215] the approximation is based on the geometrical and electrical characteristics for the losses. Furthermore, a comparison is carried out between the losses in symmetric, asymmetric, and transparent emitter IGBTs.

A.3 Zero-Voltage-Current Switching

As it is discussed in Chapter 4, using proper auxiliary components and under certain conditions, it is possible to reduce or even eliminate switching losses. The mathematical model for these transitions in the LC-SR and the LLC converter are discussed in detail in the aforementioned chapter. In this section the exact zero-voltage or zero-current mechanisms are discussed, from the perspective of the semiconductor device.

A.3.1 Turn-on

As illustrated in Fig. A.3, during dead-time, the inductive current that passes through the anti-parallel diode of the MOSFET, first discharges the parasitic output capacitor of the MOSFET. If the dead-time interval and the inductive current are large enough the capacitor is fully discharged, and the current continue to flow through the diode,clamping the voltage across the device to almost 0 volts. Hence, when the turn-on pulse is given to the gate of the MOSFET, the devices turns-on under zero-voltage and presents no losses or zero-losses switching (ZLS).

In the case that the dead-time is not long-enough and the current is small, the capacitor will be partially discharged, hence the device experiences some losses, but reduced compared to the conventional hard-switch transition. This transition is called incomplete- or partial-zero-voltage-switching (iZVS).

When the switching devices do not interrupt the power current during their transition, the commutation is called zero-current turn-on. This can be achieved, for example, when the power path has an inductor strong enough to limit the raise of the current during turn-on, like in the LC-SR converter which is discussed in Chapter 4. However, the parasitic capacitor of the MOSFET charge up to the voltage of the DC bus. Since there is no current flowing in the circuit, the capacitor remains charged up during the dead-time interval. As soon as

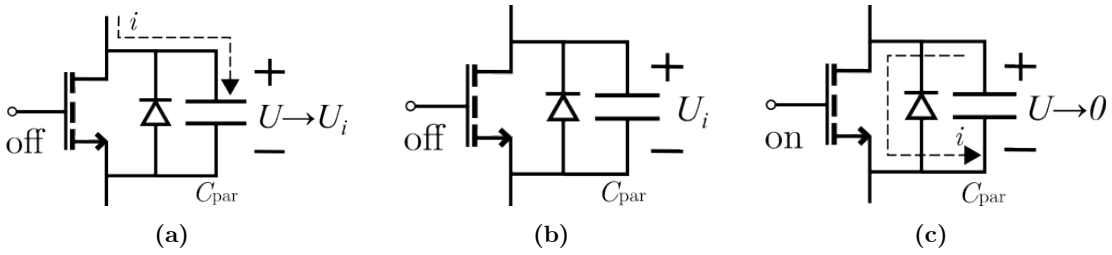


Figure A.4 MOSFET turn-on under ZCS.

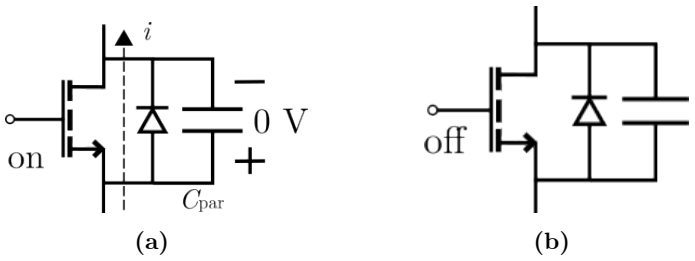


Figure A.5 MOSFET turn-off under ZVS.

a pulse is driven to the gate of the MOSFET, the channel begins to form and the capacitor discharges, creating a current that passes through the MOSFET, thus producing losses. This process is presented in Fig. A.4 and the losses are given as

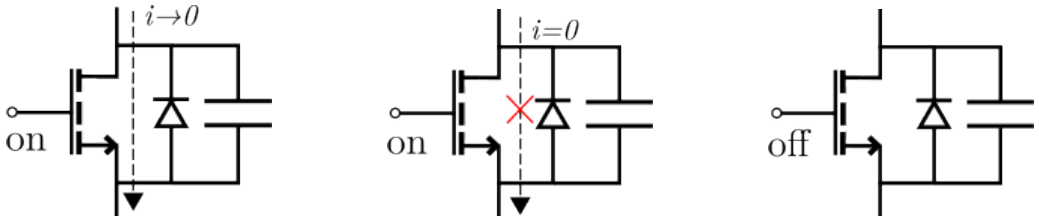
$$E_{\text{on}} = \frac{1}{2} C_{oss} U_i^2. \tag{A.19}$$

A.3.2 Turn-off

The turn-off process can be conducted under zero-voltage switching, as it is illustrated in Fig. A.5. The current passes from the source to the drain and clamps the voltage across the device to approximately zero. Then the pulse on the gate goes to zero, the transistor turn-off without any losses. If the current persist on flowing in the same direction, it passes through the antiparallel diode. ZVS-off can also be related with small $|\mathrm{d}u/\mathrm{d}t|$, compared to the $|\mathrm{d}i/\mathrm{d}t|$, which is the case when the capacitance between drain-source is large enough. However, this can produce significantly larger losses during the turn-on process.

In Fig. A.6 the turn-off process under zero-current switching is illustrated. The current that initial passes through the transistor reduces to zero, as the gate pulse is still high. Then, when the gate is grounded, the transistor turns-off without losses. In this case, there are not any other losses related to the output capacitor, as it was discussed for the ZCS-on case.

When the commutation of the transistor is not under hard- or zero-losses switching, but performs an incomplete-soft switching, the actual losses can be estimated by the equations that are presented in Section A.2, and from A.19. In this case, the E_{on} and E_{off} given in the



(a) (b) (c)

Figure A.6 MOSFET turn-off under ZCS.

datasheet of an IGBT are not particularly useful, and a method is required to estimate the tail current initial value and duration.

A.3.3 MOSFET and IGBTs

The aforementioned analysis can, at least partially, explain the behavior of the two types of transistors that is presented in Fig. 4.14 for the LC-SR converter. Since the tail-current is a predominant form of losses for the IGBTs, the capacitive DCM operation if beneficial as it suppresses it. In the inductive operation, where the IGBT experiences ZVS-on and hard turn-off, presents the greatest losses, but CCM operation, where the IGBT experiences ZVS-off and hard turn-on is very close. This difference can be mainly attributed to the switching frequency, since the IGBT turns on and off 50% more (120 kHz compared to 80 kHz) each second.

The MOSFET device can be greatly benefited from the inductive operation, where the output capacitance has been fully discharged prior the turn-on. Increasing the input power does not seem to affect the total losses in any significant manner, in contrast to any other operation region. However, DCM operation is better compared to CCM, although the output capacitor during DCM discharges through the channel of the MOSFET.

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Acronyms / Abbreviations

ACT	Air-Cored Transformer
CCM	Continuous Current Mode
CT	Cored Transformer
DAB	Dual Active Bridge
DCM	Discontinuous Current Mode
DCX	DC Transformer
EMC	Electromagnetic Compatibility
EM	Electromagnetic
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
EVC	Electric Vehicle Charging
FEM	Finite Element Method
GMV	Generalized Mean Value
GMMV	Geometric Mean Value
GND	Ground
FBR	Full-Bridge Rectifier
HFL	High Frequency Link
HP-HF	High-Power, High-Frequency
IPT	Inductive Power Transfer
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Silicon Field-Effect Transistor
MLR	Multiple Linear Regression
OBC	On-Board Charging
PCB	Printed Circuit Board
PTF	Planar Transformer
PV	Photovoltaic
PWM	Pulse Width Modulation
PW	Planar Winding
PWR	Power
RES	Renewable Energy Sources

LxRPW	x-Layer Rectangle Planar Winding
MLRPW	Multilayer Rectangle Planar Winding
RPW	Rectangle Planar Winding
SAB	Single Active Bridge
SIG	Signal
SST	Solid-State Transformer
TAB	Triple-Active Bridge
TF	Transformer
WPT	Wireless Power Transfer
ZCS	Zero-Current Switch
ZLS	Zero-Losses Switch
ZVS	Zero-Voltage Switch

Glossary (Γλωσσάριο)

Alternating Current (AC)	Εναλλασσόμενο Ρεύμα (ΕΡ)
Capacitive Regions	Χωρητική Περιοχή Λειτουργίας
Continuous Current Mode (CCM)	Λειτουργία Συνεχούς Αγωγής
Direct Current (DC)	Συνεχές Ρεύμα (ΣΡ)
Discontinuous Current Mode (DCM)	Λειτουργία Ασυνεχούς Αγωγής
Dual Active Bridge	Μετατροπέας Διπλής Ενεργού Γέφυρας
Generalized Mean Value	Γενικευμένος Μέσος Όρος
High-Frequency Link	Δίκτυο Ζεύξης Υψηλής Συχνότητας
First-Harmonic Approximation	Προσέγγιση Πρώτης Αρμονικής
Hard Switching	Σκληρή Μεταγωγή
Inductive Region	Επαγωγική Περιοχή Λειτουργίας
Inverter (DC-AC)	Αντιστροφέας (ΣΡ-ΕΡ)
Mean Absolute Error	Μέση Τιμή Απόλυτης Τιμής Σφαλμάτων
Monomial	Μονώνυμο
Multilayer Planar Winding	Επίπεδο Τύλιγμα Πολλαπλών Επιπέδων
Multiple Linear Regression	Πολλαπλή Γραμμική Παλινδρόμηση
Printed Circuit Board (PCB)	Πλακέτα Τυπωμένου Κυκλώματος (ΠΤΚ)
Pulse Width Modulation	Διαμόρφωση Εύρους Παλμών
Planar Winding	Επίπεδο Τύλιγμα (ή Επαγωγός)
Plane (in PCB)	Αγώγιμη Επιφάνεια (σε ΠΤΚ)
Rectifier (AC-DC)	Ανορθωτής (ΕΡ-ΣΡ)
Resonant Converter	Μετατροπέας (Τύπου) Συντονισμού
Resonant Region (or Operation)	Περιοχή ή Λειτουργία Συντονισμού
Soft Switching	Ομαλή Μεταγωγή
Switching Node	Διακοπτικός Κόμβος
Time-Domain Analysis	Ανάλυση στο Πεδίο του Χρόνου
Trace (in PCB)	Αγώγιμος Δρόμος (σε ΠΤΚ)
Zero-Current Switching	Μεταγωγή υπό Μηδενικό Ρεύμα
Zero-Voltage Switching	Μεταγωγή υπό Μηδενική Τάση